TSEK01 Project Hints and Example Mistakes

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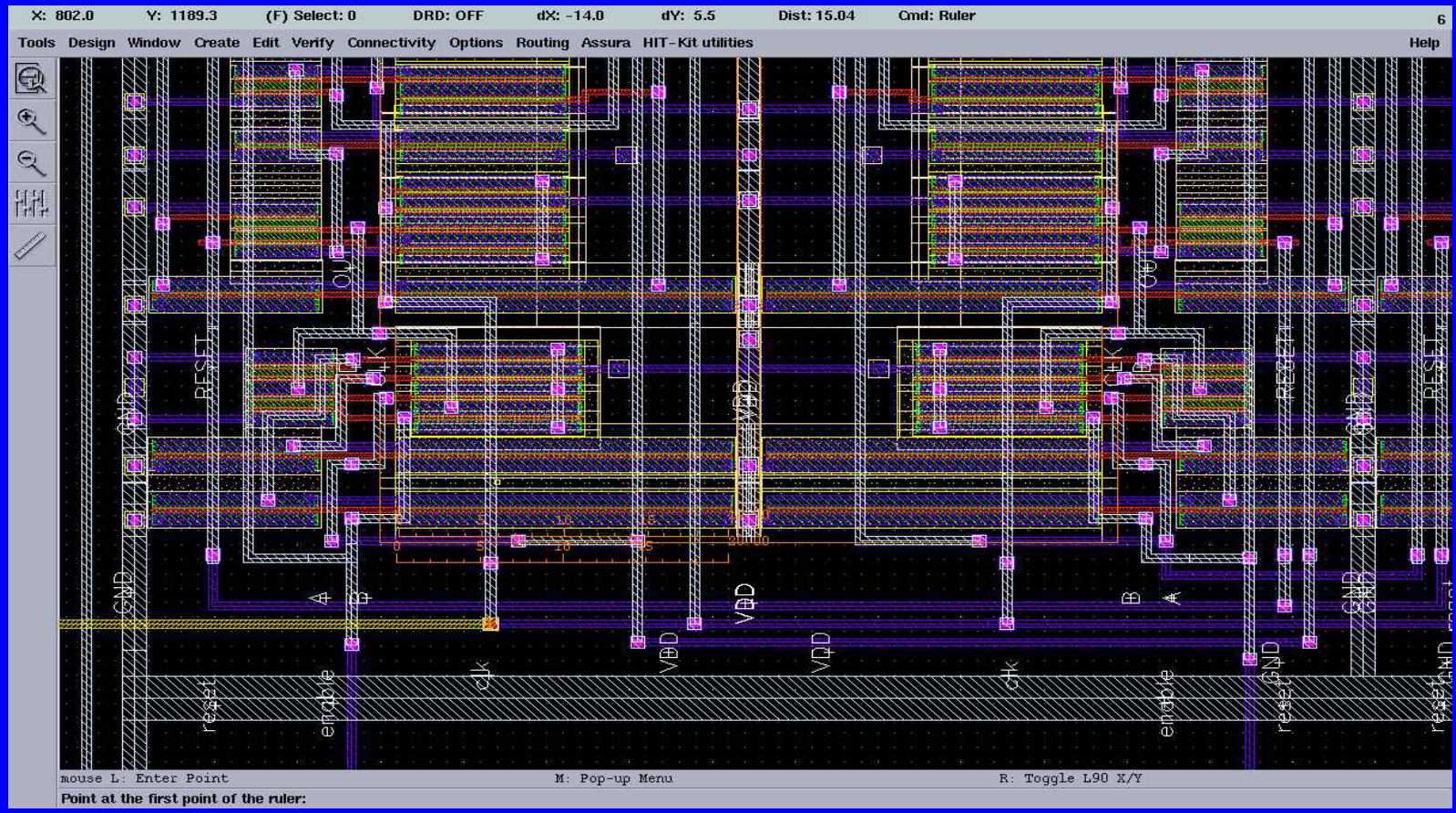
Leaf Cell Layout Considerations

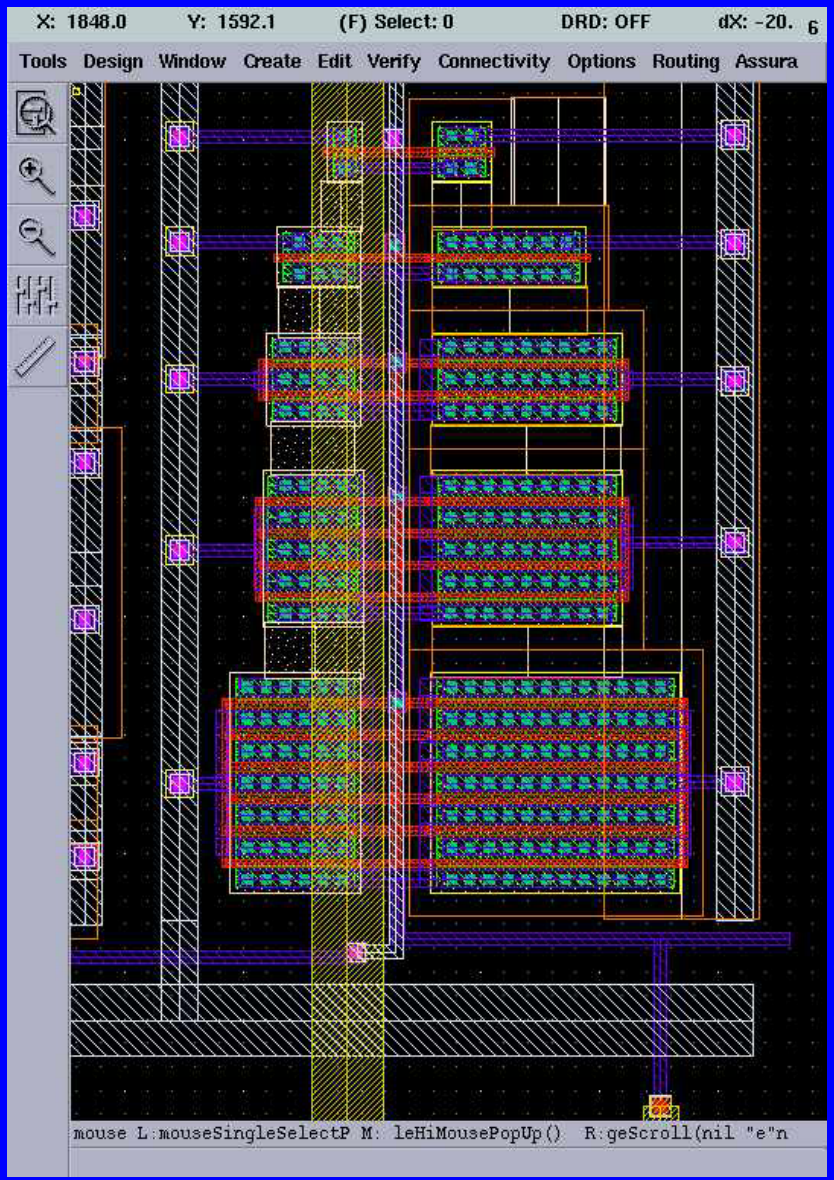
- **For very wide transistors**
  - layout a number of parallel transistors
    - Instance an vector of transistors in the schematic
    - Copy to an array is an efficient way to create many transistors
  - Each transistor should not be wider then 10 μm (15 μm)
  - Share source and drain regions if possible

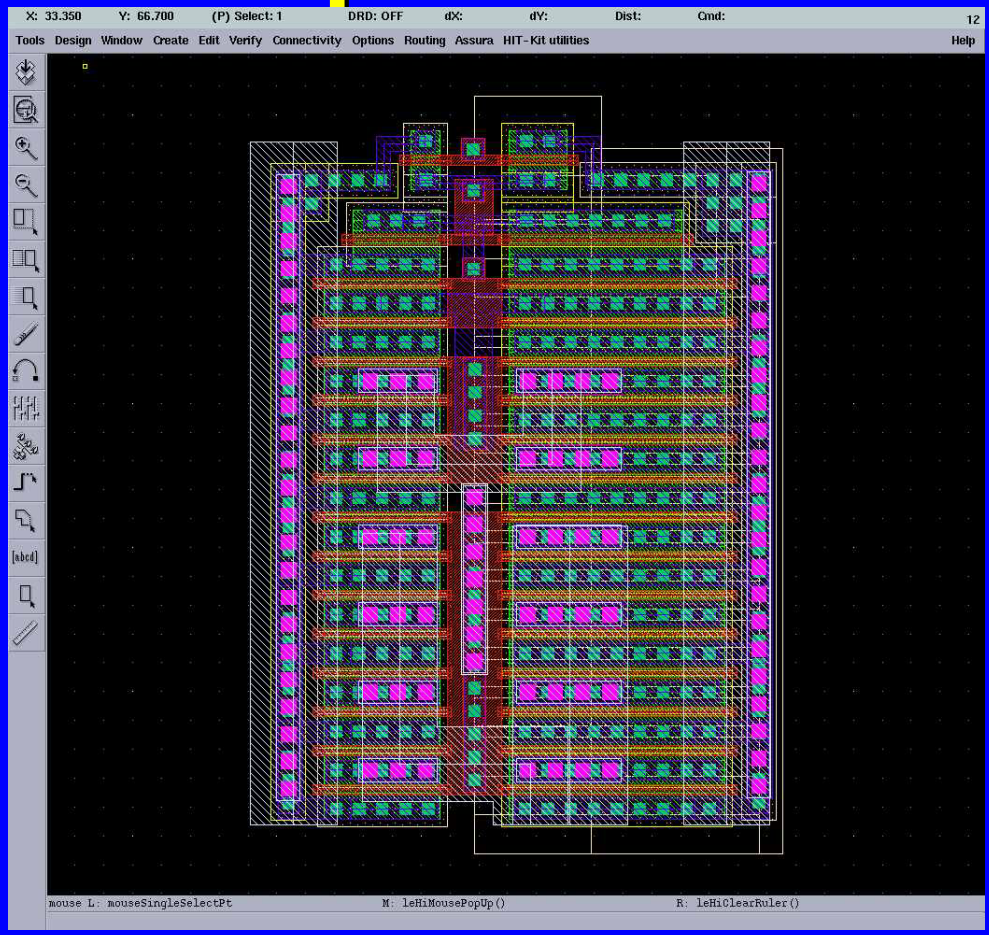
Student Chip Example



- The 20 μm wide transistor will cause sparse layout
- Poly resistivity is typ, 11 Ω/square => 600 Ω to the far end of the gate

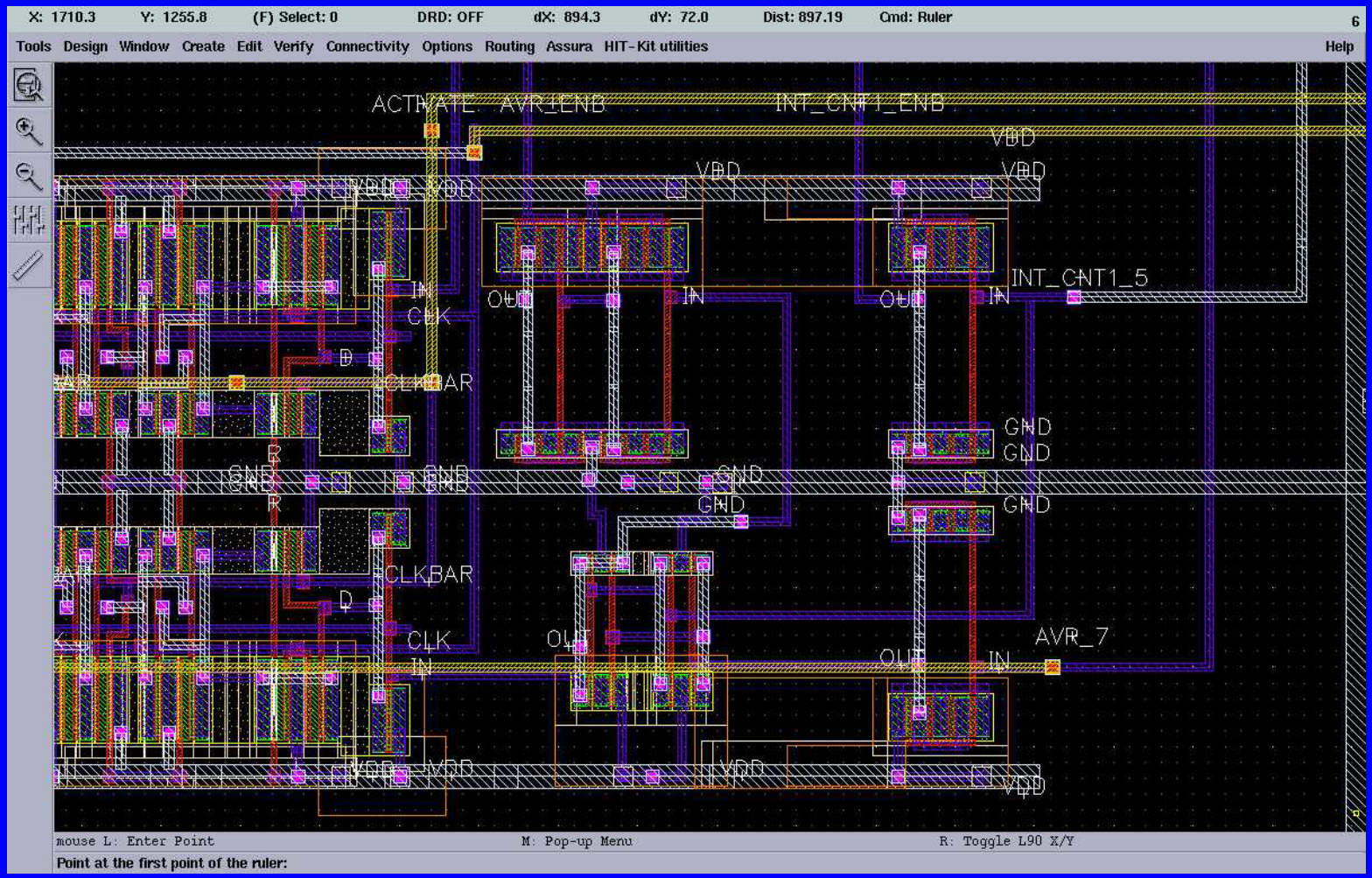
Driver Example





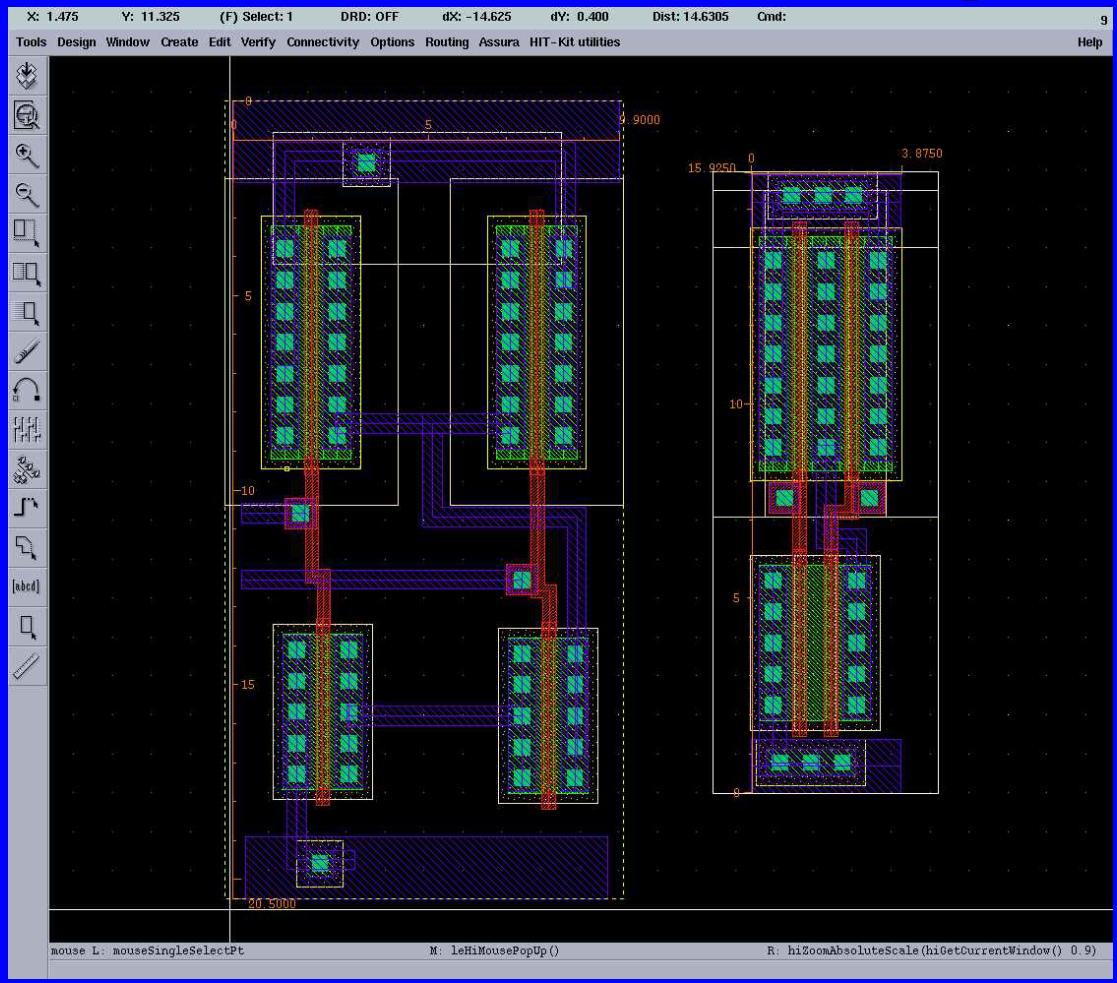
- Narrower transistors will result in denser layout
- Use the same finger size for different transistors and you will very often be a able to share drain/source contacts
- Substrate contacts are you friends! Use them!

Student Chip Example2



- This layout is not even close to dense!

NAND Gate Example



- Size of the left NAND gate: 200 μm^2
- Size of right NAND gate: 60 μm^2

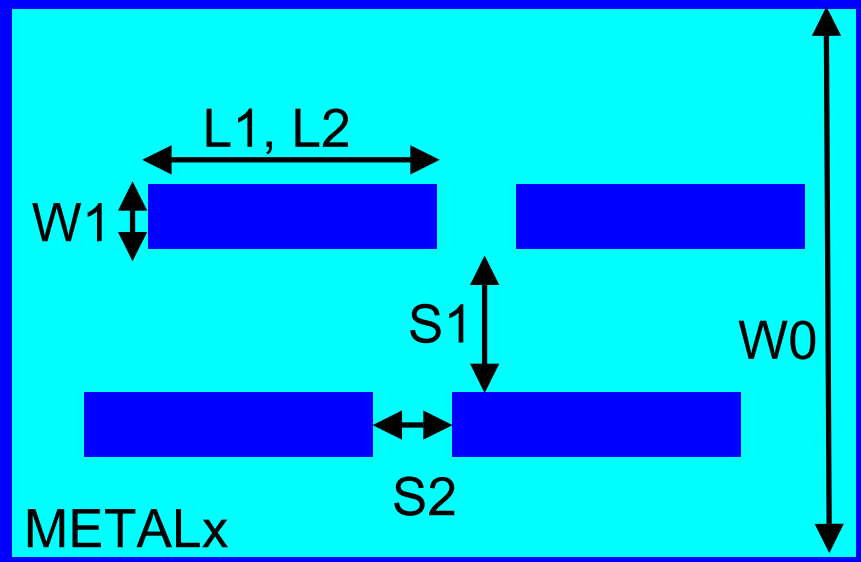
Current Density

- Too high current density will cause electromigration (transport of metal ions)
- Keep RMS current below 0.6 mA to 1 mA per μm interconnect width
- Peak current should be below 30 mA
- Metal wires > 30 μm have to be slotted
- There are FOUR metal layers – use all of them
  - Gate Poly: 11Ω/sq
  - Metal1-3: 70 mΩ/sq (typ), 120 mΩ/sq (max)
  - Metal4: 40 mΩ/sq (typ), 100 mΩ/sq (max)

Metal Slots

- Large areas of metal can cause layer separation around stress-sensitive die corners (stress-levels “frozen” into die during manufacturing)
- Solution: Introduce slots along direction of current flow in wide metals
- AMS 0.35μm slot rules:

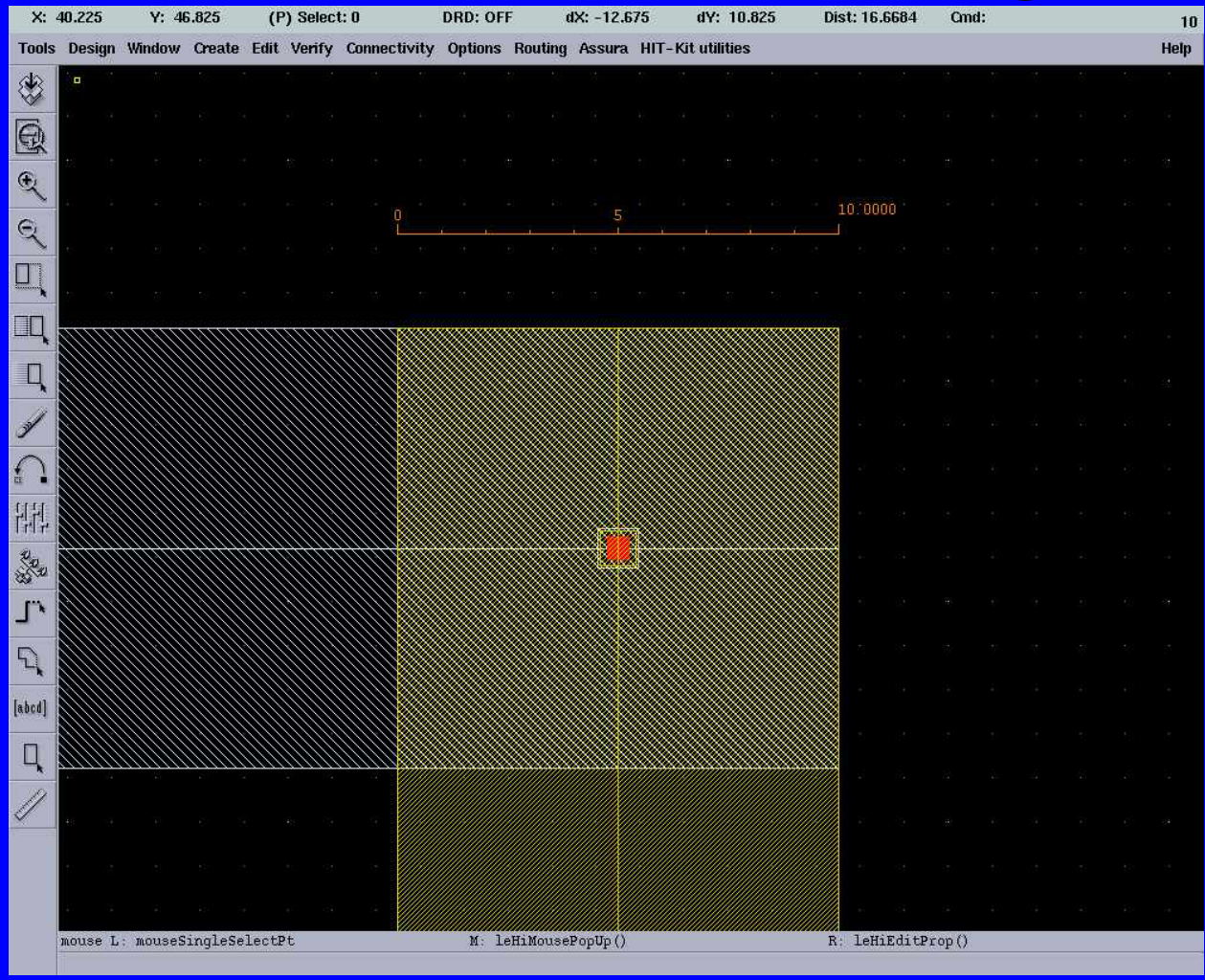
Rule	Description	Value [μm]
W0	Max. METALx width without slots	35
W1	Fixed slot width	3
L1	Min. slot length	30
L2	Max. slot lenght	300
S1	Min. spacing for parallel slots	10
S2	Min. spacing for slots in sequence	10



Contact Resistance

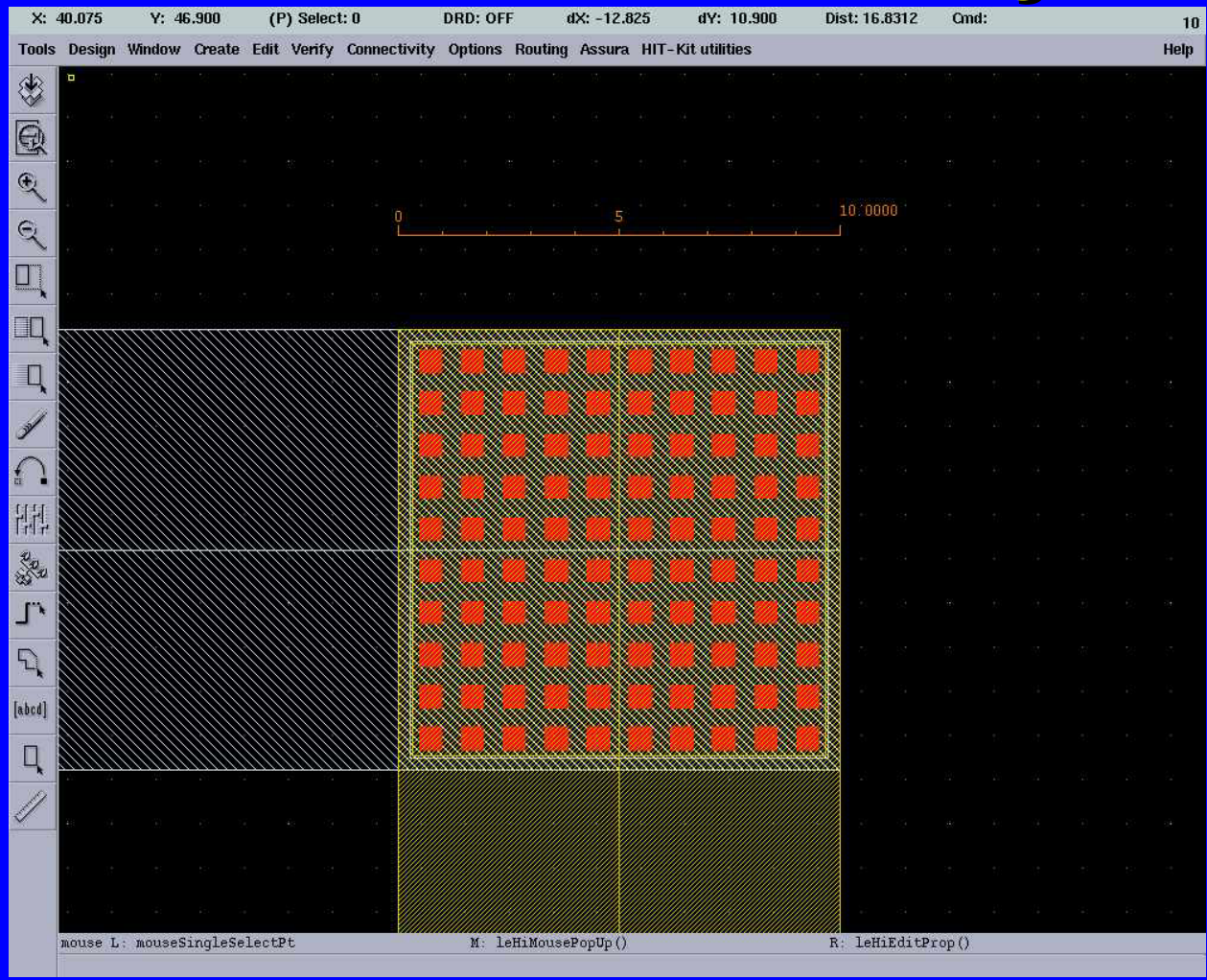
- **Contact resistances**
  - Met1 – Ndiff: typ. 30 Ω max 100 Ω
  - Met1 – Pdiff: typ. 60 Ω max 150 Ω
  - Met1 – Poly: typ. 2 Ω max 10 Ω
- **Via resistance**
  - Typ 1.2 Ω max 3 Ω

Via Current Density



If you increase metal wire width to keep current density low. Think about current density in vias

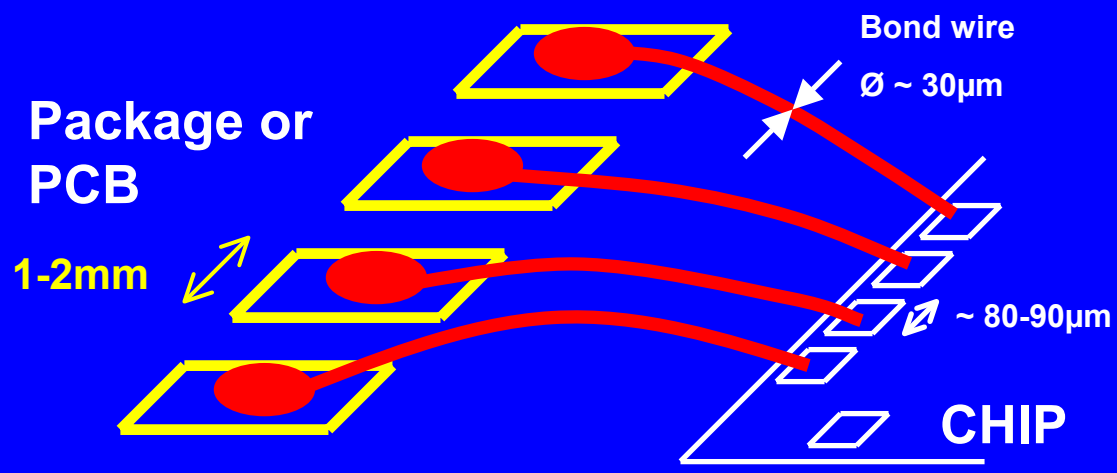
Via Current Density



Adding extra vias will not cost you anything extra!

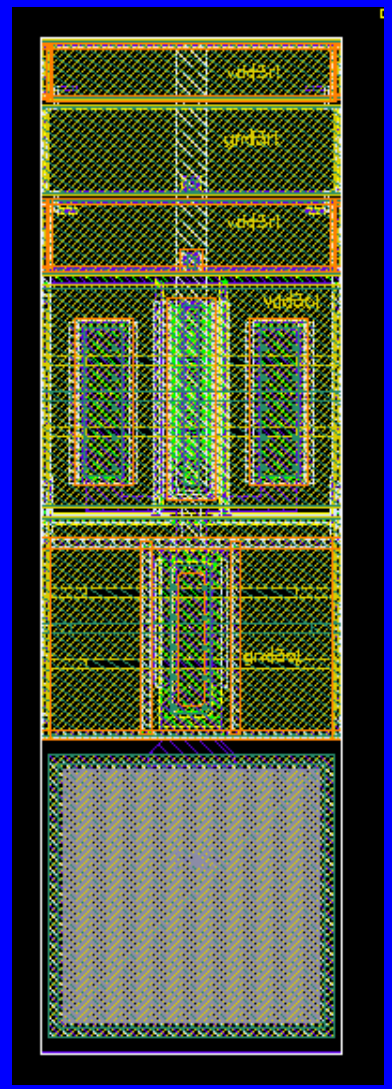
Bond Pads

- Are used to connect your chip to the outside world
- Critical part of the chip assembly
- The type of PAD depends on the signal
- The PADs are usually provided by the chip vendor
- In the lab library there is a few PADs specified



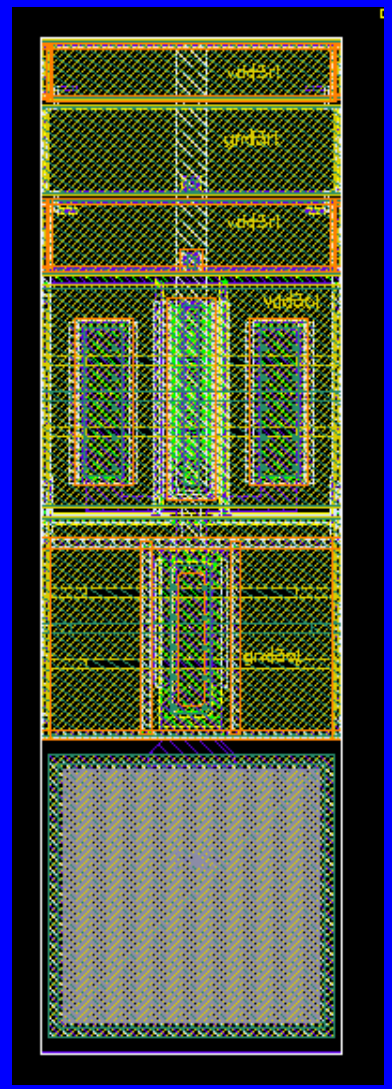
PADs Included in Lab Library

- **APRIOP**
  - Analog Input/Output PAD
  - ESD protection included
  - Signal accessed in metal 2 on core-side of the PAD
  - Padcap ~1.2pF



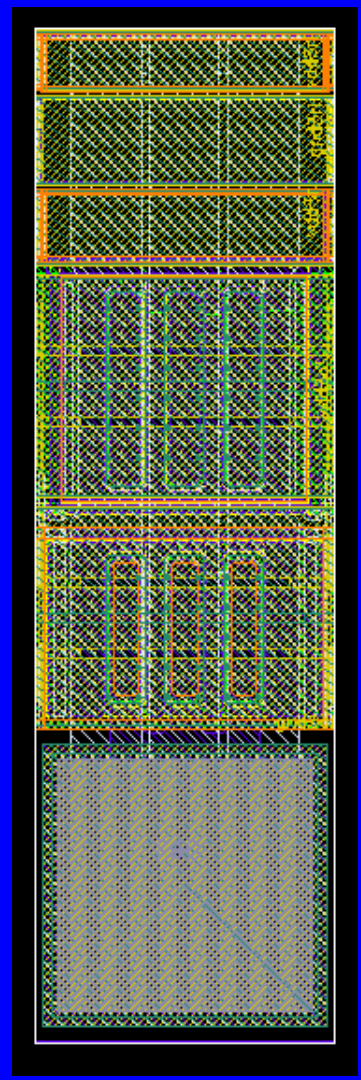
PADs Included in Lab Library

- **AUPRIOP (not yet available)**
  - Analog Input/Output PAD
  - No ESD protection
  - Signal accessed in metal 2 on core-side of the PAD
  - Suitable for high-speed I/O and power supply with different voltage than core



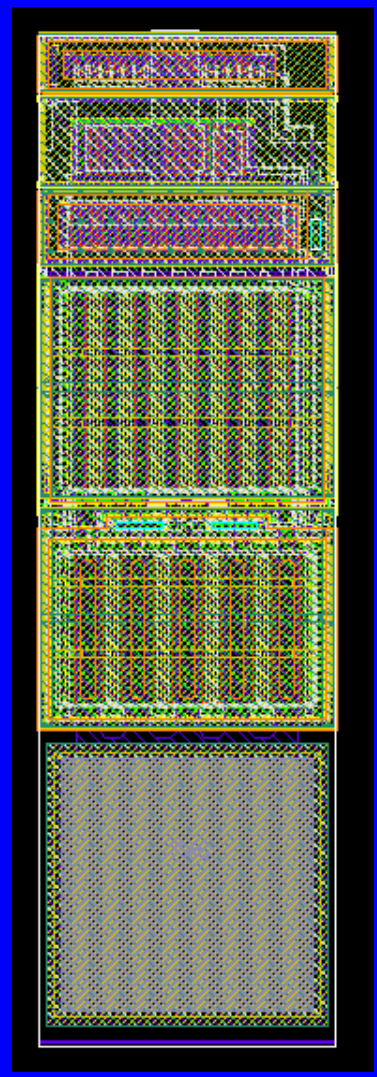
PADs Included in Lab Library

- **APRIOWP**
  - Analog Input/Output PAD
  - ESD protection included
  - Signal accessed in metal 2 on core-side of the PAD
  - Wide metal 2 from PAD to core
  - Padcap ~5pF



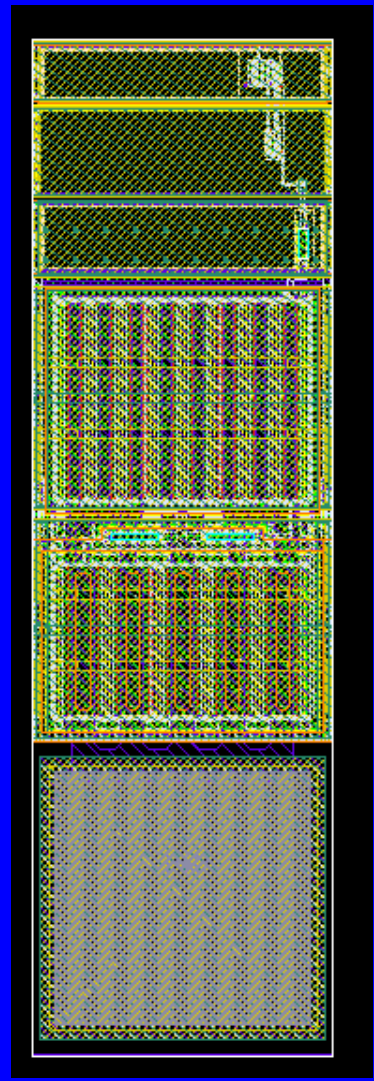
PADs Included in Lab Library

- **CLK_BUFF**
  - Clock input PAD
  - Include ESD and buffers



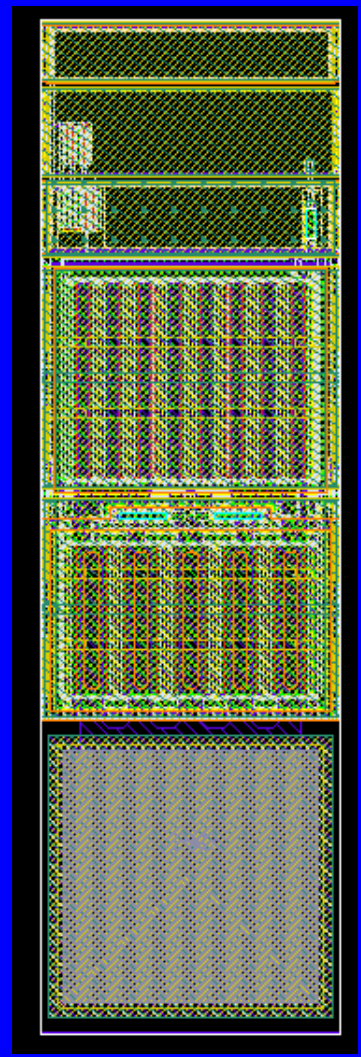
PADs Included in Lab Library

- **INPUTPAD**
  - Slow input signal PAD
  - Includes a small driver
  - ESD protection also included



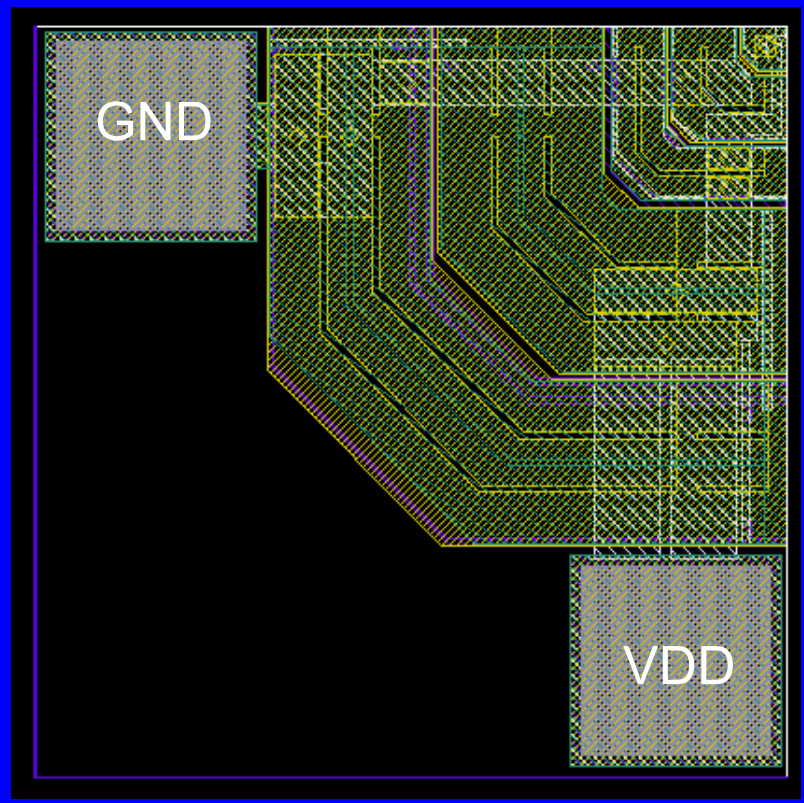
PADs Included in Lab Library

- **OUTPUTPAD**
  - Slow output signal PAD
  - Includes a driver with 8mA current drive strength
  - ESD protection included



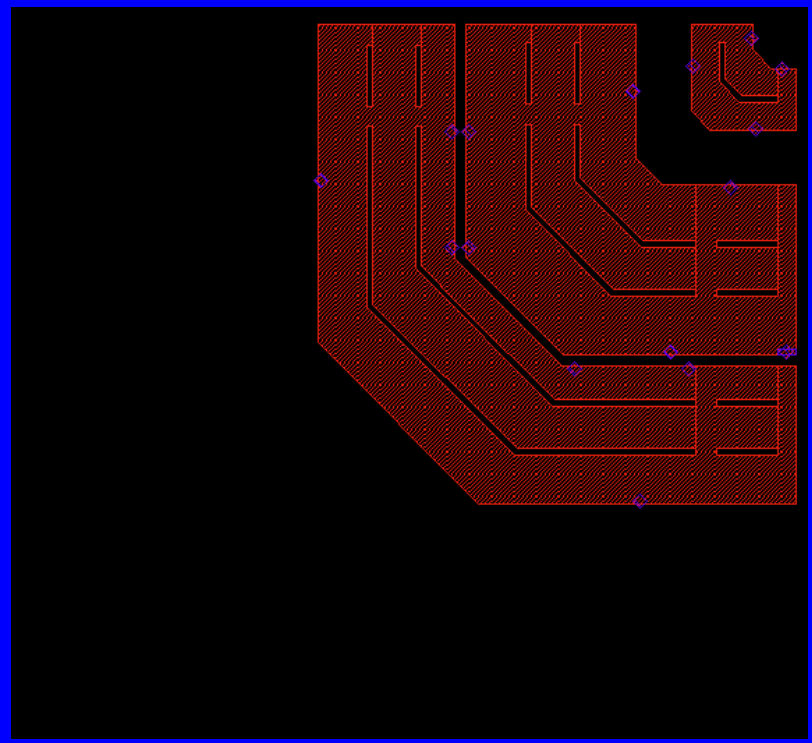
PADs Included in Lab Library

- **VDDGNDCORNER**
  - Default power supply PAD for this course
  - Provides supply voltage and ground to the PAD ring and the Core
  - VDD and GND will be accessed on-chip from the PAD-ring



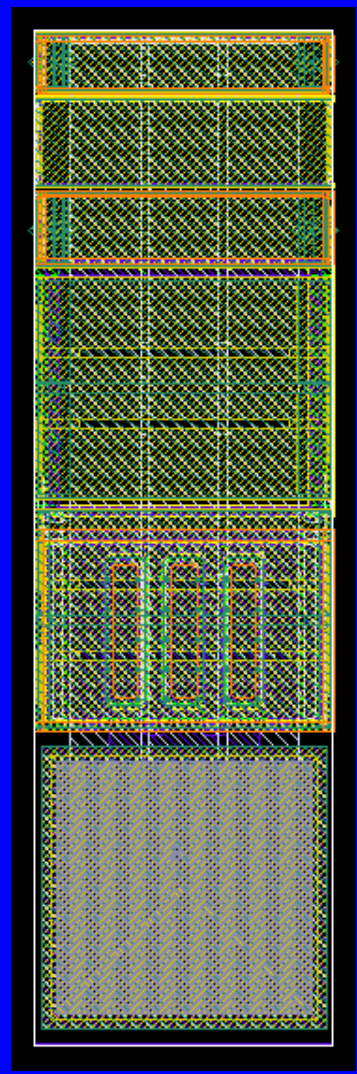
PADs Included in Lab Library

- **CORNERFILL**
  - Fill cell that should be placed under the VDDGNDCORNER pad
  - Increases fill rate in POLY1



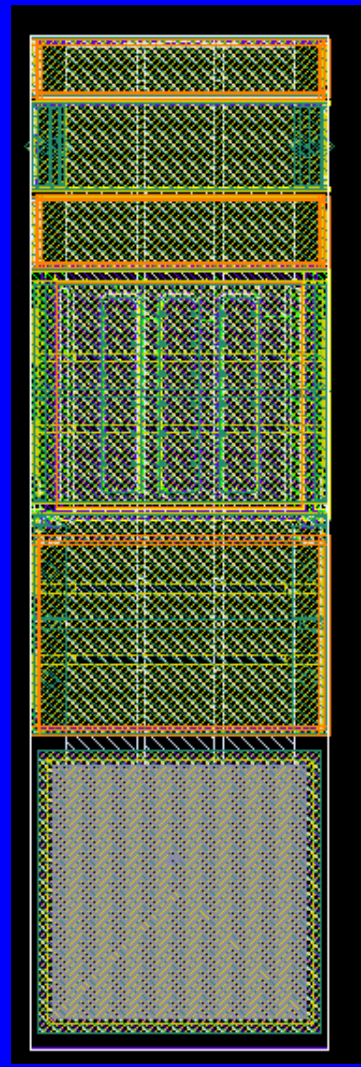
PADs Included in Lab Library

- **VDDPAD**
  - Separate power supply PAD
  - Includes ESD protection
  - Supply to PAD ring and core



PADs Included in Lab Library

- **GNDPAD**
  - Separate ground PAD
  - Includes ESD protection
  - Ground PAD ring and core

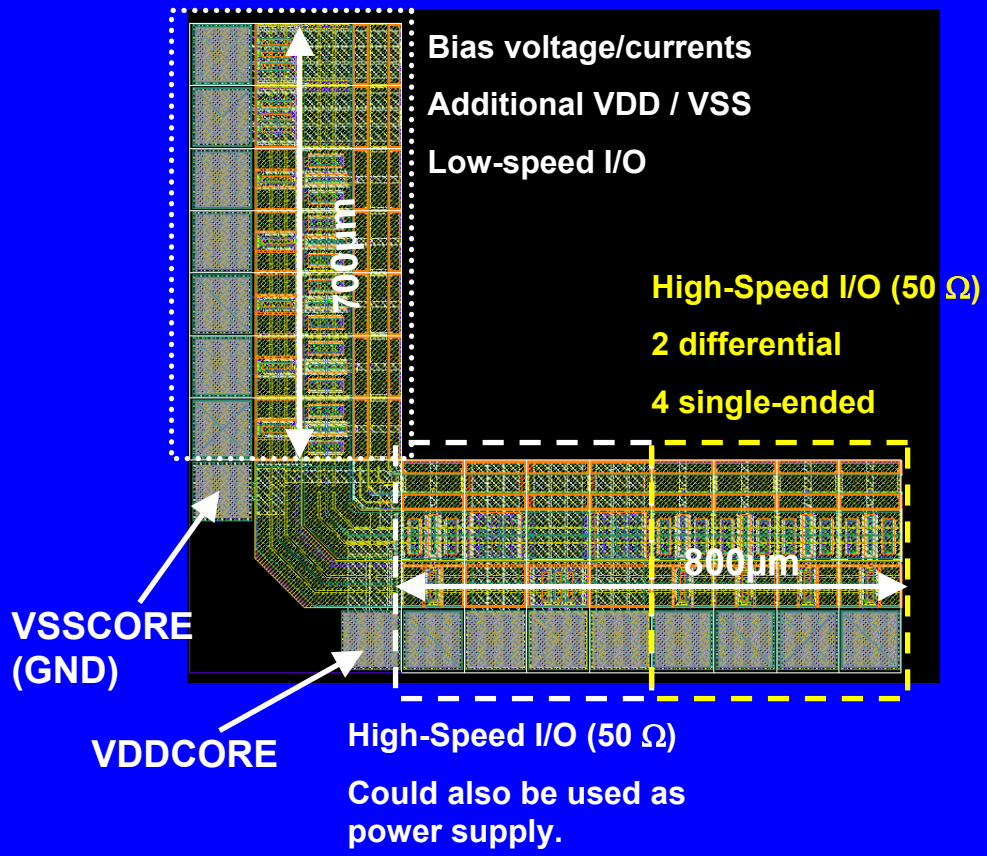


How to Build the PAD Ring

- Maximum amount of PADs is 17
- The 2 PADs in the corner are fixed
- 15 PADs remains for the students to place “freely”

How to Build the PAD Ring

- A generic PCB will be built for the measurements
- Requires that the PAD placement are somewhat restricted



On-Chip Decoupling

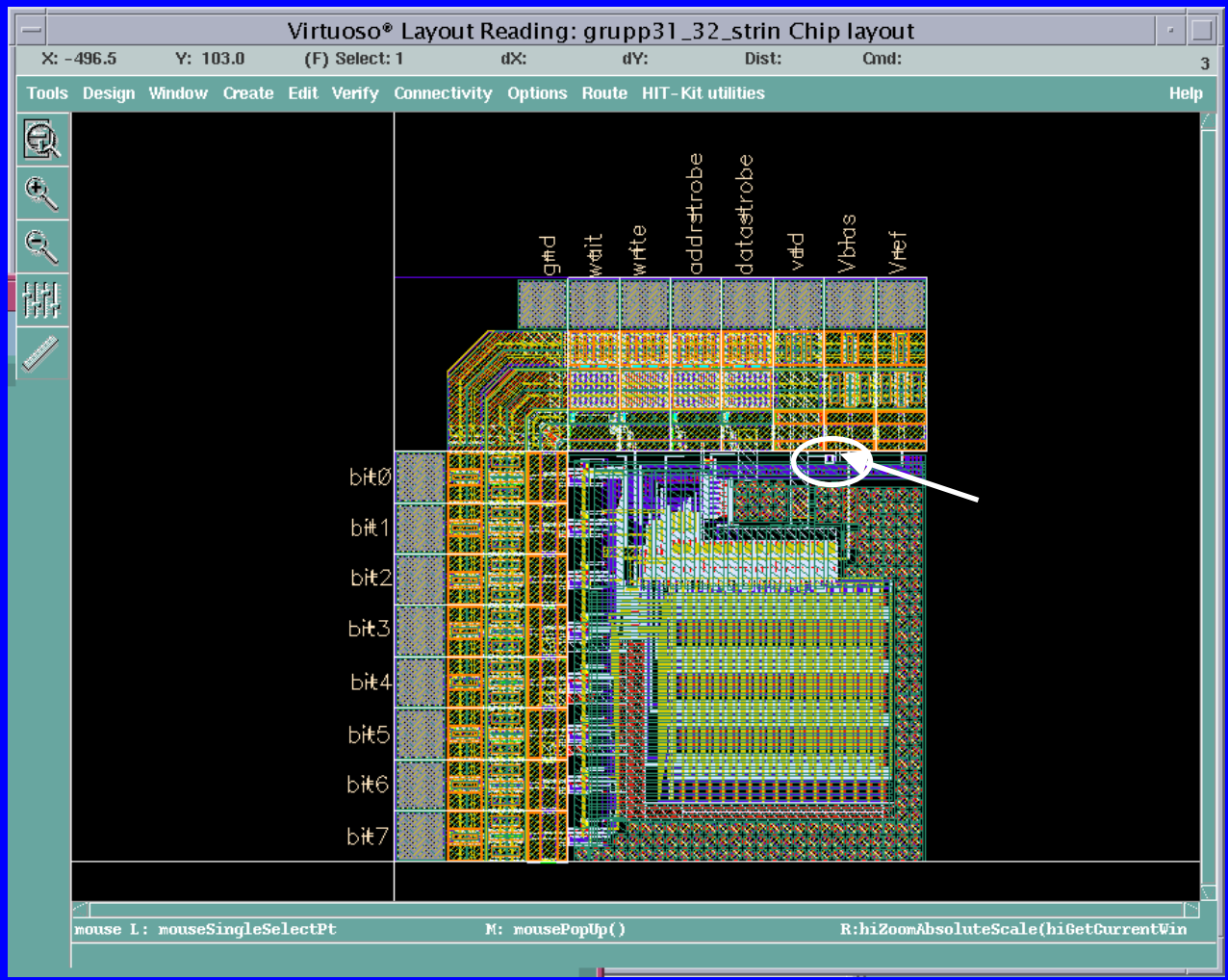
- Every switching draws a current from the power supply
- When many devices switch simultaneously, for example at the clock edges, huge current spikes might be introduced
- This gives voltage fluctuations on-chip that can cause YOUR chip to malfunction
- To filter out these high frequency components on the power supply a large capacitance between VDD and GND is used

On-Chip Decoupling

- **Capacitors for decoupling:**
  - Poly-poly capacitor, cpoly ~0.8fF/um^2
  - Gate-cap, use a transistor as a decoupling capacitor. Example: NMOS with the gate connected to VDD and Drain&Source grounded
  - Gate-cap gives more capacitance per area, ~4.5fF/um^2
- **Use decoupling for all DC-voltages**
- **How much decoupling is needed?**
  - Depends on the switching activity
  - Depends on how sensitive your design is to power supply fluctuations

Common Layout Mistakes

Too small decoupling capacitor!
ONE is NOT enough!



How to Connect Your Design to the Padframe

- Digital input/output pads have internal buffers. YOU have to make sure these buffers are powerful enough for your design
- Do you need a driver in order to drive the driver included in the I/O pad?
- You can also design your own pad driver and use an analog pad
- If you have an external clock, make sure to use an appropriate clock buffer
- Analog inputs/outputs should use the analog pads without buffers
- Use VDD/GND pads for VDD and GND

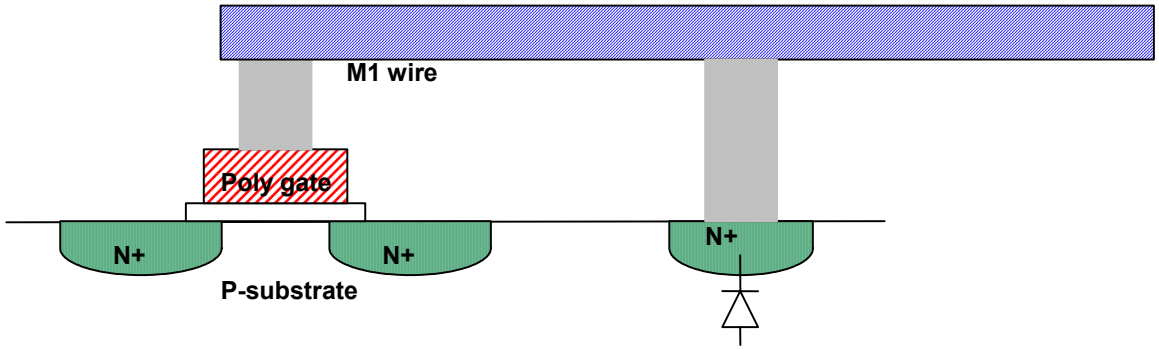
Available Components from PRIMLIB

- 3.3V NMOS/PMOS
- 5V NMOS/PMOS
- Poly1-Poly2 capacitors (cpoly)
- High-resistive poly resistor (rpolyh)
- Low-resistive poly resistor (rpoly1 and rpoly2)
- Nwell resistor (rnwell)
- There are other components as well in PRIMLIB that can be used. Discuss with your supervisor before using them!

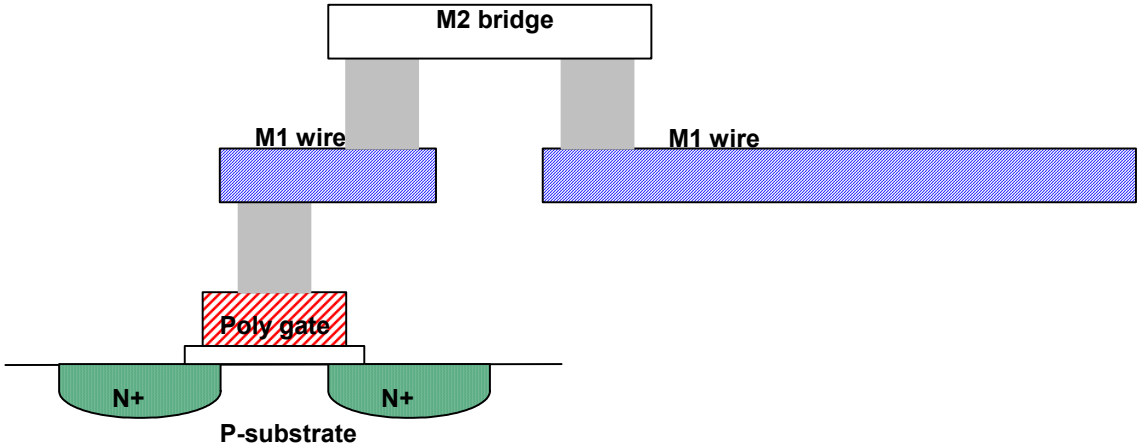
Antenna Errors

- Antenna errors occur when a large metal structure is connected to a gate. When the metal is etched in the fabrication a large amount of charged might be induced in the metal. This can cause the gate to break if there is no discharging path for high voltages (like a drain/source or a reversed diode)
- Antenna errors can be fixed by adding a reversed diode connected to the metal wire causing the problem. An N+ doped nwell contact will function as a reversed diode if connected to the substrate. Another way to solve antenna errors is to build a bridge in higher or lower layers, and thereby break the long metal wire connected to the gate

Antenna Errors



Long metal wire with reversed diode to substrate.



Long metal wire broken up by a bridge in higher or lower layers

How to Organize the TOP-LEVEL Layout

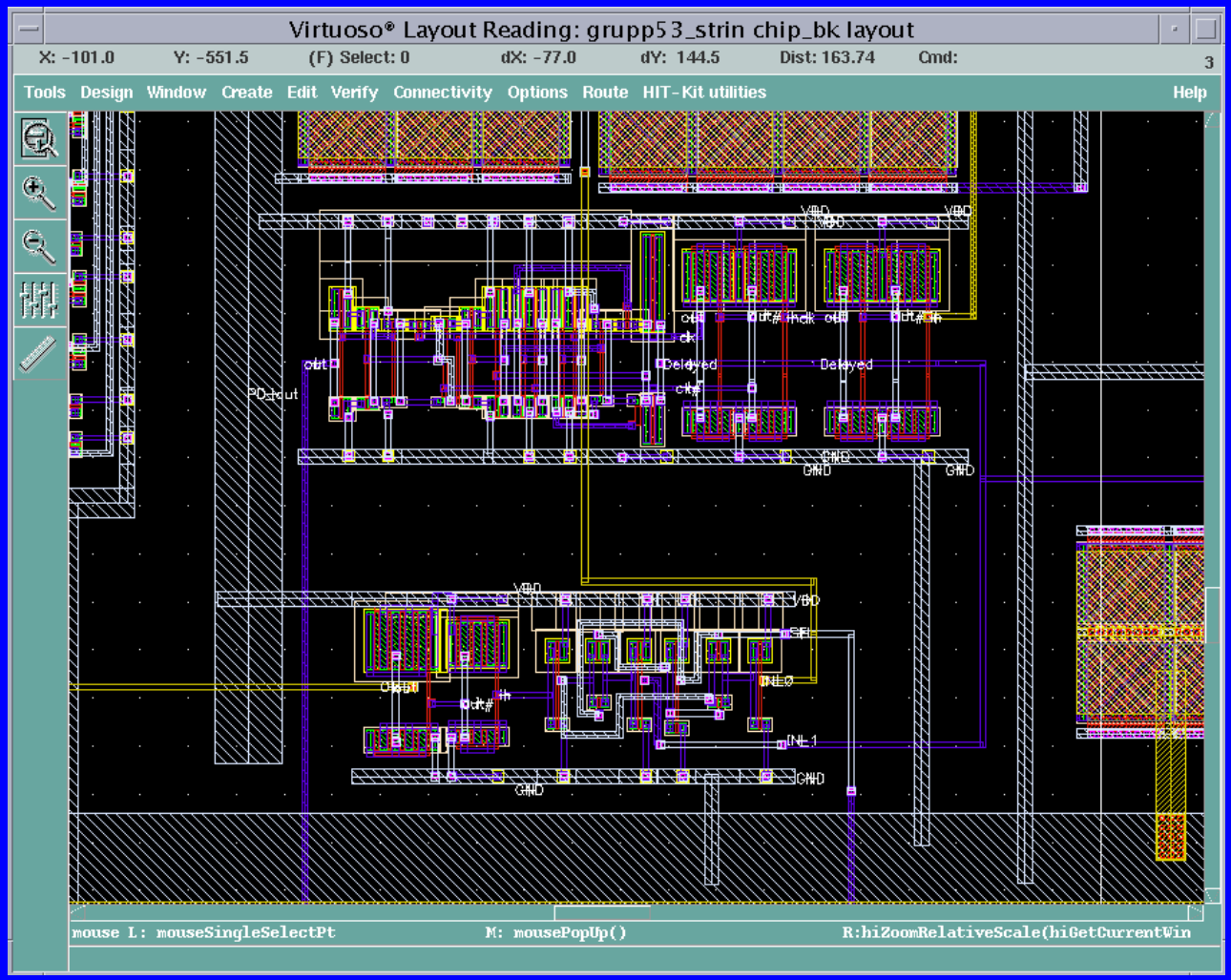
- **Your Top-Level layout should consist of the following instances:**
  - Pad frame
  - The core of your design
  - Fillpattern (up to Met3)
  - Topmet fill
  - FIMP and NLDD
- **Fill can be created by using scripts**
- **To avoid fill at certain places, add a blocking layer**

How to Organize the TOP-LEVEL Layout

- **At the top level**
  - Always make sure all the instances have the same origin, preferably (0,0)
  - If you accidentally move one cell you can easily put it back on the right place
- **Use the command "Edit in Place" if necessary, but be careful. Make sure you are doing your changes in the correct cell**

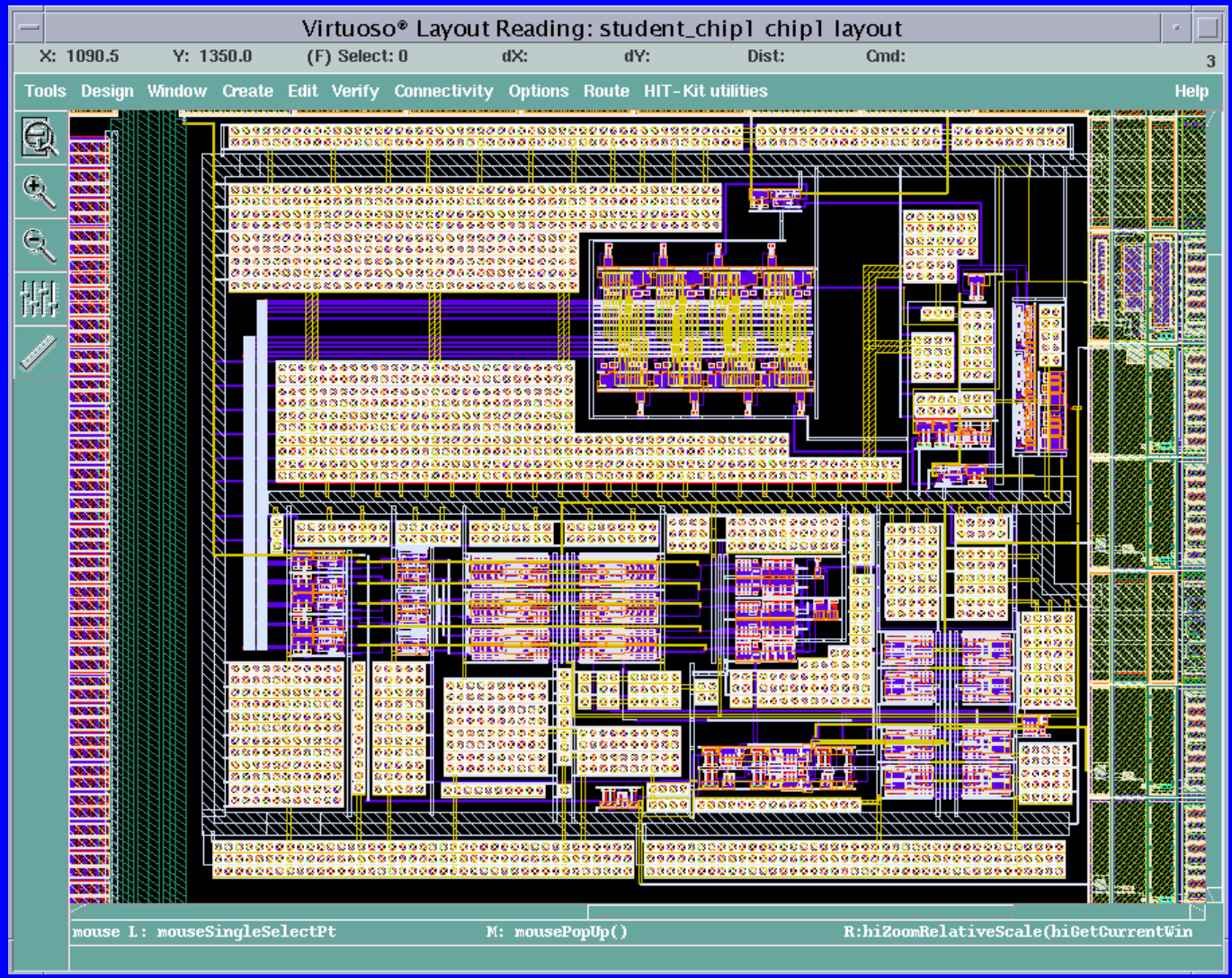
Common Layout Mistakes

Build dense layouts instead of like this one!



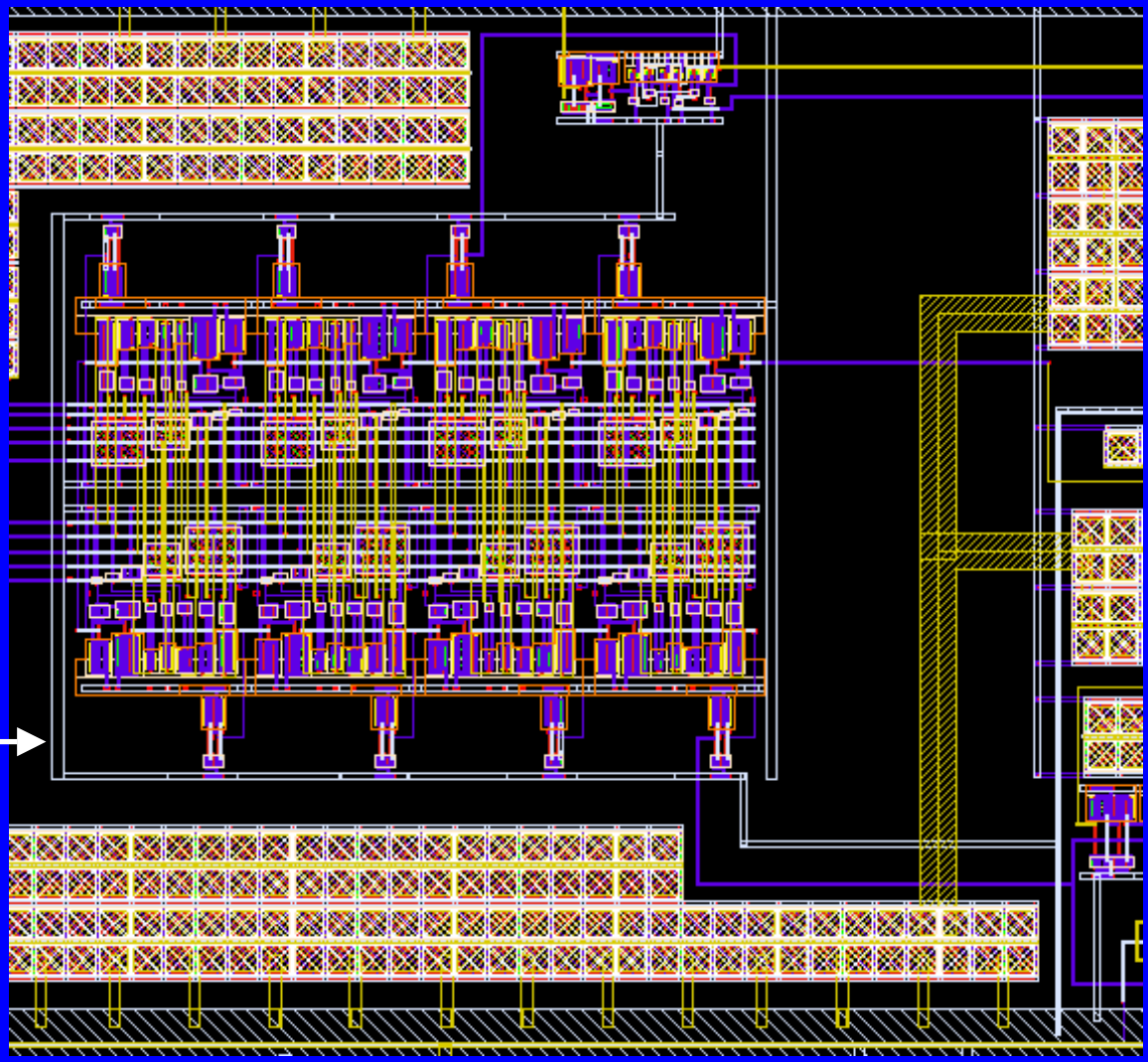
Common Layout Mistakes

Dense layouts to reduce the length of wires!



Common Layout Mistakes

Power grid!



Chip Verification Flow (1)

1. DIVA DRC and LVS of local cells
2. DIVA DRC and LVS of complex cells
3. ASSURA DRC and LVS of padframe
4. ASSURA DRC and LVS of chip topcell
   (chip core, padframe, decoupling capacitors)
   Take care of Antenna errors
5. Simulate chip topcell
   (only extracted capacitances)
6. Stream out a GDSII file
7. Stream in the GDSII file to a NEW library
8. LVS of streamed in chip top cell
   (compare streamed in layout and original schematic)

Chip Verification Flow (2)

9. **Generate Metal Fill**
   to avoid over- and under etching
10. **Generate FIMP (Field Implant) layer**
    to avoid weak parasitic transistors under poly interconnects
11. **Generate NLDD (N Lightly Doped Drain) layer**
    for transistor channel engineering purposes
12. **ASSURA DRC and LVS of chip topcell**
    (chip core, padframe, decoupling capacitors, Metal Fill, FIMP, NLDD)
13. **Stream out a GDSII file**
14. **Stream in the GDSII file to a NEW library**
15. **LVS of streamed in chip top cell**
    (compare streamed in layout and original schematic)

Stream-In to NEW library!

- Use
  File>New>Library

  to create a NEW stream-in library!
  This automatically sets library pointers correctly

- Example mistake:

  Edit > Library Path…

  Entered new stream-in library name with pointer to original design library!!

  OVERWROTE THE COMPLETE DESIGN!