TSEK03: Radio Frequency Integrated Circuits (RFIC)

Lecture 3b & 4: LNA

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LNA: Overview

- Razavi: Chapter 5, pp. 259-295, 318-322.
- Lee: Chapter 11, pp. 334-362.

- **5.1 LNA intro: NF, gain, return loss, stability, linearity**
- 5.2 Input matching
- 5.3 LNA topologies (selected)

5.1 Low-Noise Amplifier

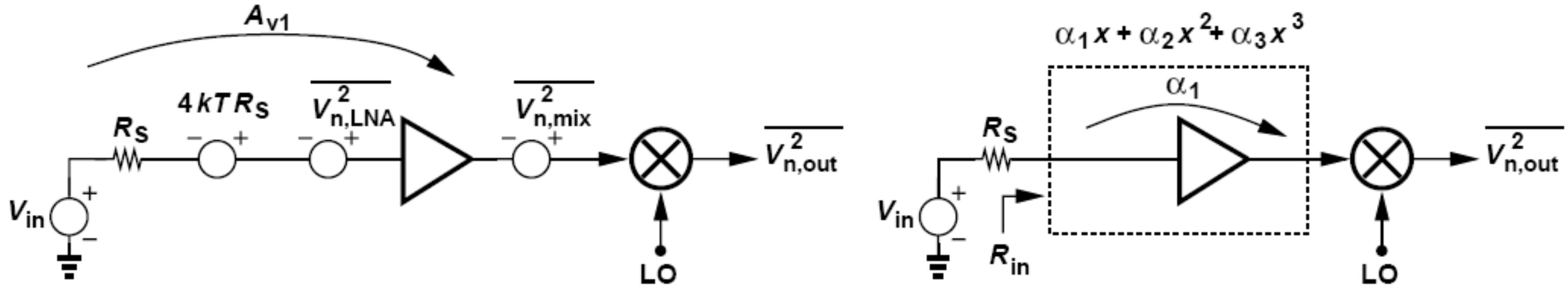
- The first stage of a receiver is usually a low-noise amplifier (LNA). The noise figure of the LNA directly adds to that of the receiver.
- It amplifies a weak signal (has gain) and should add as little as possible noise to this weak signal (NF about 2-3 dB is expected).
- Input matching (i.e., 50 Ω input impedance) is necessary, specially when a filter precedes the LNA.
- Trade-offs between gain, input impedance, noise figure, and power consumption should be considered carefully.
- In this section: NF, gain, input return loss, stability, linearity, bandwidth, power dissipation are discussed.

General considerations: Gain

- The gain of the LNA must be large enough to minimize the noise contribution of subsequent stages, specifically, the downconversion mixer(s).
- Usually leads to a compromise between the noise figure and the linearity of the receiver.
- The noise and IP3 of the stage following the LNA are divided by different LNA gains.
- (Modern design often have not matching between LNA and mixer, therefore voltage gains are easier to use.)

LNA: Gain

- LNA+mixer:



$$\mathrm{NF_{tot}} = \frac{A_{v1}^2(\overline{V_{n,LNA}^2} + 4kTR_S) + \overline{V_{n,mix}^2}}{A_{v1}^2} \frac{1}{4kTR_S}$$

$$= \mathrm{NF_{LNA}} + \frac{\overline{V_{n,mix}^2}}{A_{v1}^2} \cdot \frac{1}{4kTR_S}.$$

$$\frac{1}{\mathrm{IP}_{3,\mathrm{tot}}^2} = \frac{1}{\mathrm{IP}_{3,\mathrm{LNA}}^2} + \frac{\alpha_1^2}{\mathrm{IP}_{3,\mathrm{mixer}}^2}$$

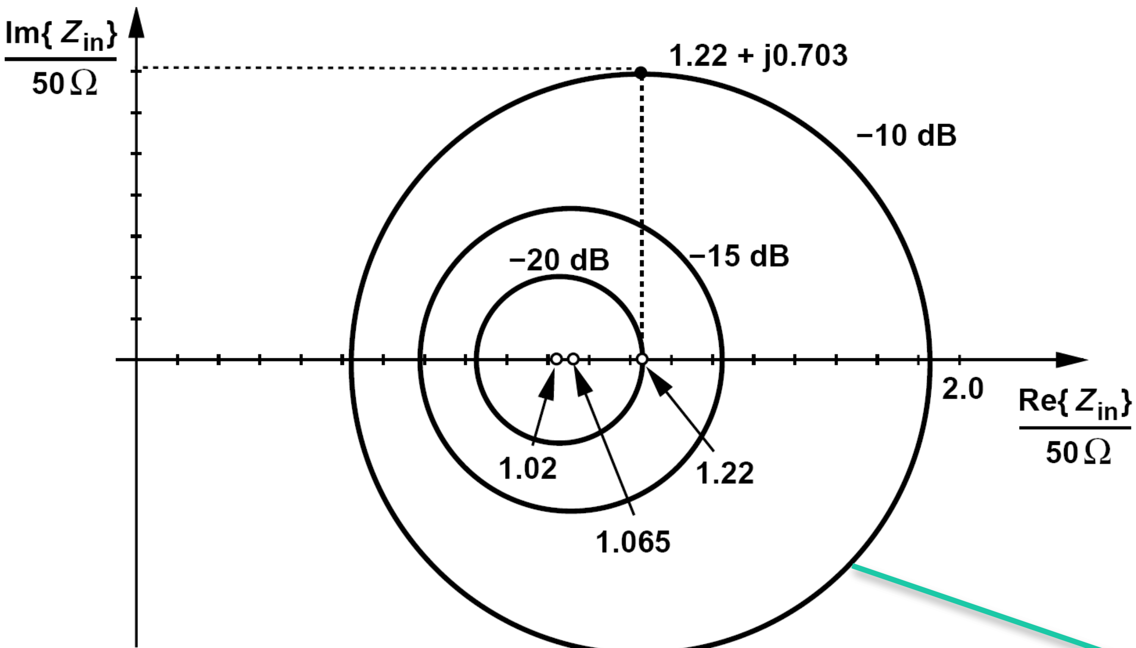
General considerations: Input Return Loss

- Input matching of the LNA is required to transfer the maximum power from antenna to the LNA if there is no filter between. If there is a filter, this matching is a must to keep the characteristics of filter.
- The quality of the input match is expressed by the input "return loss", defined as the reflected power divided by the incident power. For a source impedance of R_S, the return loss is given by:

$$\Gamma = \left| \frac{Z_{in} - R_S}{Z_{in} + R_S} \right|^2$$

General considerations: Input Return Loss

- Figure below plots contours of constant Γ in the Zin plane. Each contour is a circle with its center shown.



Input return loss

$$\Gamma = \left| \frac{Z_{in} - R_S}{Z_{in} + R_S} \right|^2$$

< -10 dB (<10 %) is usually acceptable

constant Γ

General considerations: Stability

- Oscillations leads to high non-linearity and "strange" behavior.
- Stability of an RF circuit can be checked by Stern (Rollett) stability factor which is based on s-parameters:

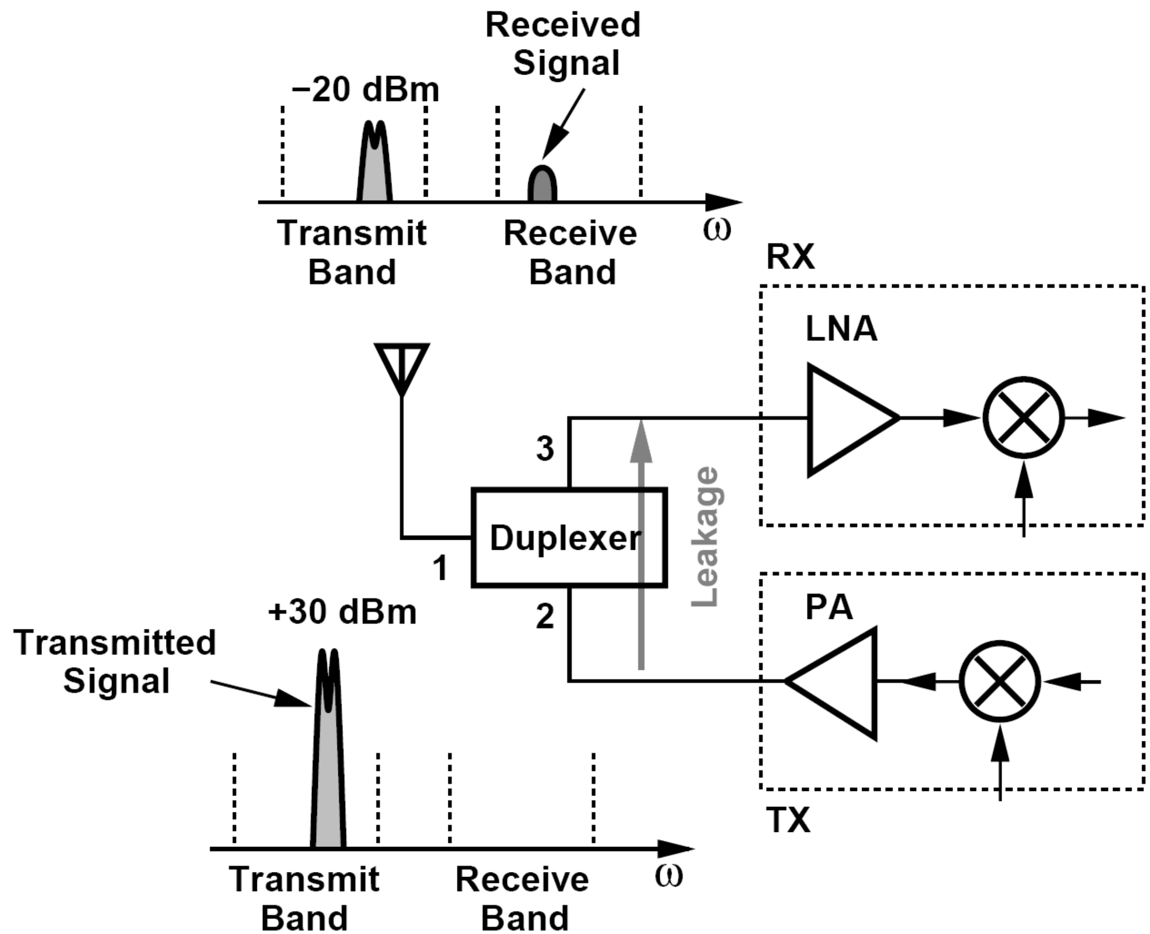
$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} \qquad K > 1$$

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}| \qquad |\Delta| < 1$$

- If K > 1 and Δ < 1, then the circuit is unconditionally stable for any combination of input and output impedances.

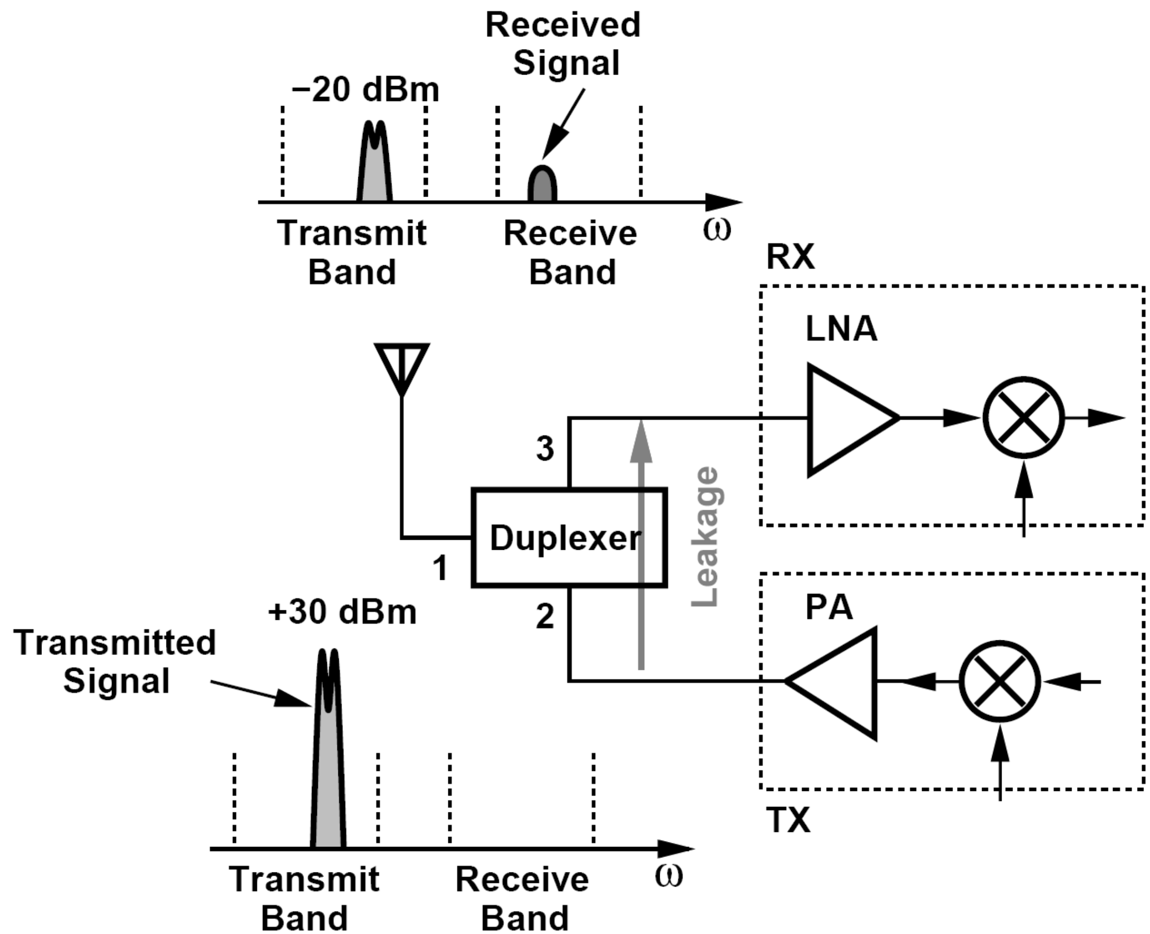
General considerations: Linearity

- In most applications, the LNA does not limit the linearity of the receiver.
- An exception to the above rule arises in "full-duplex" systems:



General considerations: Linearity

- Leakages through the filter and the package yield a finite isolation between ports 2 and 3 as characterized by an S_{32} of about -50 dB. The received signal may be overwhelmed.

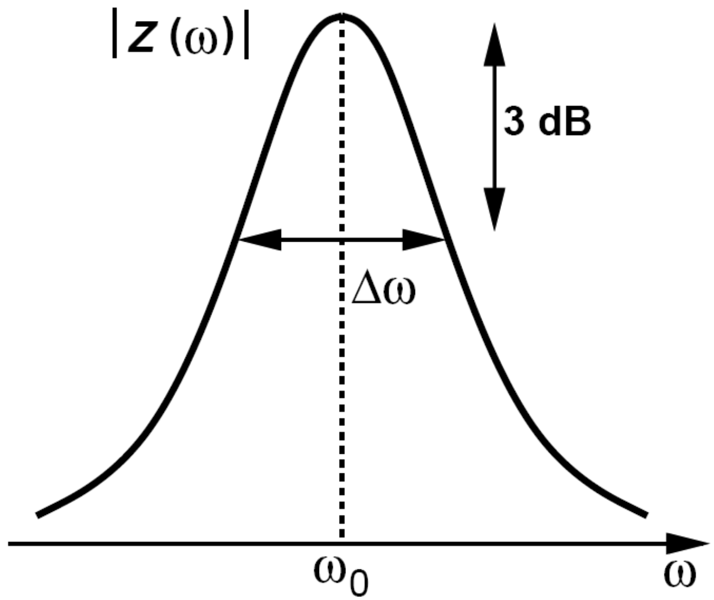


General considerations: Bandwidth

- The LNA must provide a relatively flat response for the frequency range of interest, preferably with less than 1 dB of gain variation. The LNA -3-dB bandwidth must therefore be substantially larger than the actual band so that the roll-off at the edges remains below 1 dB.
- “Fractional bandwidth” defined as the total -3-dB bandwidth divided by the center frequency of the band.

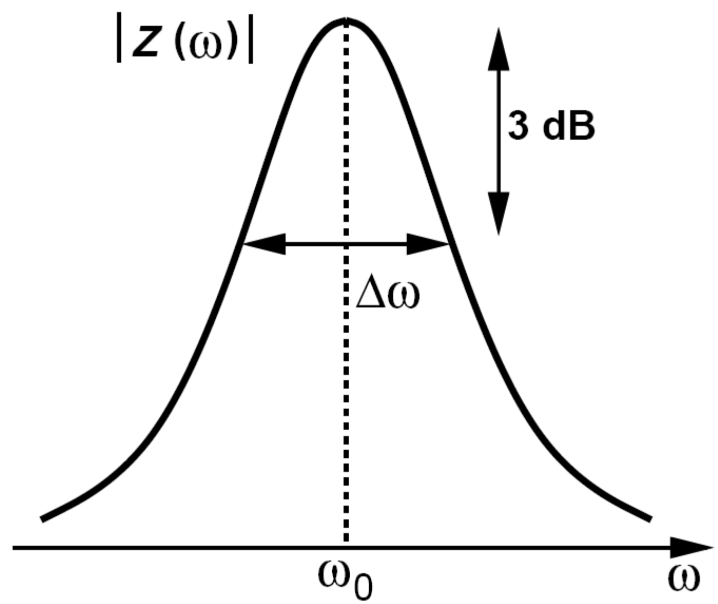
Example 5.3

- An 802.11a LNA must achieve a -3-dB bandwidth from 5 GHz to 6 GHz. If the LNA incorporates a second-order LC tank as its load, what is the maximum allowable tank Q?



Example 5.3

- As illustrated in figure below, the fractional bandwidth of an LC tank is equal to $\Delta\omega/\omega_0 = 1/Q$. Thus, the Q of the tank must remain less than 5.5 GHz/1 GHz = 5.5.



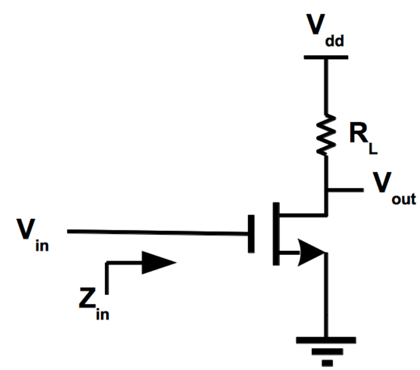
LNA Power Dissipation

- The LNA typically exhibits a direct trade-off among noise, linearity, and power dissipation.
- In most receiver designs, the LNA consumes only a small fraction of the overall power.
- Conclusion: the LNAs noise figure generally proves much more critical than its power dissipation.

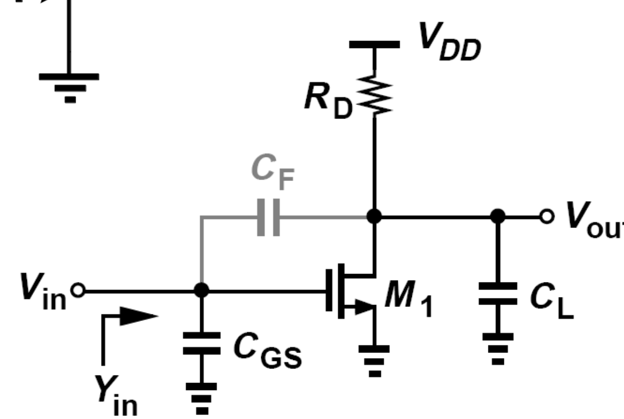
5.2 Input Matching

- LNAs are typically designed to provide a 50-Ω input resistance and negligible input reactance. This requirement limits the choice of LNA topologies.
- Generic amplifier

$$Z_{in} = Re\{Z_{in}\} + Im\{Z_{in}\}$$

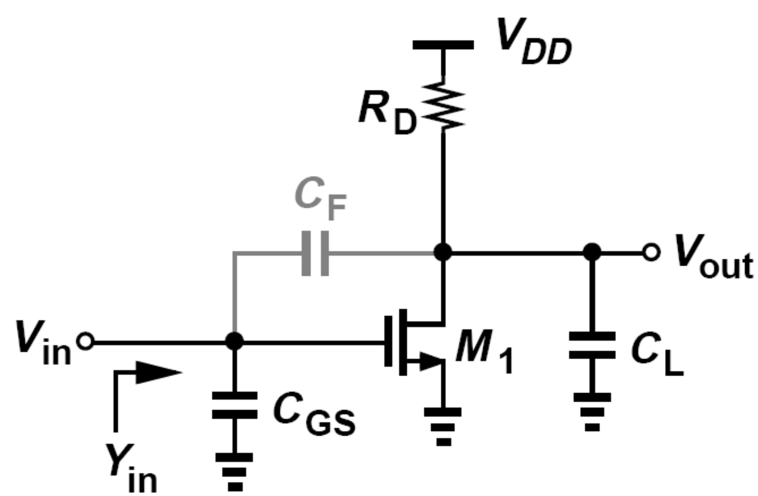


- With more details



Input Matching

- At high frequency, *Re{Z_{in}}* can be quite low because of C_{GD} feedback (C_F) + 2nd order effects at the gate-oxide interface
- *Im{Z_{in}}* comes from C_{GS}, which is a large capacitor => small *Im{Z_{in}}* (far away from 50 Ω)



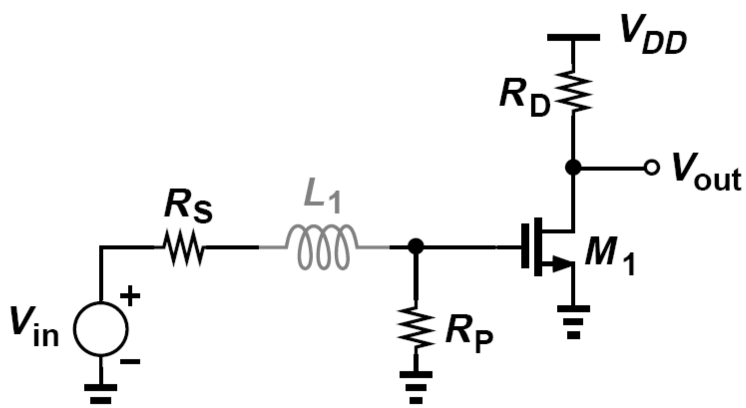
Input Matching: Resistive termination?

- Such a topology is designed in three steps:

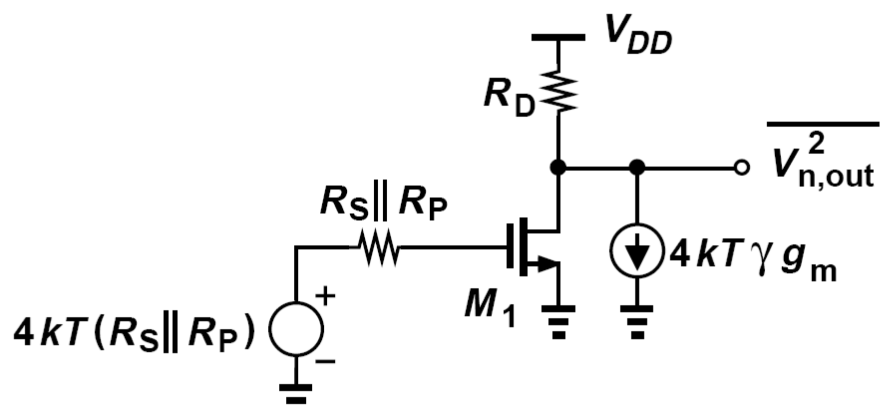
(1) M_1 and R_D provide the required noise figure and gain

(2) R_P is placed in parallel with the input to provide Re{Z_{in}} = 50 Ω

(3) an inductor is interposed between R_S and the input to cancel Im{Z_{in}}.



Circuit with resistive input matching



Simplified for noise analysis

Input Matching: Resistive termination

- Express the total output noise as:

$$\overline{V_{n,out}^2} = 4kT(R_S||R_P)(g_m R_D)^2 + 4kT\gamma g_m R_D^2 + 4kTR_D \quad (5.17)$$

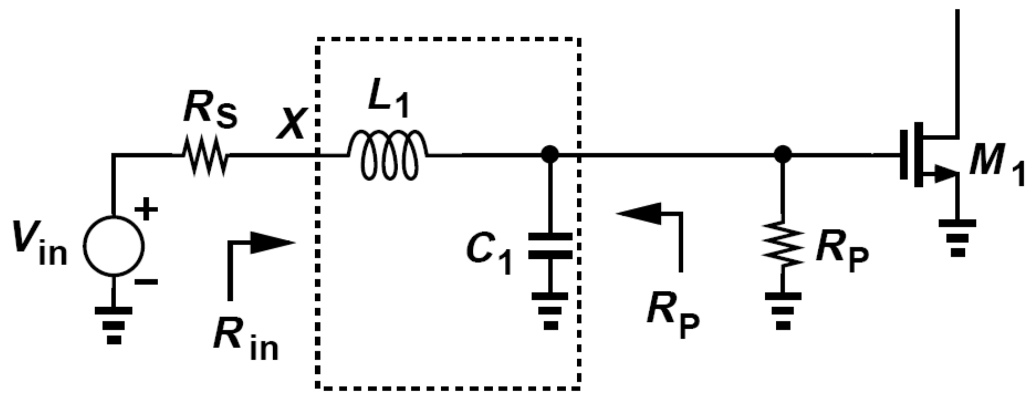
- NF is given by:

$$\text{NF} = 1 + \frac{R_S}{R_P} + \frac{\gamma R_S}{g_m (R_S||R_P)^2} + \frac{R_S}{g_m^2 (R_S||R_P)^2 R_D} \quad (5.18)$$

- If $R_S \approx R_P$, then NF will be ≥ 3 dB.
- We need better way to provide good input matching without the noise of a physical resistor!

Example 5.5

- A student decides to defy the above observation by choosing a large R_P and transforming its value down to R_S. The resulting circuit is shown below (left), where C_1 represents the input capacitance of M_1. (The input resistance of M_1 is neglected.) Can this topology achieve a noise figure less than 3 dB?



- Long derivation in the book => NF = 3 dB
- Conclusion: no.

5.3, 5.6 Some LNA Topologies

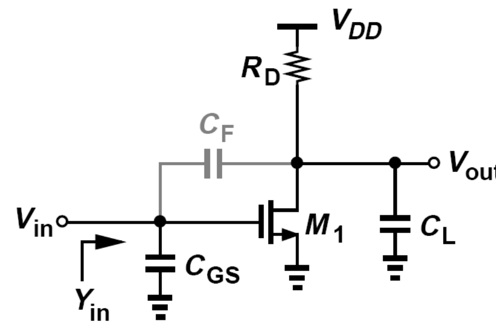
- Proper input (conjugate) matching of LNAs requires certain circuit techniques that yield a real part of 50 Ω in the input impedance without the noise of a 50-Ω resistor.
- The noise figure, input matching, and gain are the principal targets in LNA design. We will present a number of LNA topologies and analyze their behavior with respect to these targets.

Common–Source Stage with	**Common–Gate Stage with**	**Broadband Topologies**
✔ ▪ **Inductive Load**	✔ ▪ **Inductive Load**	▪ **Noise–Cancelling LNAs**
✔ ▪ **Resistive Feedback**	✔ ▪ **Feedback**	▪ **Reactance–Cancelling LNAs**
✔ ▪ **Cascode, Inductive Load,** ✔ **Inductive Degeneration**	▪ **Feedforward**	
	✔ ▪ **Cascode and Inductive Load**	✔ Differential

5.3.1 CS with inductive load

- In general, the trade-off between the voltage gain and the supply voltage in the CS stage with resistive load makes it less attractive as the latter scales down with technology.
  For example, at low frequencies:

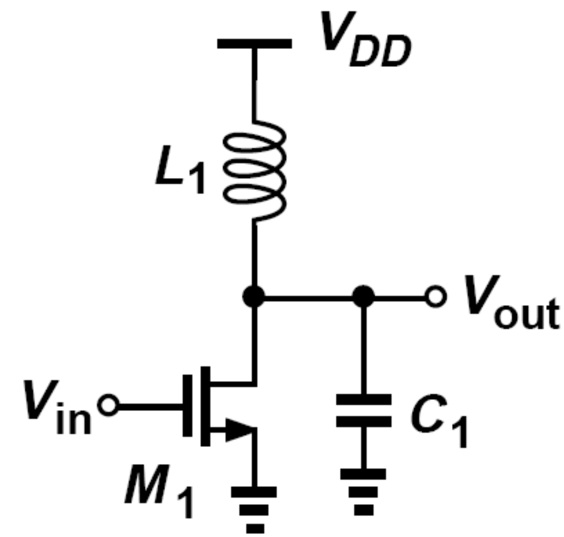
$$
\begin{aligned}
|A_v| &= g_m R_D \\
&= \frac{2I_D}{V_{GS} - V_{TH}} \cdot \frac{V_{RD}}{I_D} \\
&= \frac{2V_{RD}}{V_{GS} - V_{TH}},
\end{aligned}
$$



- A CS stage with resistive load does not provide proper matching
- To circumvent the trade-off expressed above and also operate at higher frequencies, the CS stage can incorporate an <u>inductive load</u>.

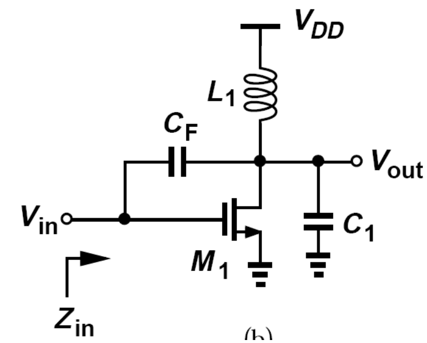
CS with inductive load

- With an inductive load:
  - It can operate with very low supply voltages (smaller DC drop over inductor)
  - L_1 resonates with the total capacitance at the output node (C_1), affording a much higher operation frequency than the resistively-loaded counterpart



CS with inductive load: input match

- Considering C_F (C_{gd} feedback or Miller cap), derivations (p. 272) show that the real part of input impedance can be positive and it is possible to get 50 Ω.



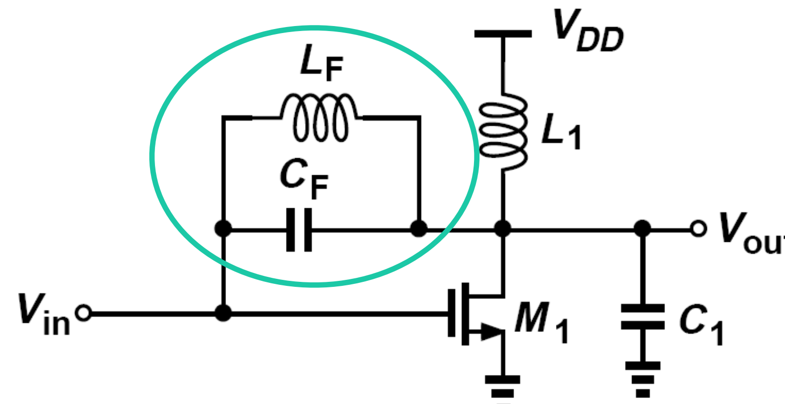
$$Re\{Z_{in}\} = \frac{g_m L_1^2 (C_1 + C_F)\omega^2 + R_S(1 + g_m R_S)(C_1 + C_F) - (R_S C_1 + g_m L_1)}{D}\omega. \quad (5.35)$$

- But at some frequency, Z_{in} becomes negative and might cause instability in the LNA:

$$\omega_1^2 = \frac{R_S C_1 + g_m L_1 - (1 + g_m R_S) R_S (C_1 + C_F)}{g_m L_1^2 (C_1 + C_F)}. \quad (5.36)$$

CS with inductive load: neutralization

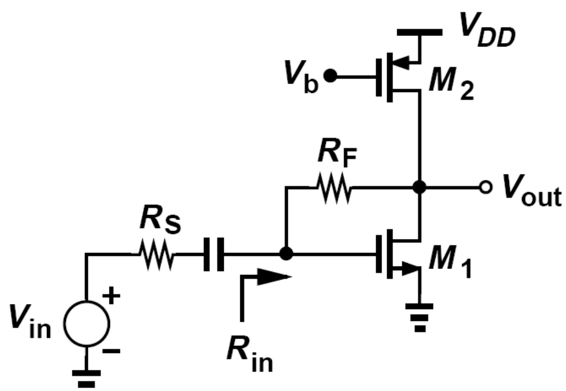
- The feedback capacitance C_F gives rise to a negative input resistance at other frequencies, potentially causing instability.
- It is possible to “neutralize” the effect of CF in some frequency range through the use of parallel resonance.
- Will introduce significant parasitic capacitances at the input and output and degrading the performance.

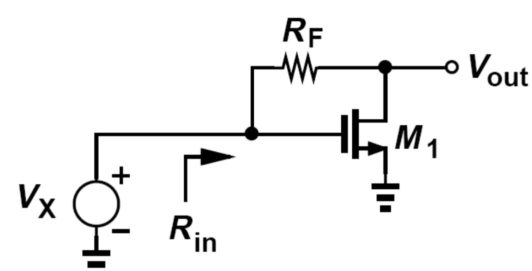


5.3.2 CS with resistive feedback

- Neglecting the channel length modulation => $R_{in} = 1/g_{m1}$
- So we select $g_{m1} = 1/R_s$ to provide matching
- Gain after matching (if $R_F \gg R_S$):

PMOS active load





$$A_v = \frac{1}{2}\left(1 - \frac{R_F}{R_S}\right) \approx -\frac{R_F}{R_S}.$$

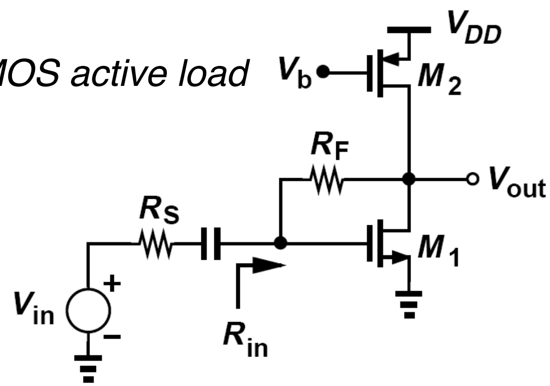
No bias current through R_F => No trade-off between A_v and V_{dd}

CS with resistive feedback

- NF (p. 274/275):

The noise of R_F appears at the output

PMOS active load



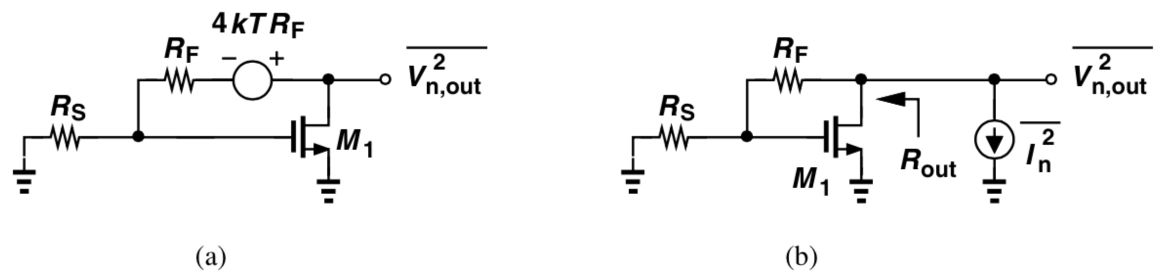


Figure 5.14 *Effect of noise of (a) R_F and (b) M_1 in CS stage.*

- $R_{out} = (R_F+R_S)/2$

$$\overline{V^2_{n,out}}|_{M1,M2} = 4kT\gamma(g_{m1}+g_{m2})\frac{(R_F+R_S)^2}{4}$$

CS with resistive feedback

$$\text{NF} = 1 + \frac{4R_F}{R_S\left(1 - \frac{R_F}{R_S}\right)^2} + \frac{\gamma(g_{m1} + g_{m2})(R_F + R_S)^2}{\left(1 - \frac{R_F}{R_S}\right)^2 R_S}$$

(5.49) $$\approx 1 + \frac{4R_S}{R_F} + \gamma(g_{m1} + g_{m2})R_S$$

$R_F >> R_S$

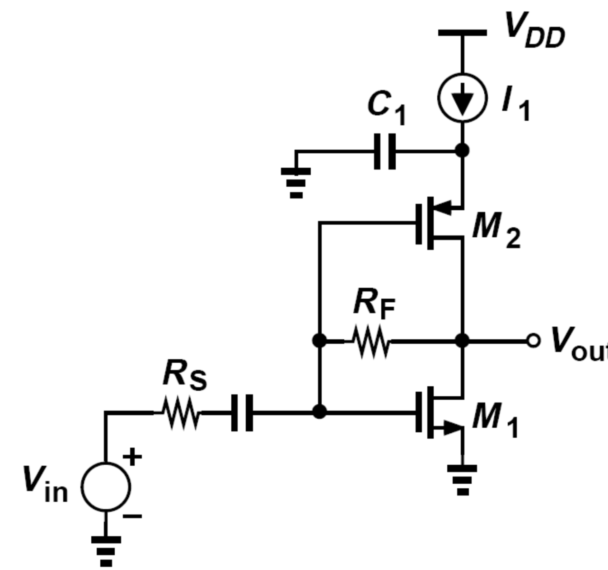
(5.50) $$\approx 1 + \frac{4R_S}{R_F} + \gamma + \gamma g_{m2} R_S.$$

$g_{m1} = 1/R_S$

For $\gamma \approx 1$, NF > 3 dB even if rest of the terms are less than 1

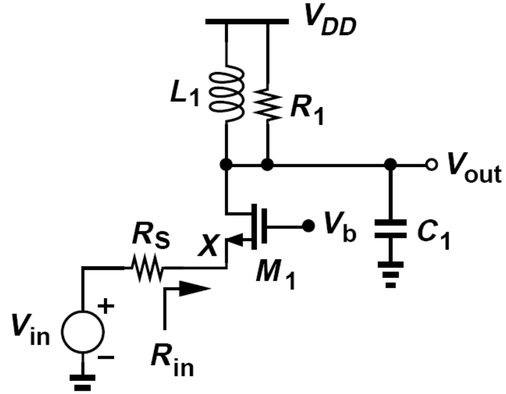
Example 5.7

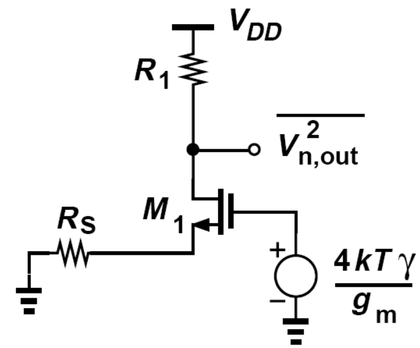
- In the circuit, the PMOS current source is converted to an "active load," amplifying the input signal. The idea is that, if M_2 amplifies the input in addition to injecting noise to the output, then the noise figure may be lower. Neglecting channel-length modulation, calculate the noise figure. (Current source I_1 defines the bias current and C_1 establishes an ac ground at the source of M_2).



5.3.3 Common Gate with inductive load

- Low input impedance of common gate (≈$1/g_m$) makes it attractive. Possible to select $g_m = 1/R_s$.





$$\frac{V_{out}}{V_X} = g_m R_1 = \frac{R_1}{R_S}$$

$$\overline{V_{n,out}^2}|_{M1} = \frac{4kT\gamma}{g_m}\left(\frac{R_1}{R_S + \frac{1}{g_m}}\right)^2 = kT\gamma\frac{R_1^2}{R_S}.$$

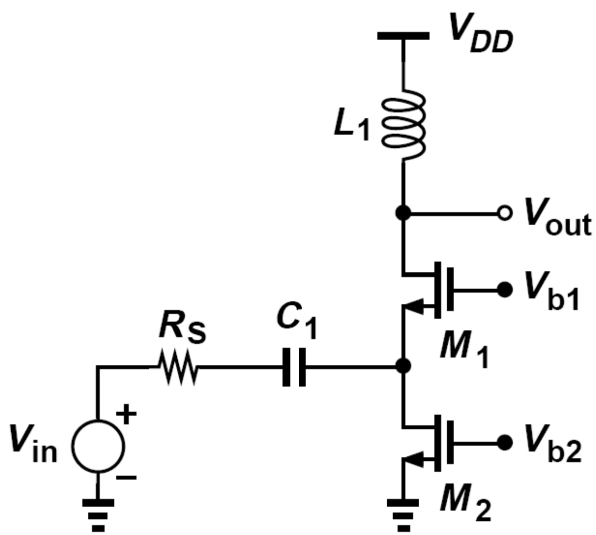
Common Gate with inductive load

$$\Rightarrow \quad \begin{aligned} \mathrm{NF} &= 1 + \frac{\gamma}{g_m R_S} + \frac{R_S}{R_1}\left(1 + \frac{1}{g_m R_S}\right)^2 \\ &= 1 + \gamma + 4\frac{R_S}{R_1}. \end{aligned}$$

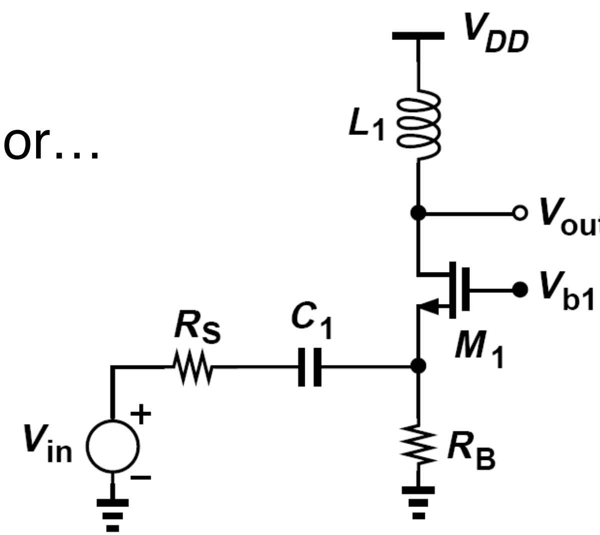
- Even if $4R_S/R_1 << 1+ \gamma$, still around 3 dB or higher.
- $g_m=1/R_S$ => higher g_m yields a lower NF but also a lower input resistance.

Example 5.8

- To provide the bias current of CG stage, is using a resistor (R_B) better than using a transistor (M_2)?

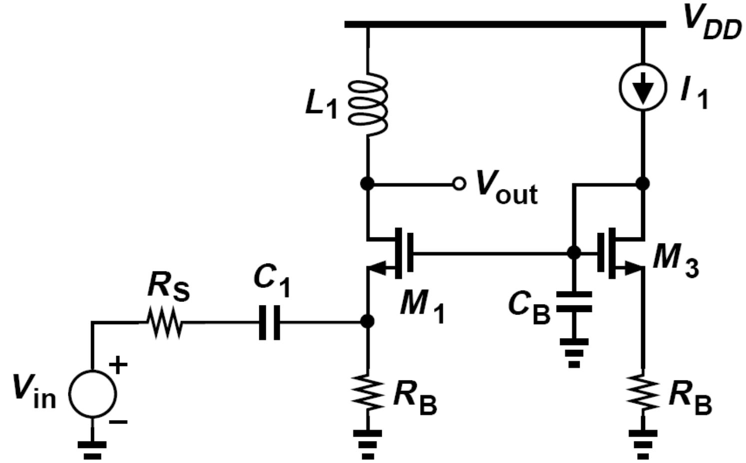


or…



Example 5.8

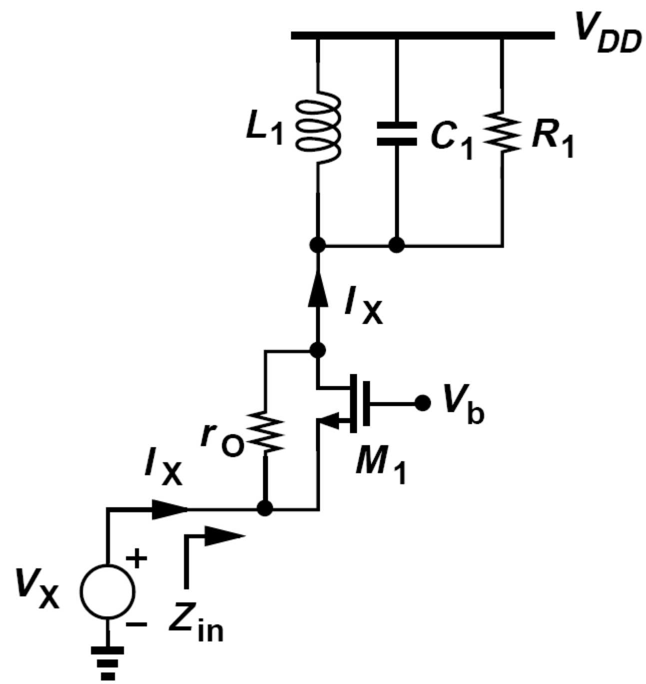
- Since V_{GS2}-V_{TH2} ≤ V_{RB}, the noise contribution of M_2 is about twice that of R_B (for γ ≈ 1). Additionally, M_2 may introduce significant capacitance at the input node.
- The use of a resistor is therefore preferable, as long as R_B is much greater than R_S so that it does not attenuate the input signal. Note that the input capacitance due to M_1 may still be significant. We will return to this issue later. Figure below shows an example of proper biasing in this case.



CG with CLM (r_0 channel length modulation)(p. 279)

- In the presence of CLM ($r_o \neq \infty$):

$$V_X = r_O(I_X - g_m V_X) + I_X R_1$$



$$\frac{V_X}{I_X} = \frac{R_1 + r_O}{1 + g_m r_O}$$

$$\frac{V_{out}}{V_{in}} = \frac{g_m r_O + 1}{2\left(1 + \frac{r_O}{R_1}\right)}$$

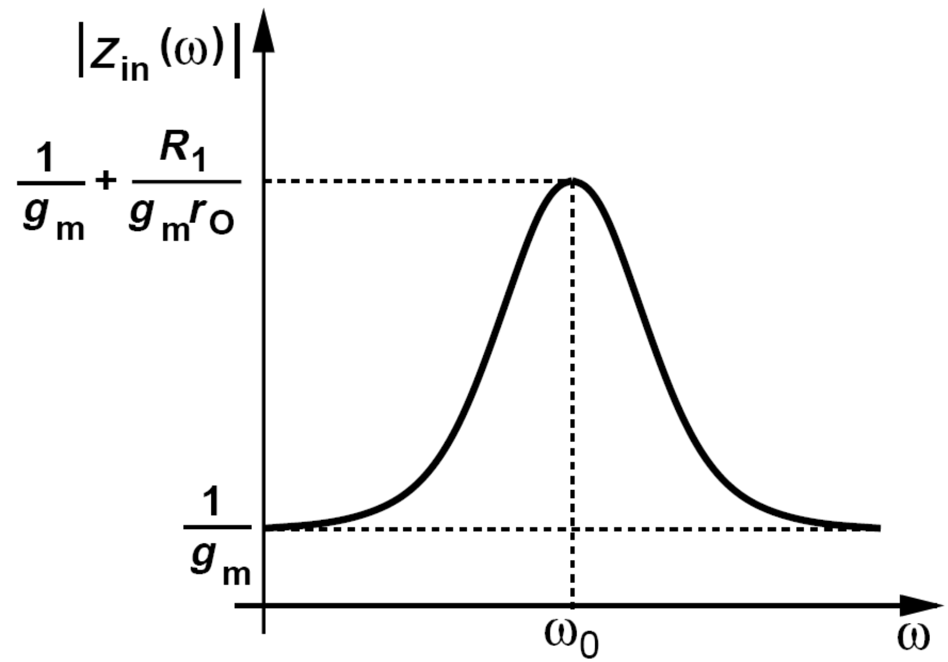
$g_m r_0$ usually <10

If r_O and R_1 are comparable, then gain ~ $g_m r_O/4$, a very low value.

Example 5.9

- Plot the input impedance as a function of frequency (neglect M_1 cap)

- At very low or high frequency, $Z_{in} = 1/g_m$
- At some resonance frequency, the tank will influence Z_{in} considerably!



Cascode CG (p. 281)

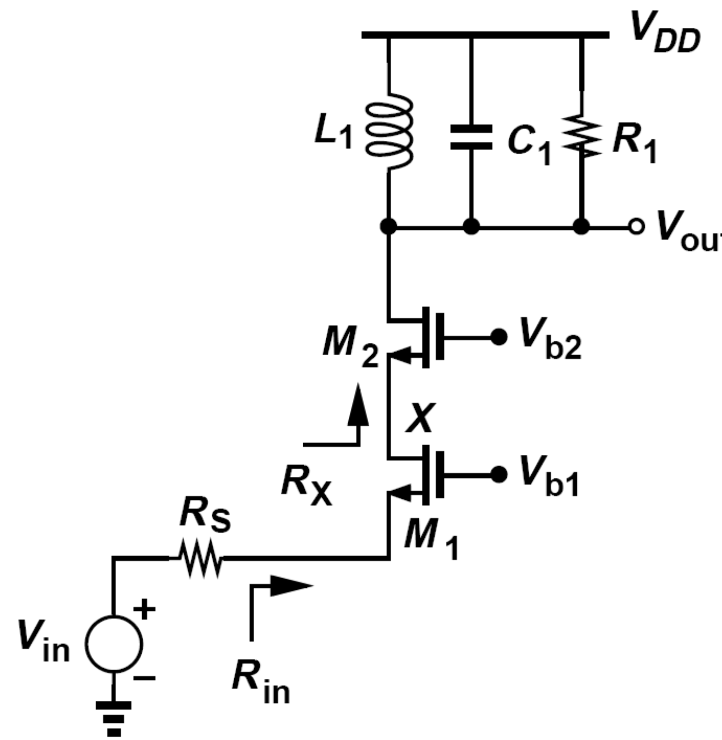
- To lower the input impedance in the presence of CLM, one solution is to use a CG cascode stage.

$$R_X = \frac{R_1 + r_{O2}}{1 + g_{m2} r_{O2}}$$

$$R_{in} = \left(\frac{R_1 + r_{O1}}{1 + g_{m2} r_{O2}} + r_{O1} \right) \div (1 + g_{m1} r_{O1})$$

If $g_m r_O$ >>1, then:

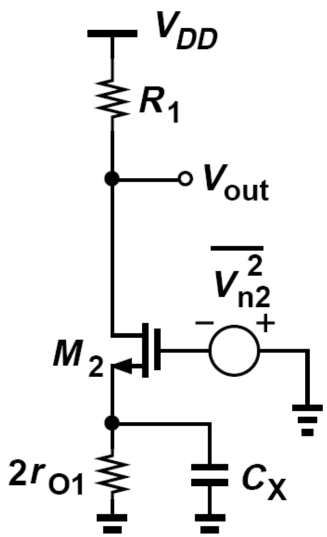
$$R_{in} \approx \frac{1}{g_{m1}} + \frac{R_1}{g_{m1} r_{O1} g_{m2} r_{O2}} + \frac{1}{g_{m1} r_{O1} g_{m2}}$$

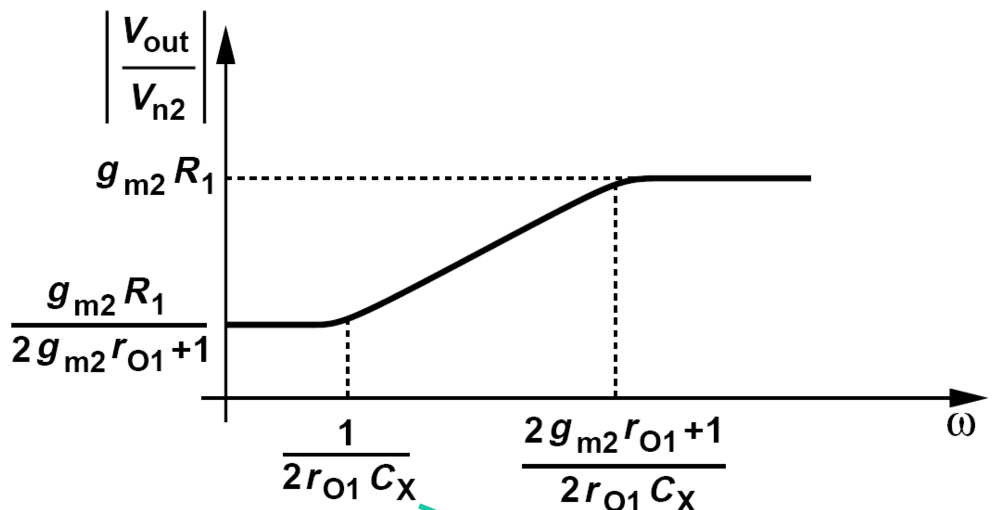


It means $R_{in} \approx 1/g_m$ and the input impedance is reduced significantly

Cascode CG

- Noise contribution of the cascode transistor:





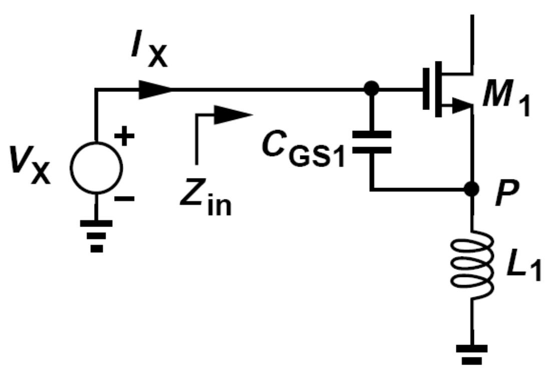
$$\frac{V_{n,out}}{V_{n2}}(s) = \frac{R_1}{\frac{1}{g_{m2}} + (2r_{O1})||\frac{1}{C_X s}}$$

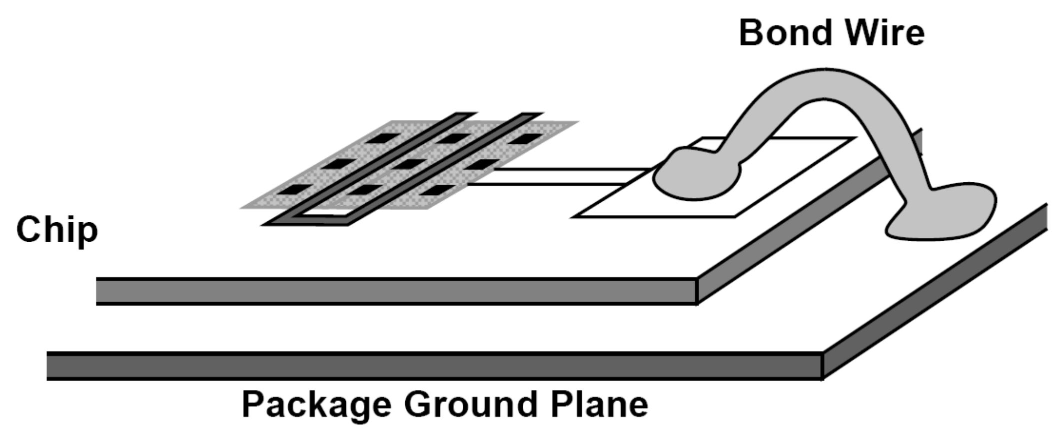
$$= \frac{2r_{O1}C_X s + 1}{2r_{O1}C_X s + 2g_{m2}r_{O1} + 1} g_{m2}R_1$$

Noise from M_2 is small up to some frequency, then it manifests itself more.

5.3.4 CS with Degeneration

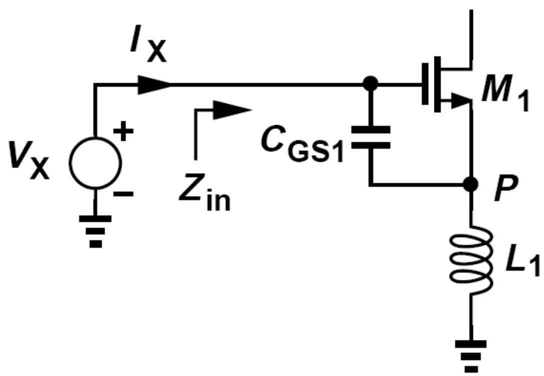
- The feedback through the gate-drain capacitance many be exploited to produce the required real part but it also leads to a negative resistance at lower frequencies.





CS with Degeneration

- Creating a resistive term without additional noise:



$$V_P = \left(I_X + \frac{g_m I_X}{C_{GS1} s} \right) L_1 s$$

Since $V_X = V_{GS1} + V_P$

$$\frac{V_X}{I_X} = \frac{1}{C_{GS1} s} + L_1 s + \frac{g_m L_1}{C_{GS1}}$$

$$Z_{in} = sL_1 + \frac{1}{sC_{GS1}} + \frac{g_m}{C_{GS1}} L_1 \approx sL_1 + \frac{1}{sC_{GS1}} + \omega_T L_1$$

Real part which is considered as a resistive term ~ 50 Ω

In practice, the degeneration inductor is often realized as a bond wire since the latter is inevitable in packaging and must be incorporated in the design.

Example 5.13

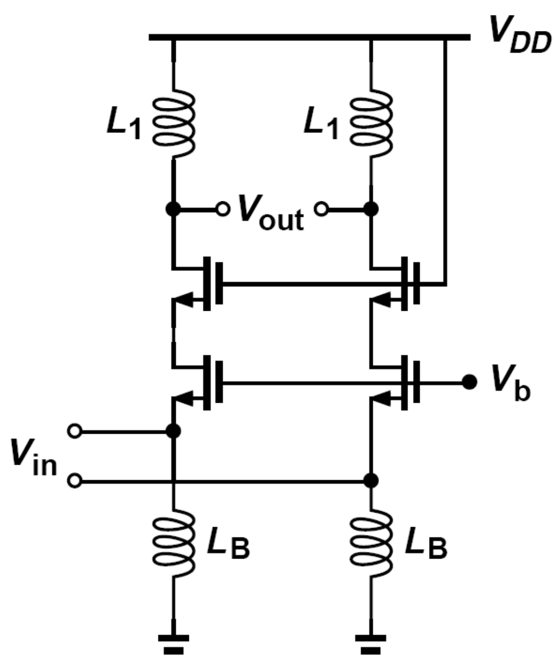
- A 5-GHz LNA requires a value of 2 nH for L_G. Discuss what happens if L_G is integrated on the chip and its Q does not exceed 5.

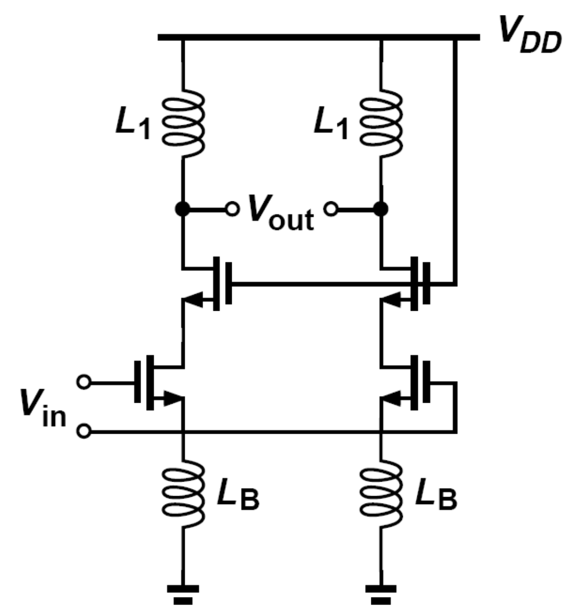
With Q = 5, L_G suffers from a series resistance equal to $L_G\omega/Q$ =12.6 Ohm. This value is not much less than 50 Ohm, degrading the noise figure considerably. For this reason, L_G is typically placed off-chip.

Lecture 7: inductors and other passives on chip.

5.6.1 Differential

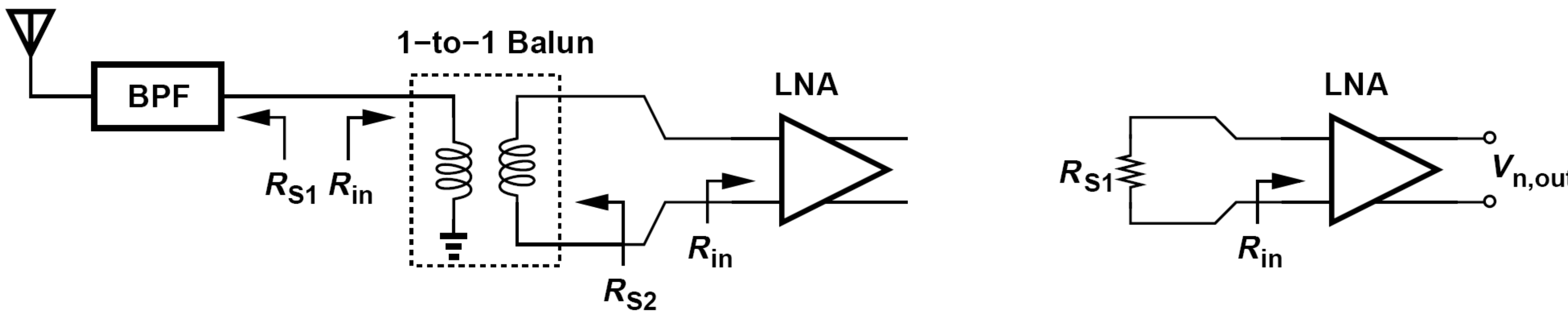
- Differential LNAs can achieve high IP_2 because symmetric circuits produce no even-order distortion. In principle, any single-ended LNA can be converted to differential form (CG (left) and CS (right), both simplified).





Differential

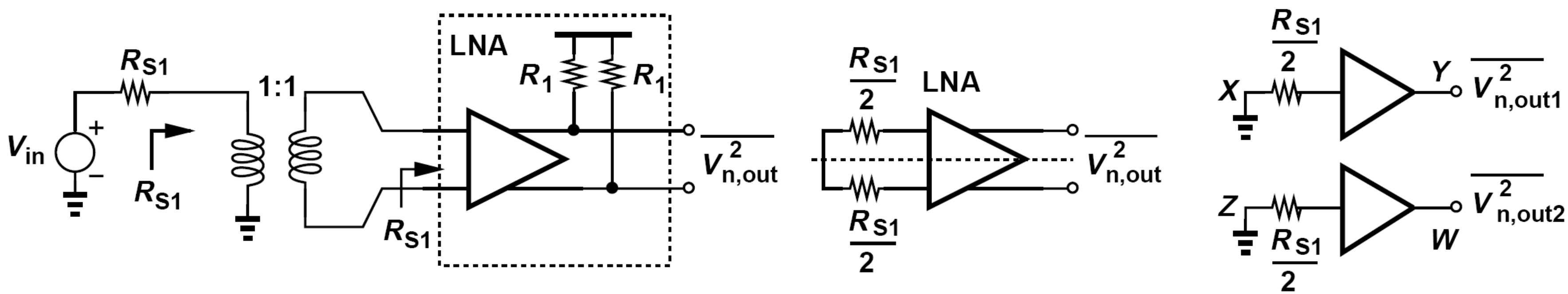
- Since the antenna and the preselect filter are typically single-ended, a transformer (**balun**) must precede the LNA to perform single-ended to differential conversion.



- The transformer is called a "balun," an acronym for "balanced-to-unbalanced" conversion because it can also perform differential to single-ended conversion if its two ports are swapped.
- Figure above right is the setup for output noise calculation.

Differential CG LNA: Noise Figure

- Assuming it is designed such that the impedance seen between each input node and ground is equal to $R_{S1}/2$:



- From the symmetry of the circuit that we can compute the output noise of each half circuit and add the output powers:

$$\overline{V^2_{n,out}} = \overline{V^2_{n,out1}} + \overline{V^2_{n,out2}}$$

Differential

$$\overline{V_{n,out1}^2} = kT\gamma \frac{R_1^2}{R_{S1}/2} + 4kTR_1 + 4kT\frac{R_{S1}}{2}\left(\frac{R_1}{\frac{2R_{S1}}{2}}\right)^2. \tag{5.149}$$

gives the NF for the differential circuit

$$\text{NF} = \frac{\overline{V_{n,out}^2}}{A_v^2} \cdot \frac{1}{4kTR_{S1}} \tag{5.150}$$

$$= 1 + \gamma + \frac{2R_{S1}}{R_1}. \tag{5.151}$$

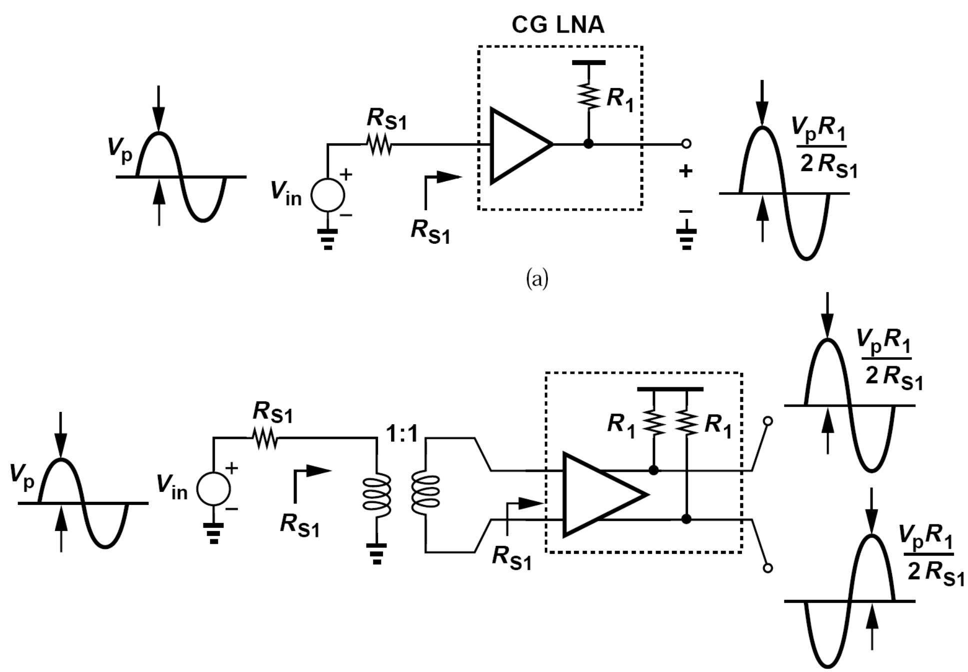
compare this with the NF for the single-ended circuit!

$$\text{NF} = 1 + \frac{\gamma}{g_m R_S} + \frac{R_S}{R_1}\left(1 + \frac{1}{g_m R_S}\right)^2 \tag{5.57}$$

$$= 1 + \gamma + 4\frac{R_S}{R_1}. \tag{5.58}$$

Comparison SE and Diff LNA

- Voltage gain of a differential CG LNA is twice that of the single ended version. On the other hand, the overall differential circuit contains two R_1 at its output, each contributing a noise power of $4kTR_1$.



Summary

- The LNA is used for amplification of the received signal in RF receivers. It should have as little as possible noise.
- There is a trade-off between noise figure, gain, linearity, input impedance, and power consumption of LNAs.
- Different LNA topologies have been presented. The main idea is to reduce the noise figure while providing input match and good gain.