TSEK03: Radio Frequency Integrated Circuits (RFIC)

Lecture 11: PA

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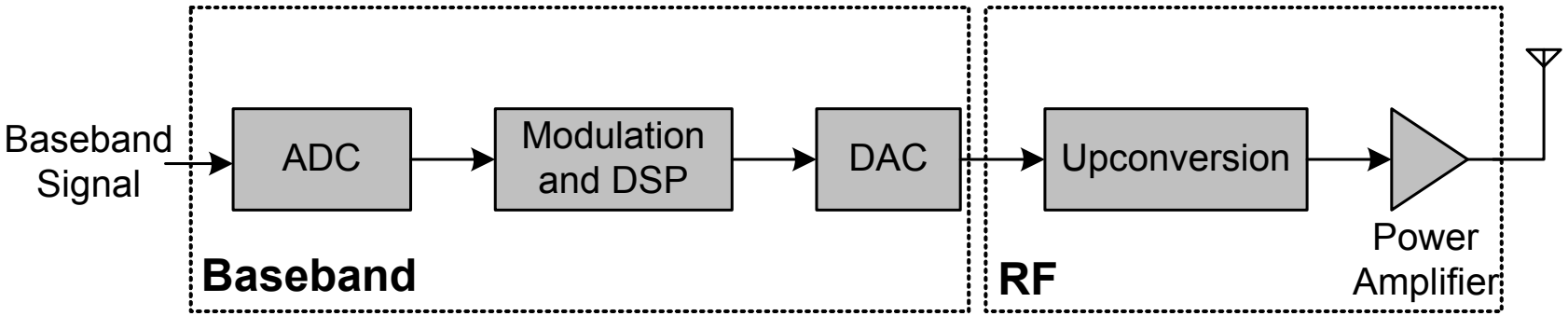
Overview

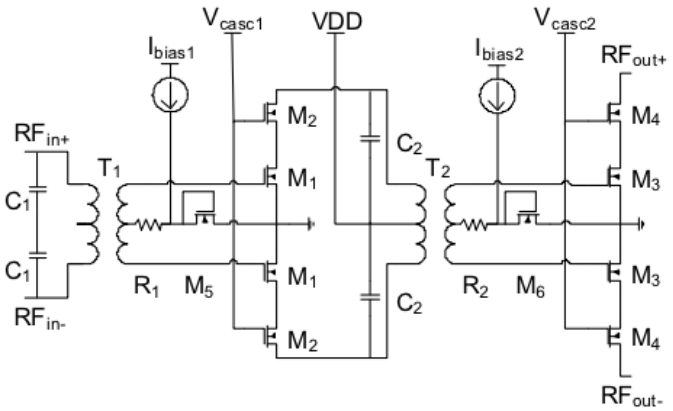
- Razavi: Chapter 12, mainly pp. 767-798.
  - 12.1 General considerations
  - 12.2 - 12.3 PA classes
  - 12.4 - 12.8 highlights: cascodes, matching, polar modulation, outphasing, Doherty (a few slides only).

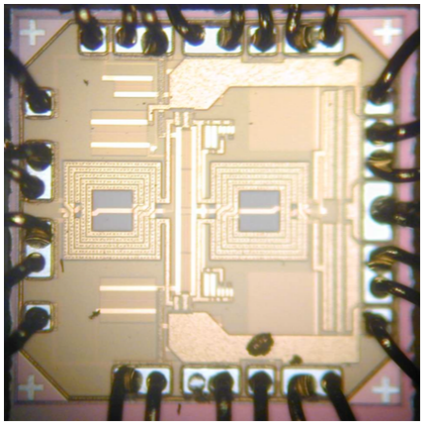
- Lee: Chapter 15

Power Amplifiers

- To transmit an RF signal, we need a power amplifier.



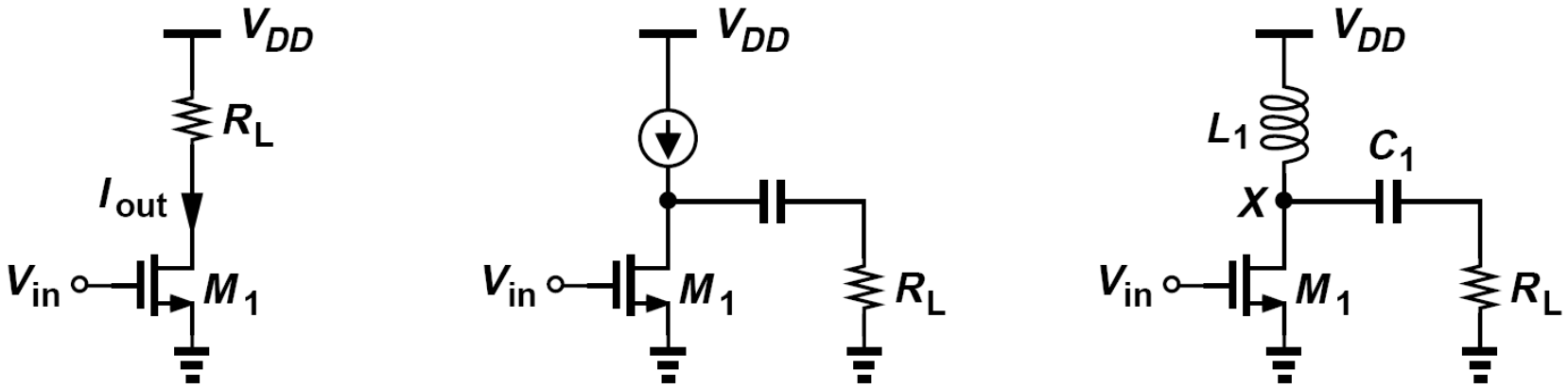




For WLAN using 65 nm CMOS, Fritzin & Johansson (2006)

Output Power and Voltage Swing

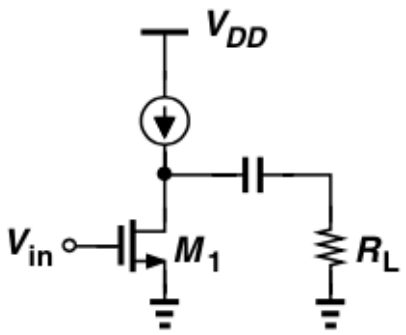
- For a common-source (or common-emitter) stage to drive the load directly, a supply voltage greater than V_{pp} is required.
- If the load is realized as an inductor, the drain ac voltage exceeds V_{DD}, even reaching $2V_{DD}$ (or higher). But the maximum drain-source voltage experienced by M_1 is still at least 20 V if the stage must deliver 1 W to a 50-Ω load.
- It can be proven that the product of the breakdown voltage and f_T of silicon devices is around 200 GHz·V.



Output Power and Voltage Swing

- Ex: 1 W (30 dBm) into a resistive 50 Ω load (e.g. antenna).

$$P = \frac{V_p^2}{2R_L}$$



=> 10 V_p, I_p = 200 mA.

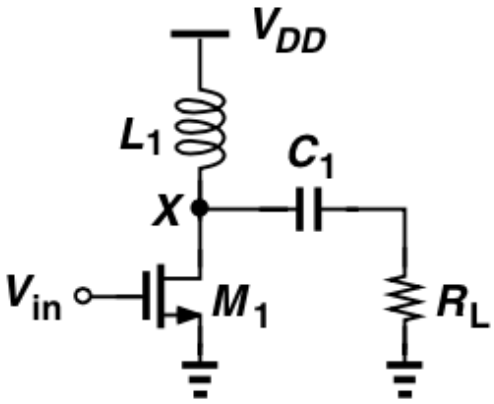
- How can we achieve this with nm-CMOS?

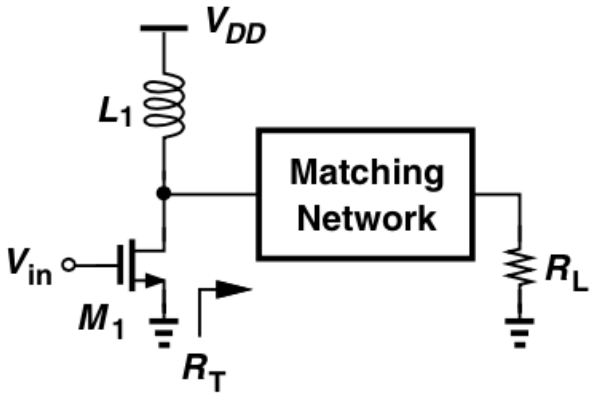
=> Impedance transformation: lower voltage, more current

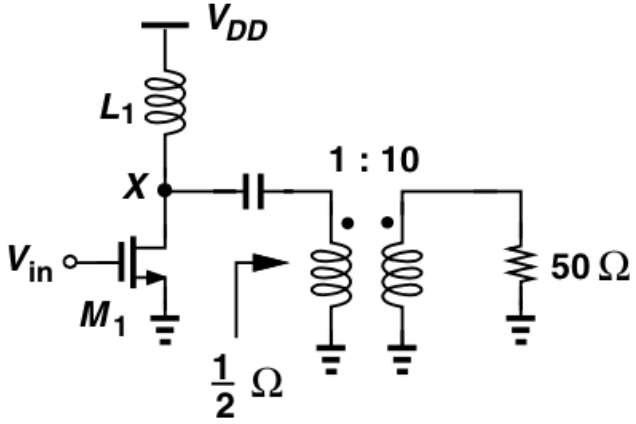
- For high-power PAs: as high supply voltage as possible, and impedance transformation.

PA: how to reach high power

- By using an inductive load, we can reach 2*V_{DD}.
- By adding a matching network, we can increase output power with same supply (by increased transistor size).

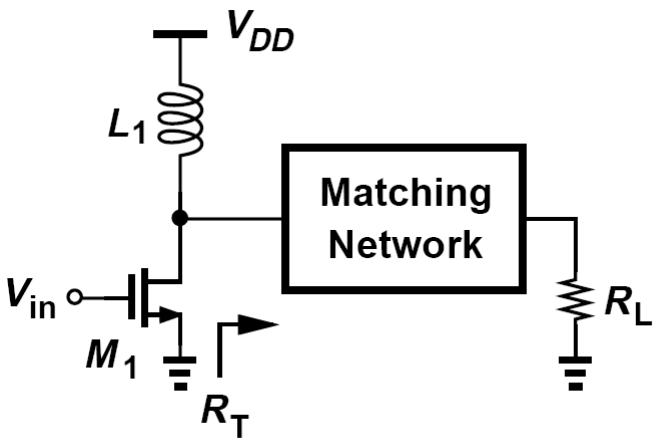


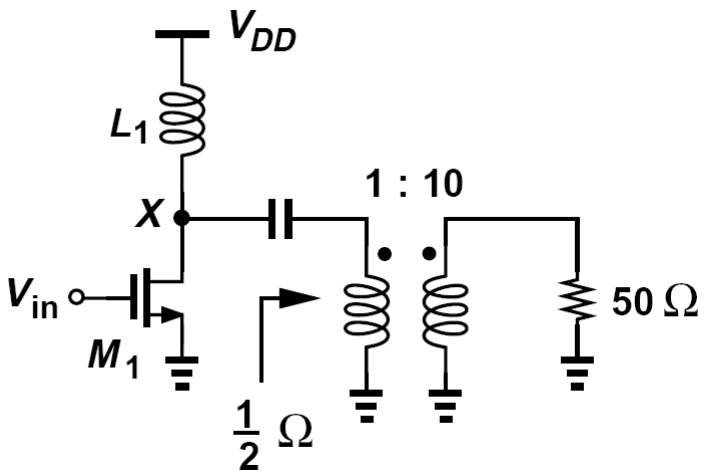




Matching Network

- In order to reduce the peak voltage experienced by the output transistor, a matching network is interposed between the PA and the load. This network transforms the load resistance to a lower value, R_T, so that smaller voltage swings still deliver the required power.





Example 12.2

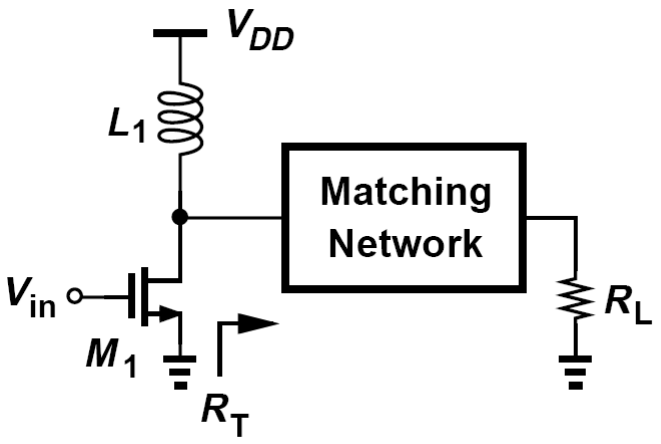
- The PA must deliver 1 W to R_L = 50 Ω with a supply voltage of 1 V. Estimate the value of R_T.

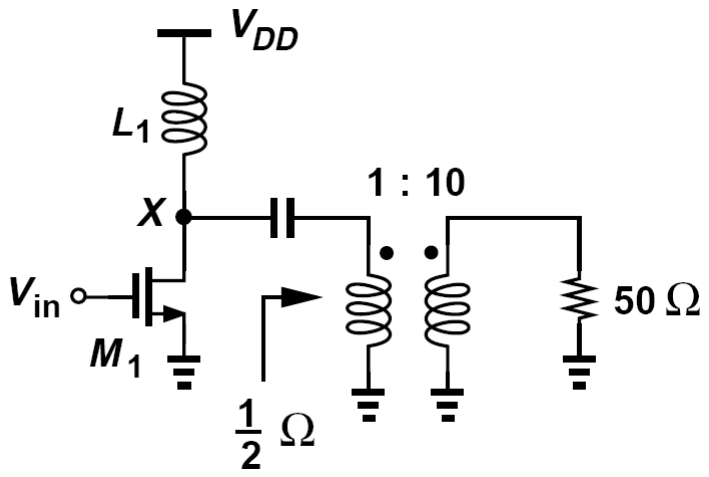
- The peak-to-peak voltage swing, V_{pp}, at the drain of M_1 is approximately equal to 2 V.

$$\begin{aligned} P_{out} &= \frac{1}{2}\left(\frac{V_{pp}}{2}\right)^2 \frac{1}{R_T} \\ &= 1\ \text{W}, \end{aligned} \quad \Rightarrow \quad R_T = \frac{1}{2}\ \Omega.$$

Example 12.2

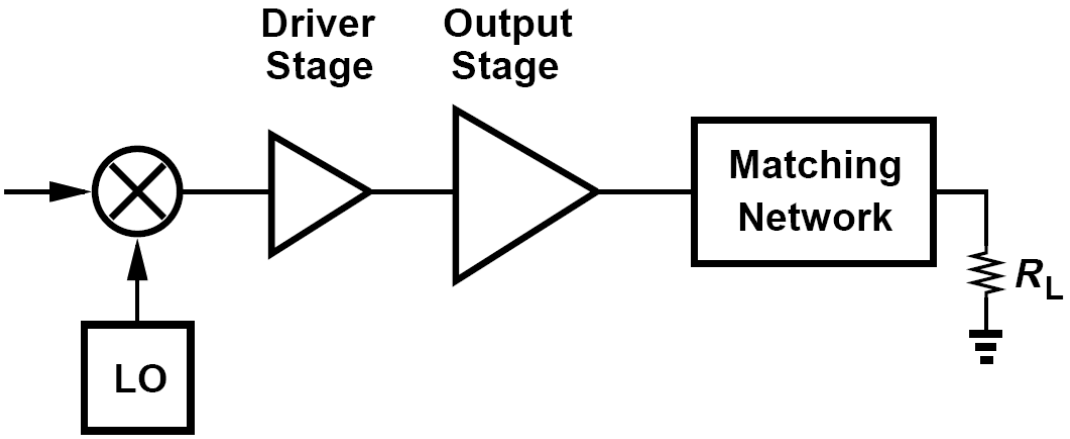
- The matching network must therefore transform R_L down by a factor of 100.
- Figure below shows an example, where a lossless transformer having a turns ratio of 1:10 converts a 2-V_{pp} swing at the drain of M_1 to a 20-V_{pp} swing across RL.



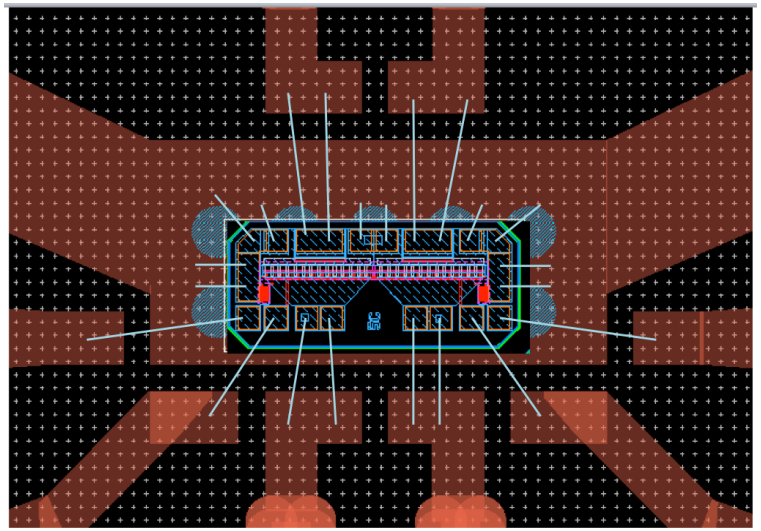


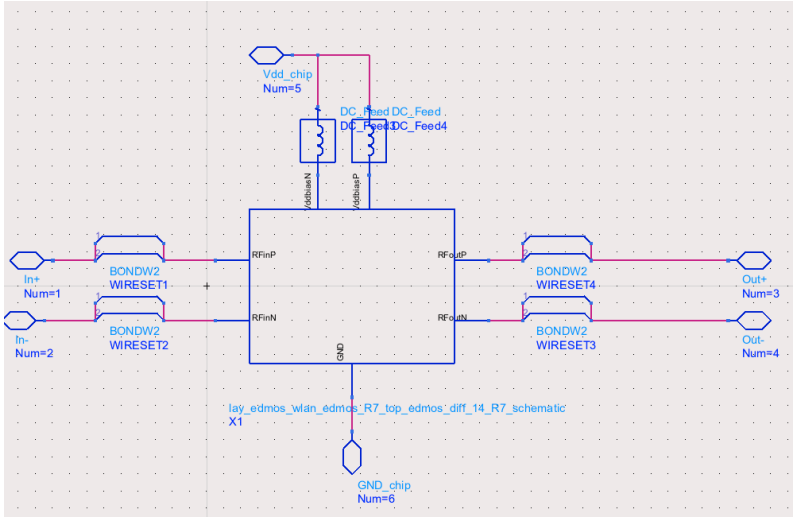
High output power PAs

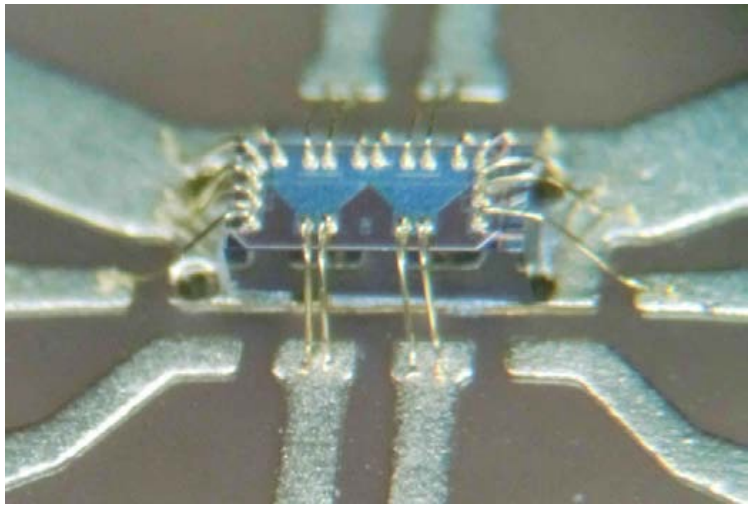
- Usually consists of 2-3 stages (integrated), to handle matching and gain, including interstage matching, but the output matching network is usually off-chip.

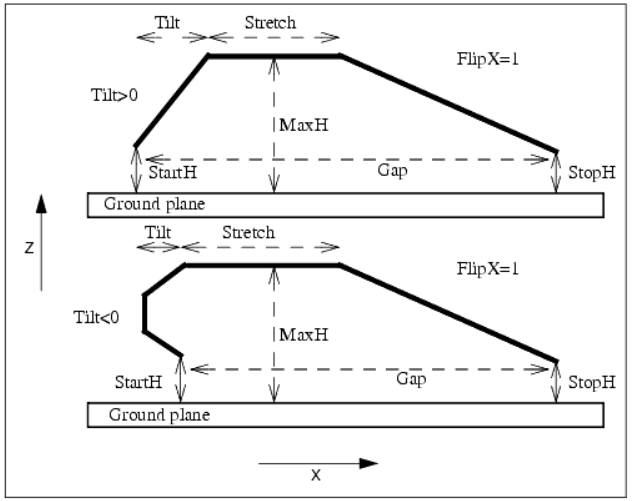


PA bondwires (65 nm CMOS WLAN-PA)

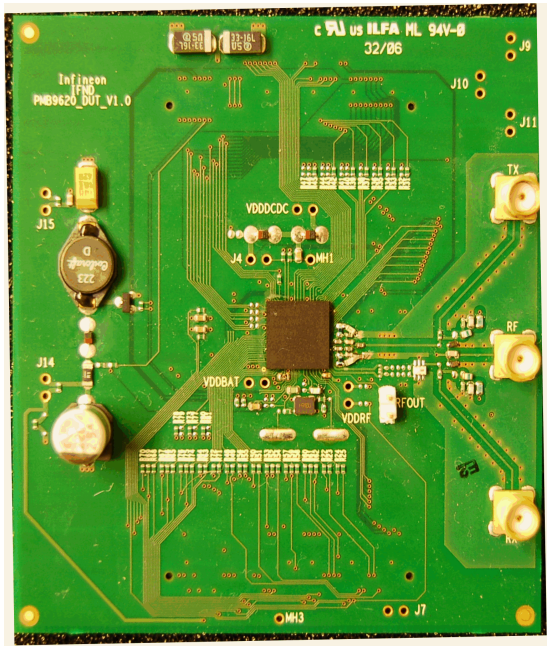


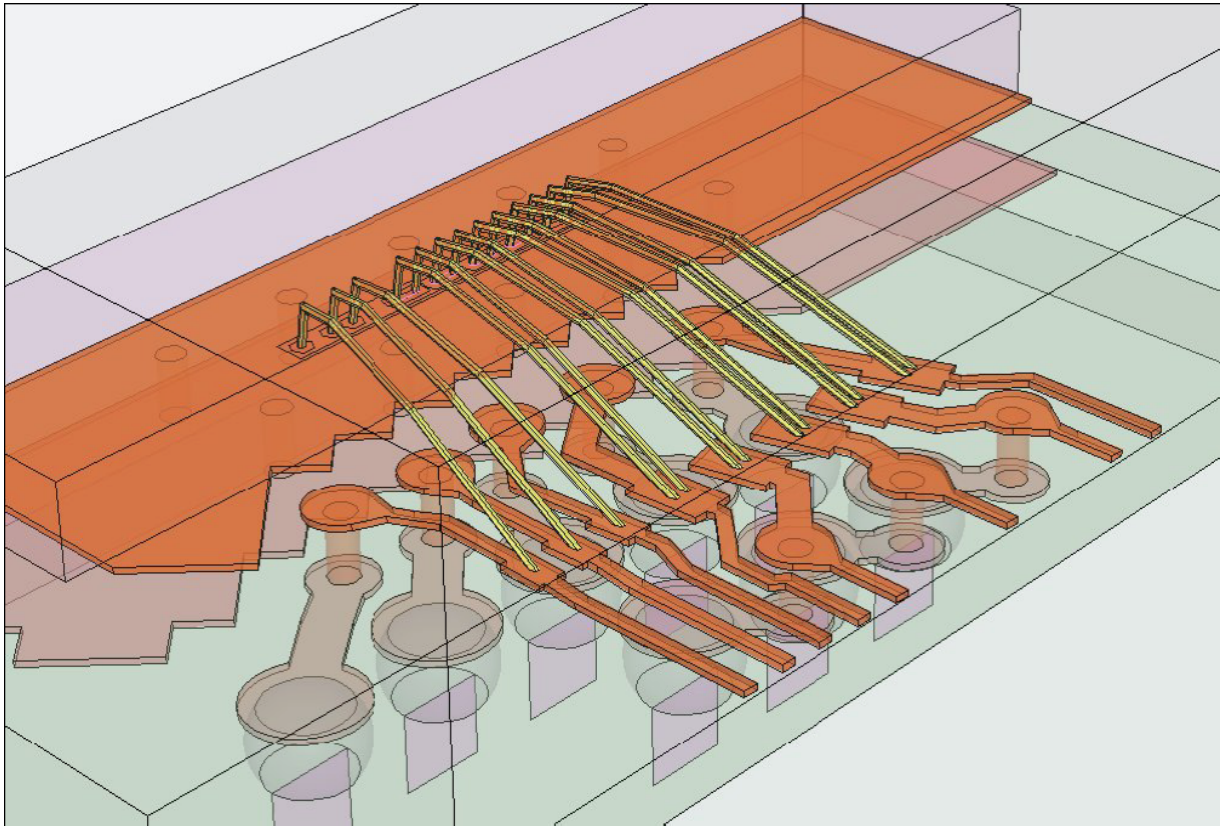






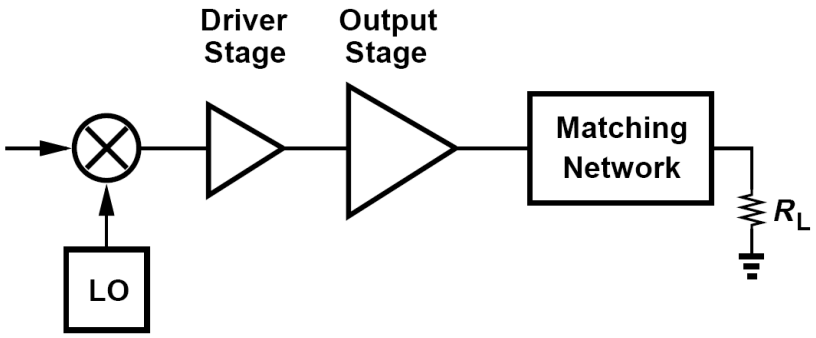
PA package + bondwires





Example 12.4

- The output transistor in previous example with a transformer carries a current varying between 0 and 4 A at a frequency of 1 GHz.
- What is the maximum tolerable bond wire inductance in series with the source of the transistor if the voltage drop across this inductance must remain below 100 mV?



Example 12.4

The drain current of M_1 can be approximated as

$$I_D(t) = I_0 \cos \omega_0 t + I_0, \tag{12.4}$$

where $I_0 = 2$ A and $\omega_0 = 2\pi(1\text{ GHz})$. The voltage drop across the source inductance, L_S, is given by

$$V_{LS} = L_S \frac{dI_D}{dt}, \tag{12.5}$$

reaching a peak of $L_S\omega_0 I_0$. For this drop to remain below 100 mV, we have

$$L_S < 7.96\,\text{pH}. \tag{12.6}$$

This is an extremely small inductance. (A single bond wire's inductance typically exceeds 1 nH.)

PA: Efficiency

- Drain (collector) efficiency [%]

$$\eta_D = \frac{P_{RF}}{P_{DC}}$$

- Power-added efficiency [%]

$$PAE = \frac{P_{RF} - P_{IN}}{P_{DC}}$$

- PAE can also be expressed as

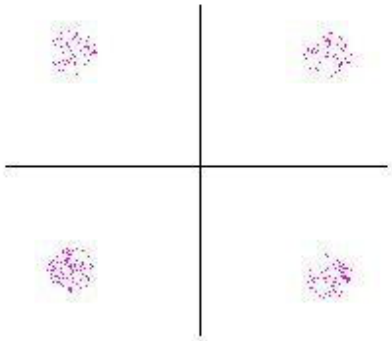
$$PAE = \eta_D \frac{G-1}{G}$$

- PAE: when gain is low, it takes some power to drive the PA, must be accounted for!

- Efficiency: Assume 50 % efficiency
  => 1 W Pout => 2 W from battery/supply!

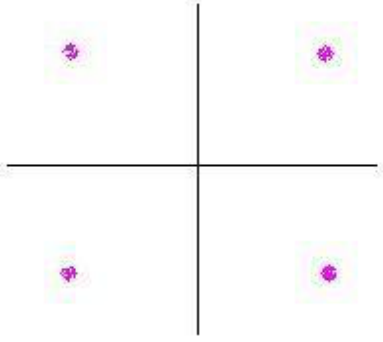
PA characterization: Linearity

- Linearity in wireless systems requirements: EVM and ACPR, but takes long time to simulate.



QPSK Costellation with EVM=20 dB

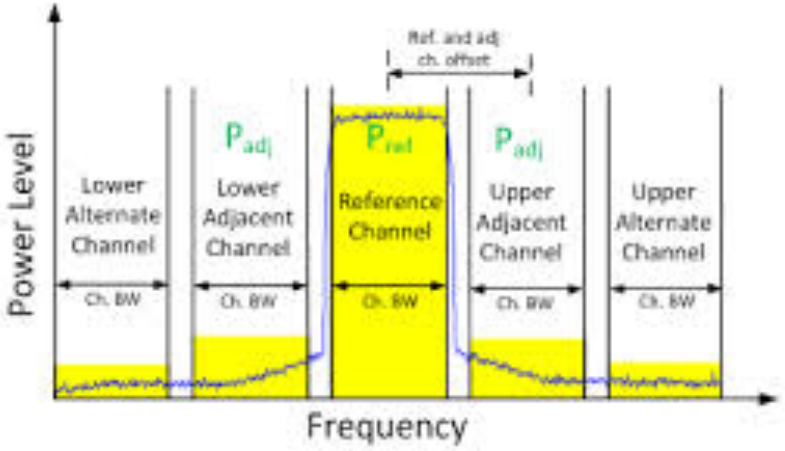
Fig. 2a



QPSK Costellation with EVM=35 dB

Fig. 2b

$$ACPR(dBc) = 10 \cdot log_{10}\left(\frac{P_{adj}}{P_{ref}}\right)$$

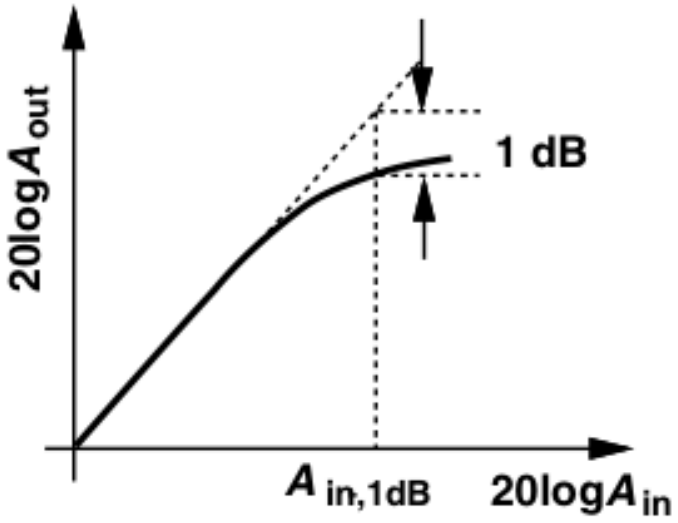


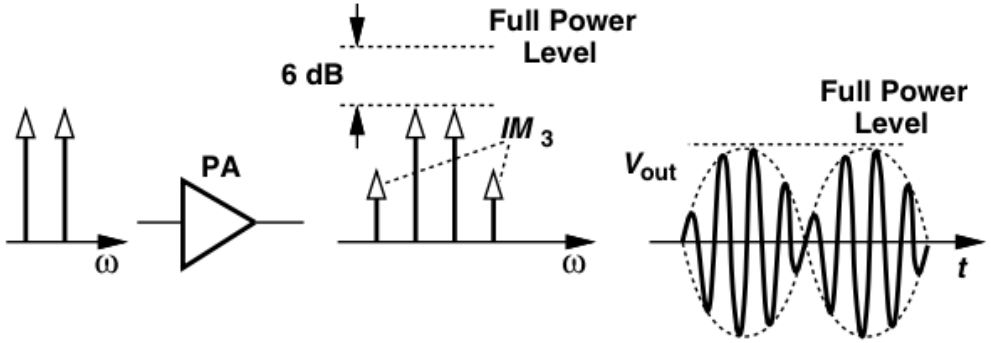
EVM

ACPR

PA characterization: Linearity

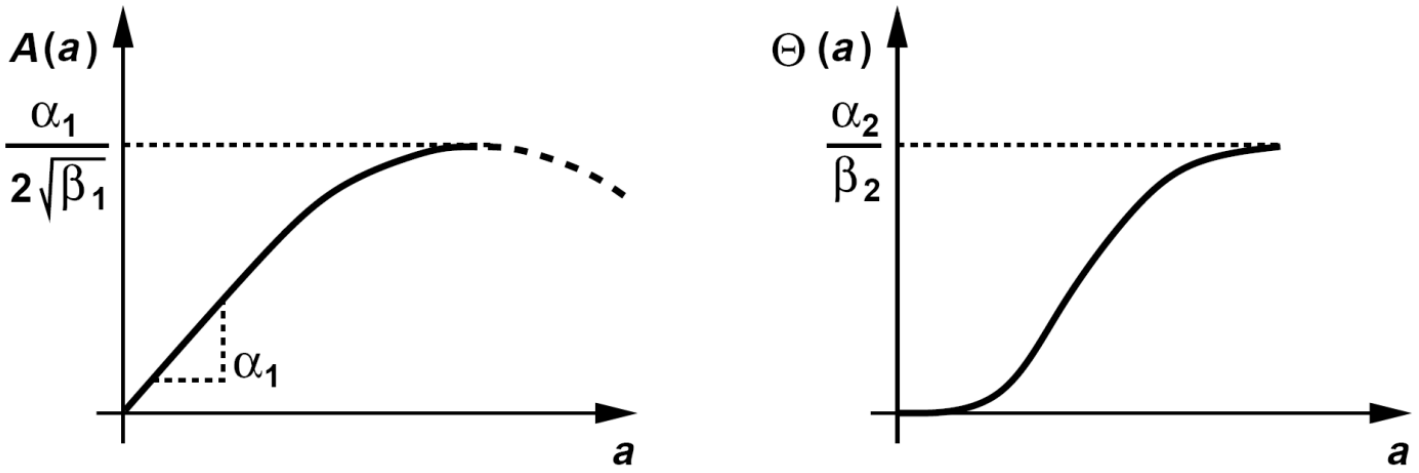
- During design work, P_{1dB} compression point (one-tone) and intermodulation (two tones) give fast information!





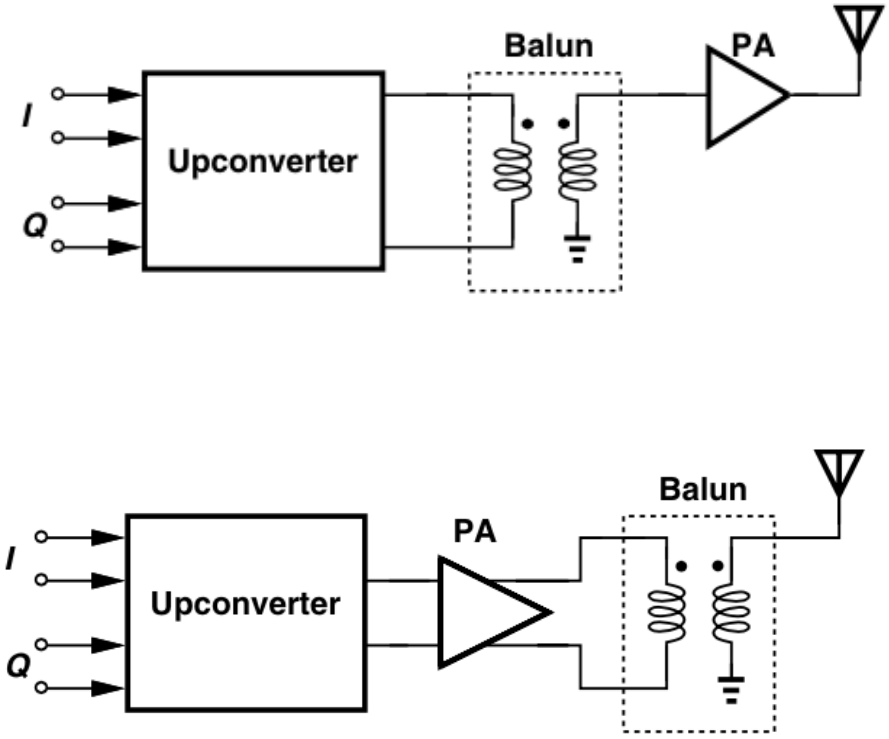
PA characterization: Linearity

- Simulating (and measuring) the AM-AM and AM-PM conversion are also fast methods to estimated linearity.



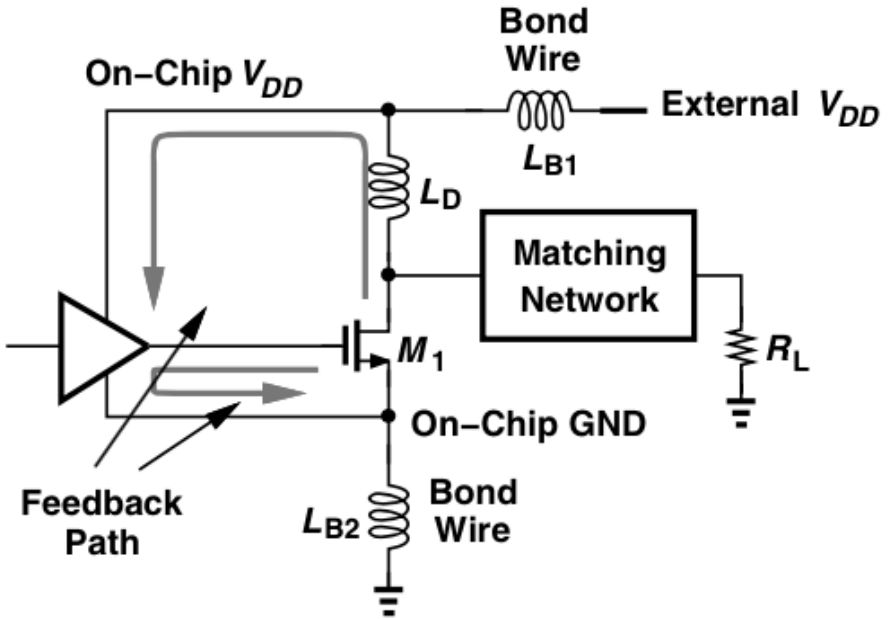
SE vs. Differential

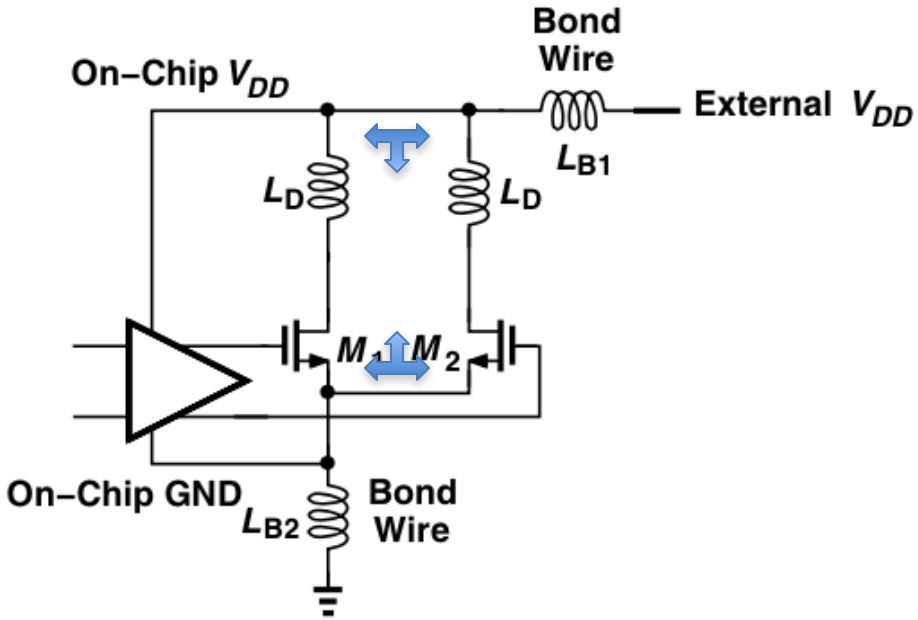
- Possibly differential outputs from previous blocks in IC design.
- By cutting the PA in two halves, a factor of 4 better impedance/more output power (for same Z) is gained.
- But we need baluns on output and maybe also on the input => losses.



SE vs. Differential

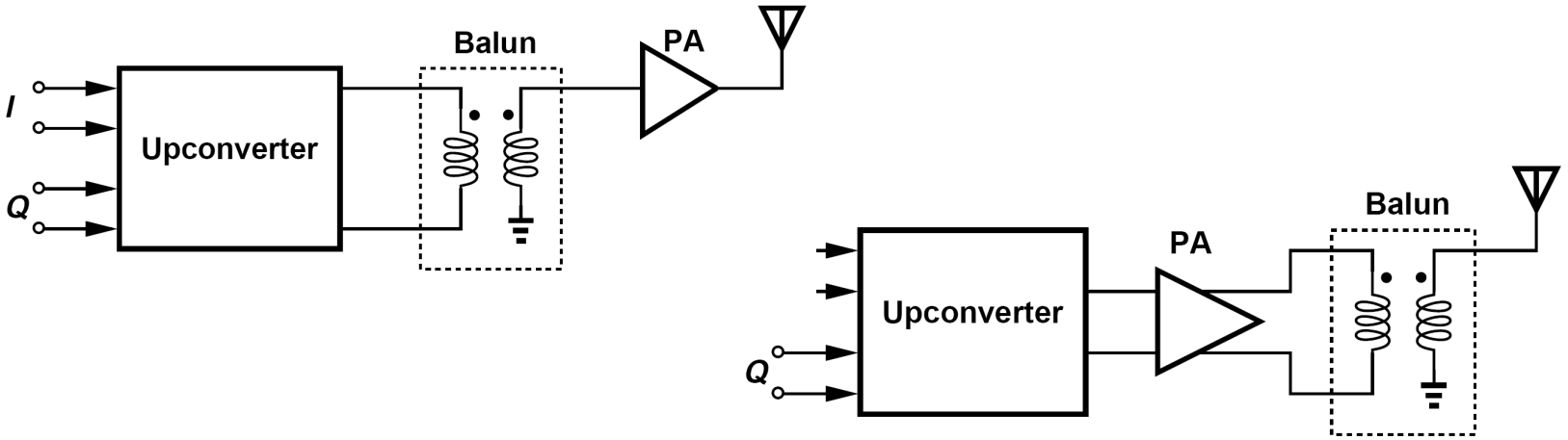
- With a differential design, some of the large currents will be internal, not external!



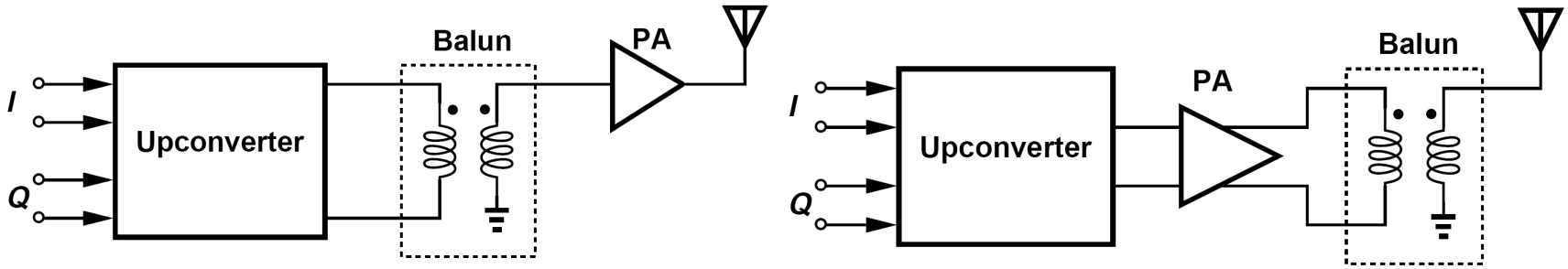


Example 12.6

- Suppose a given balun design has a loss of 1.5 dB. In which one of the transmitters shown below does this loss affect the efficiency more adversely?

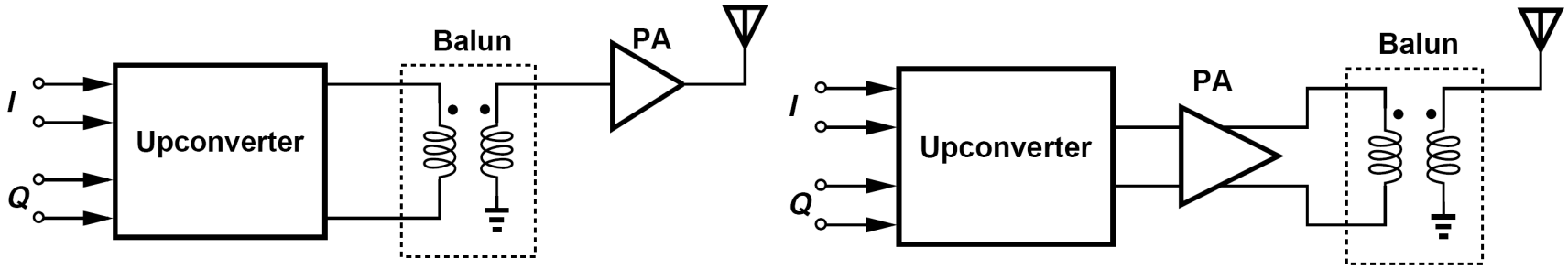


Example 12.6



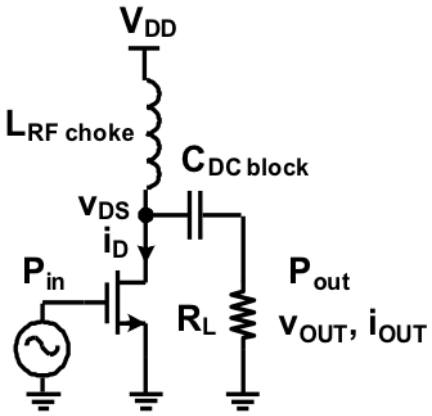
- In the figure left, the balun lowers the voltage gain by 1.5 dB but does not consume much power.
- For example, if the power delivered by the upconverter to the PA is around 0 dBm, then a balun loss of 1.5 dB translates to a heat dissipation of 0.3 mW.

Example 12.6

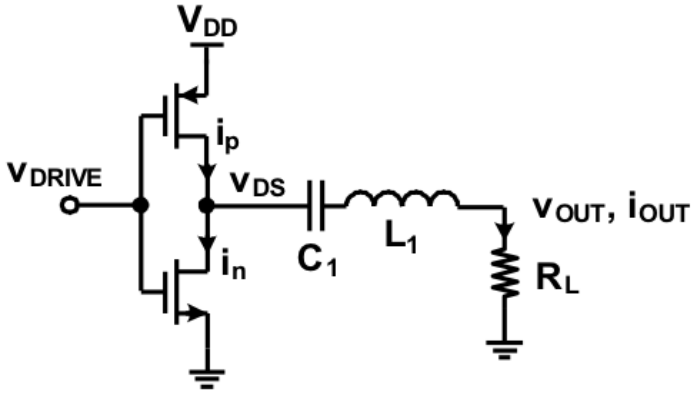


- In the figure right, the balun experiences the entire power delivered by the PA to the load, dissipating substantial power.
- For example, if the PA output reaches 1 W, then a balun loss of 1.5 dB corresponds to 300 mW. The TX efficiency therefore degrades more significantly in the latter case.

PA-classes

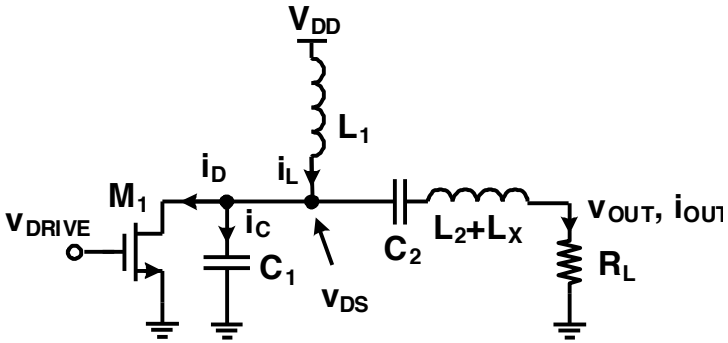


class-A/AB/B/C (linear)

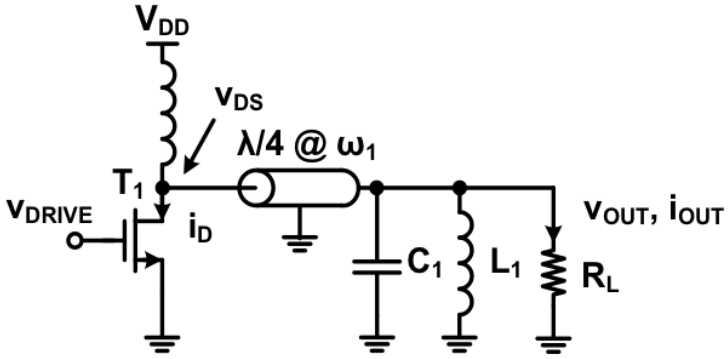


inverter-based class-D (switched)

class-E (switched)

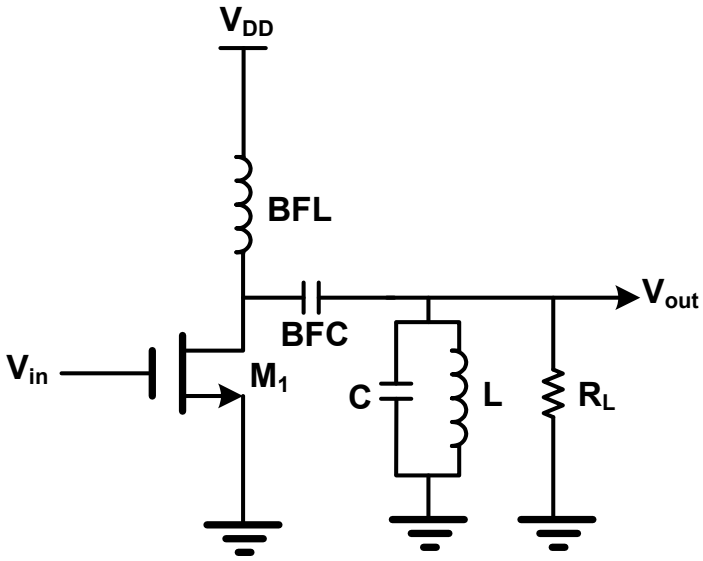


class-F (switched)



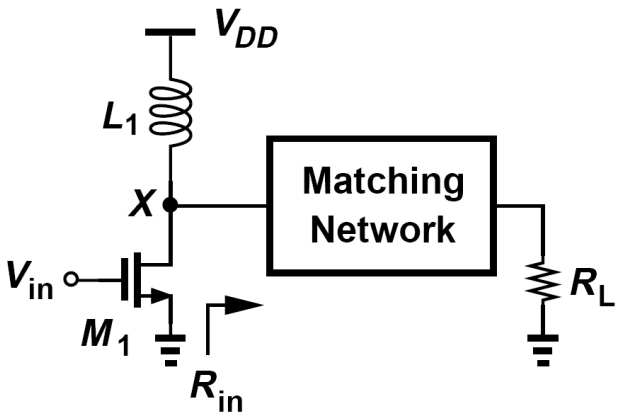
The linear classes A to C PAs

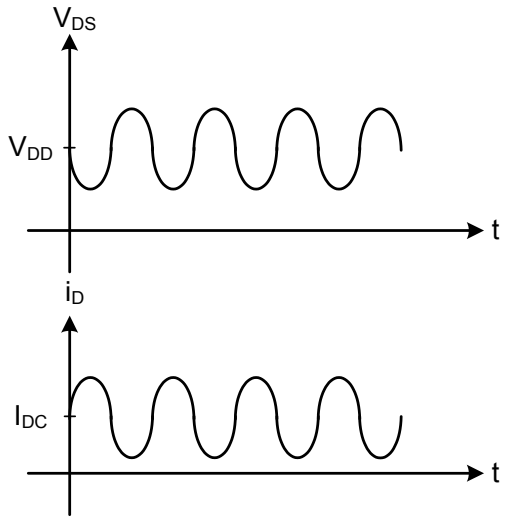
- Output power delivered to R_L.
- A “big fat” inductor (BFL) feeds DC power to the drain. It is big enough to create a constant current.
- BFC prevents DC dissipation in the load.
- The tank absorbs the parasitics of the transistor.
- LC tank filters out of band emissions created by non-linearities in the transistor.
- Different gate-biases => linear class A, AB, B, C.



Class A

- Since BFL presents a DC short, the drain voltage (which is the sum of DC and the signal voltage) has a symmetrical swing around V_{DD}.
- The drain voltage and current has a 180° phase difference.
- The product of drain current and voltage is positive; the transistor always dissipates power.

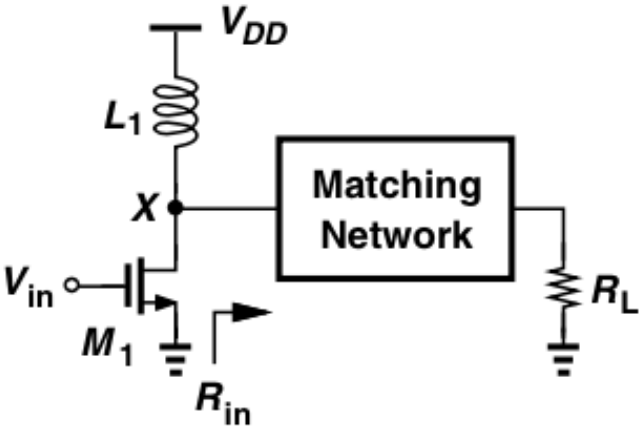


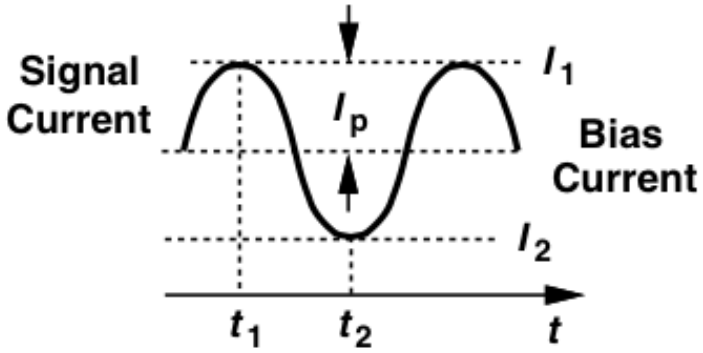


Class A

- Device biased to ~ $I_{max}/2$ to never switch off.
- Good linearity.
- Efficiency <= 50 %.
- V_x swings up to 2 x V_{DD} and the peak drain current is $2V_{DD}/R_L$. The device must be able to manage this stress!

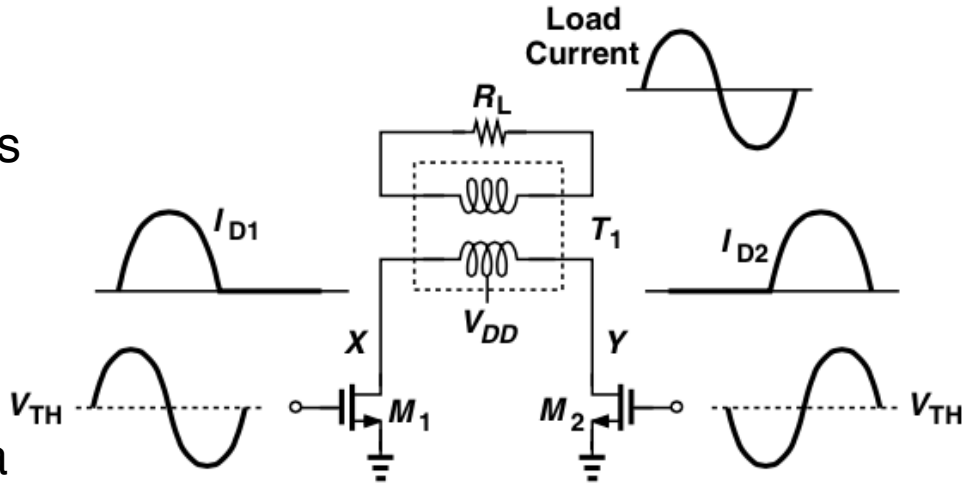
$$\eta = \frac{V_{DD}^2/(2R_{in})}{V_{DD}^2/R_{in}} = 50\%.$$





Class B

- Gate is typically biased to V_{TH}. The transistor will be switched off half of the time.
- The traditional class B PA employs two parallel stages each of which conducts for only 180°, thereby achieving a higher efficiency than the class A counterpart.
- This can also be achieved using a differential design + transformer.
- The efficiency can be up to π/4 (~79 %).



Class AB

- In a class A amplifier, the device conducts 100 % of the time, and in a class B, it conducts 50 % of the time.
- A class AB amplifier is something in-between; the device conducts between 50 % and 100% of the time.
- The efficiency and the linearity are intermediate between a class A and class B amplifier.
- Due to these trade-offs, class AB power amplifiers are popular in many applications.

Conduction angle

- When gate-bias is lowered, the transistor will be off for a part of the period. This changes the properties of the amplifier, the "class".

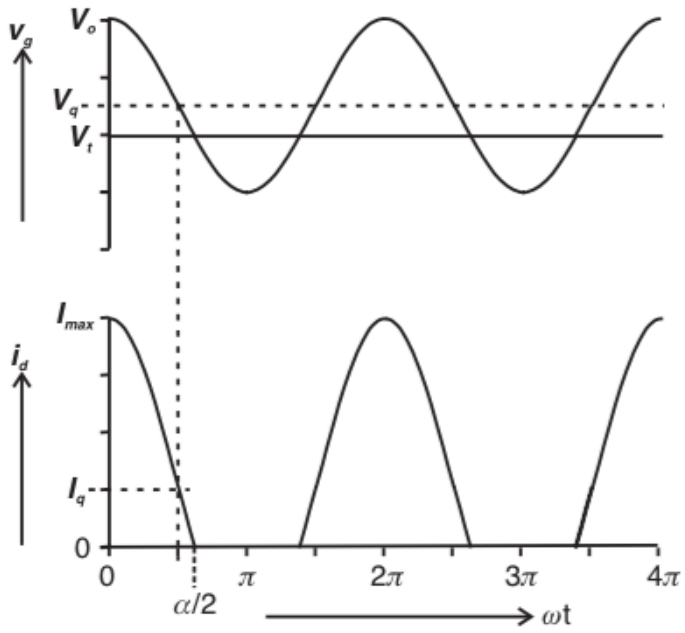
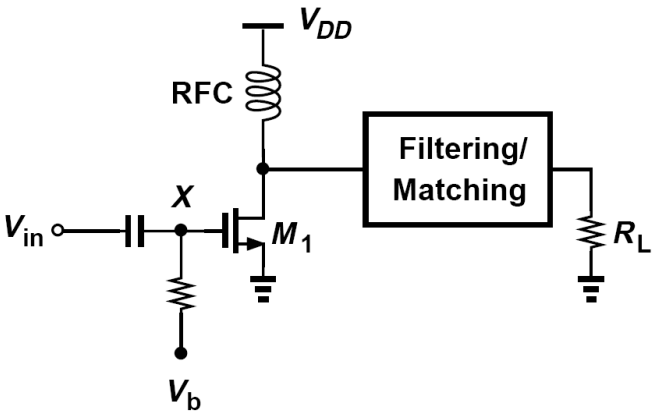


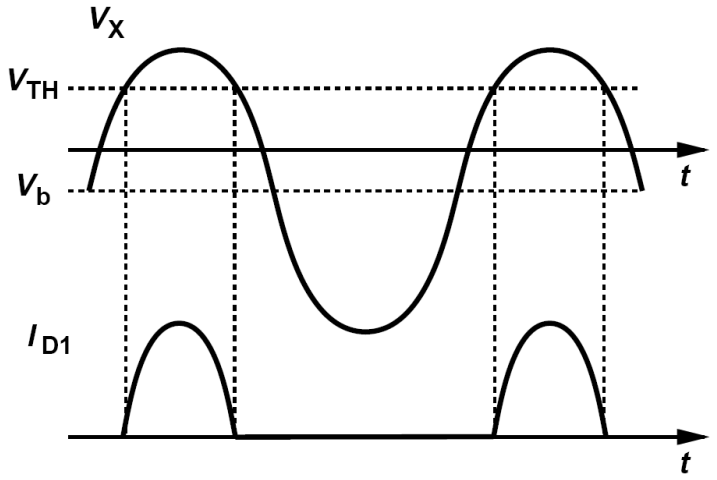
Table 3.1 Classical Reduced Conduction Angle Modes

Mode	*Bias Point (Vq)*	*Quiescent Current*	*Conduction Angle*
A	0.5	0.5	2π
AB	0–0.5	0–0.5	π–2π
B	0	0	π
C	< 0	0	0-π

Class C

- In a class C power amplifier, the time in which the transistor conducts is decreased to less than half period.
- The drain current consists of a periodic train of pulses, which can be approximated by the top pieces of a sine wave



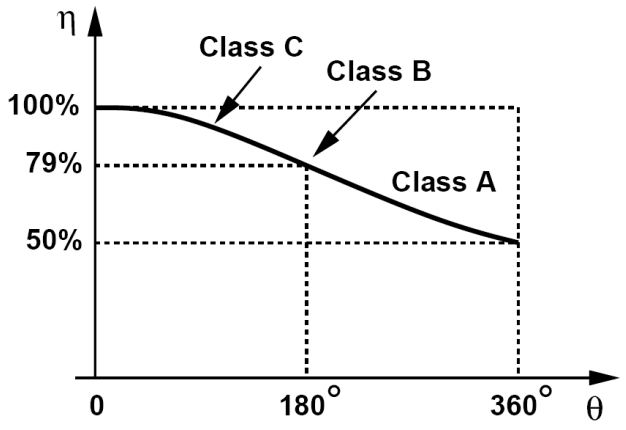


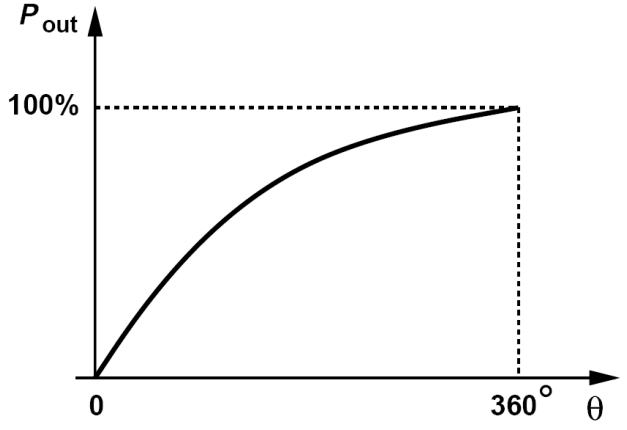
Class C

- The drain efficiency can be determined as:

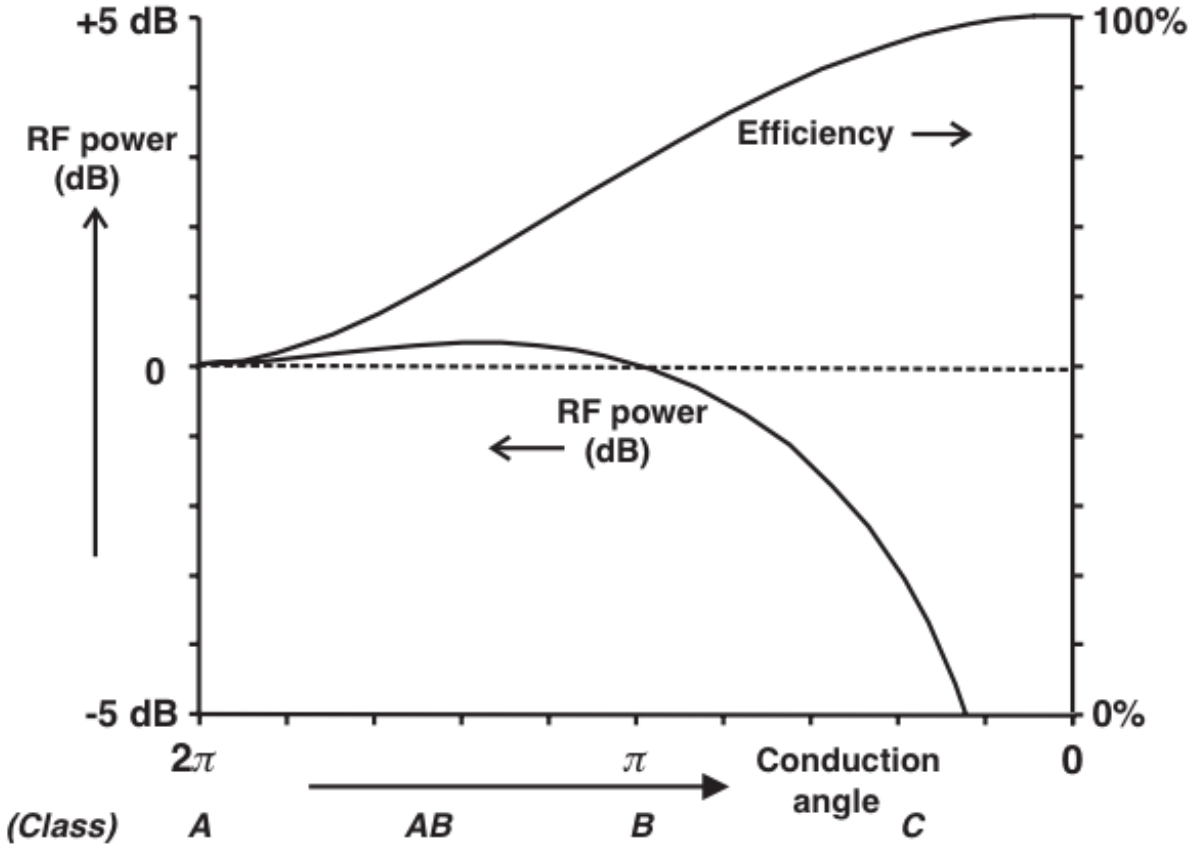
$$\eta = \frac{1}{4}\frac{\theta - \sin\theta}{\sin(\theta/2) - (\theta/2)\cos(\theta/2)}$$

- Efficiency of 100 % as θ approaches zero.
- P_{out} falls to zero as θ approaches zero.





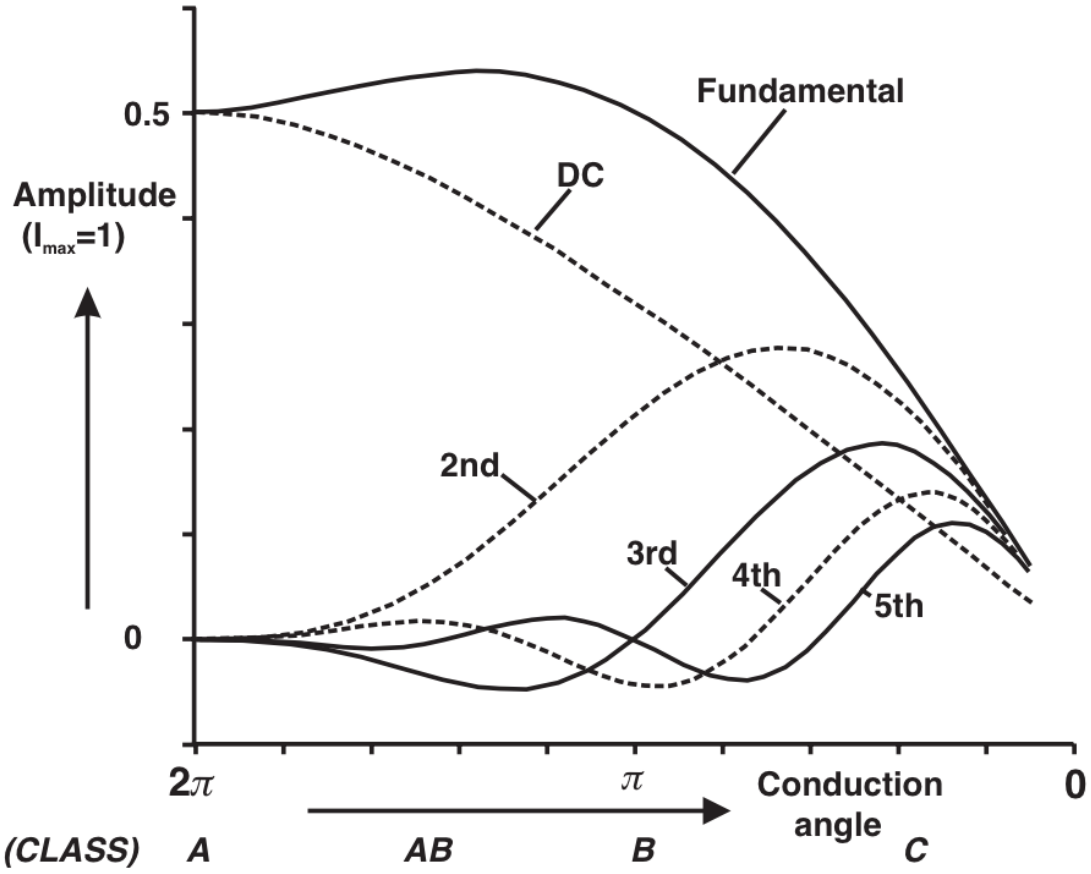
Linear PAs (A, AB, B, C)



RF power (relative to Class A) and efficiency as a function of conduction angle; optimum load and harmonic short assumed.

S. Cripps, "RF Power Amplifiers for Wireless Communications", 2nd ed, 2006.

Linear PAs (A, AB, B, C)

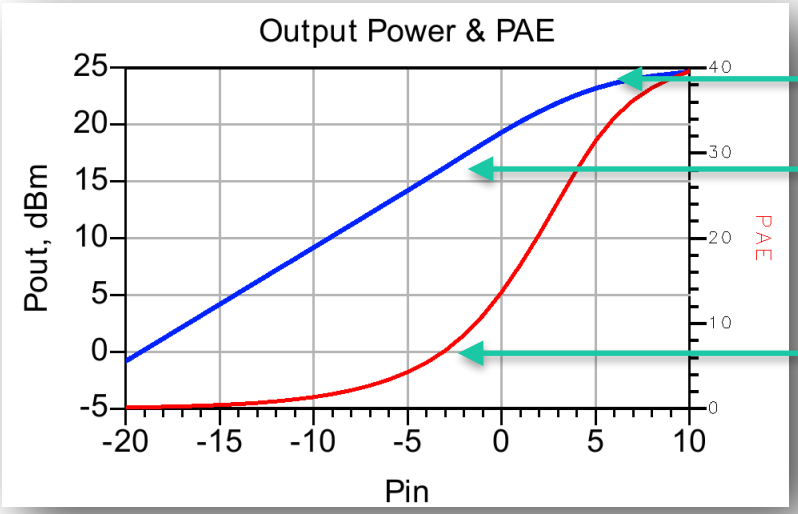


Fourier analysis of reduced conduction angle current waveforms.

S. Cripps, "RF Power Amplifiers for Wireless Communications", 2nd ed, 2006.

Efficiency with modulated signals

- When input signal (swing) is reduced, the efficiency for linear PAs drops fast (PAE).



maximum linear peak power

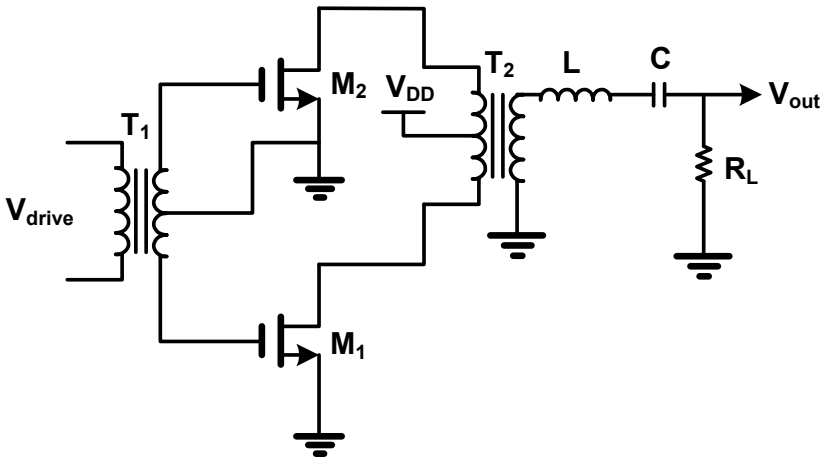
average linear power

average power efficiency

- WLAN 11ac uses OFDM, which has high PAPR (about 8 dB) => average output power and efficiency becomes very low with modulated signals.

Class D

- An ideal switch does not dissipate any power because there is either zero voltage across it or zero current through it.
- For this reason, implementing PA based on switching property of a device can provide a 100 % efficiency.
- Class D PAs explores this idea, e.g. using two switches.
- M_1 and M_2 are behaving as switches, ideally dissipating no power.

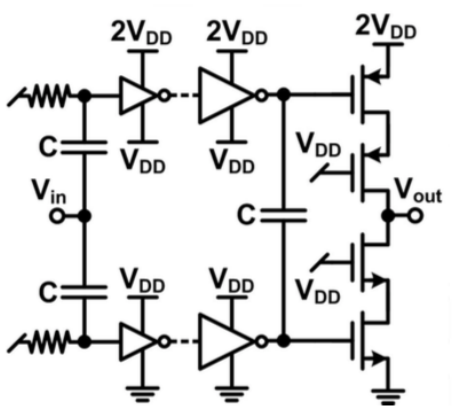


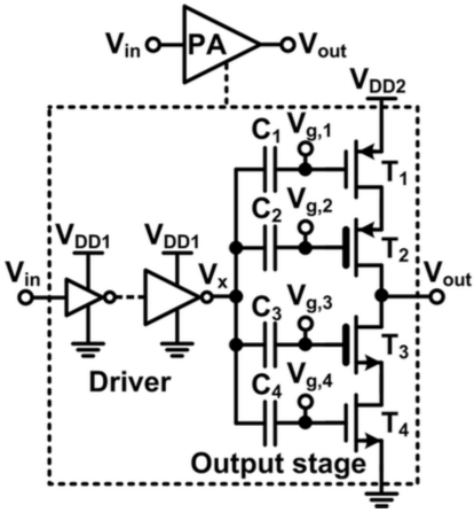
Class D

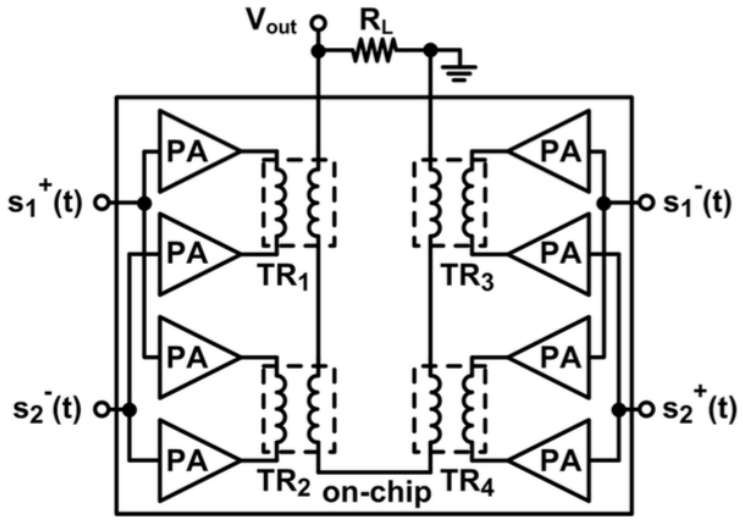
- Historically, low switching speed, therefore mostly used in audio applications (also integrated in CMOS for mobile phones).
- Recently, applied with CMOS for PAs.
- Switch is now a CMOS inverter (a chain of).
- Modulation can be done by *out-phasing* or by switching banks of smaller PA elements on/off

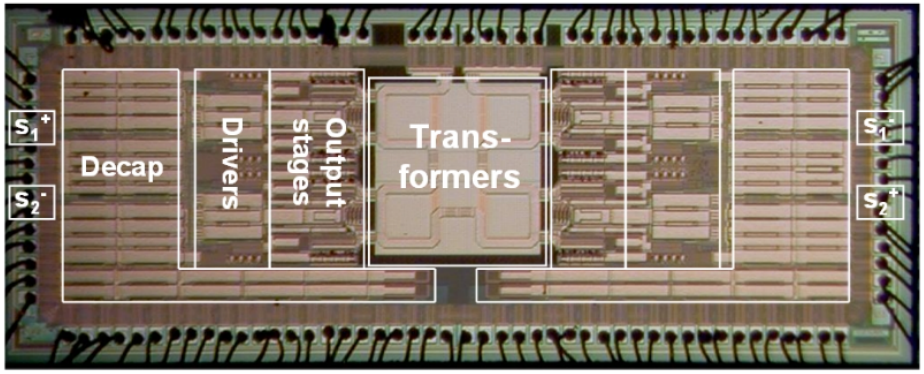
Class D

Fritzin et al., 2010, 2011







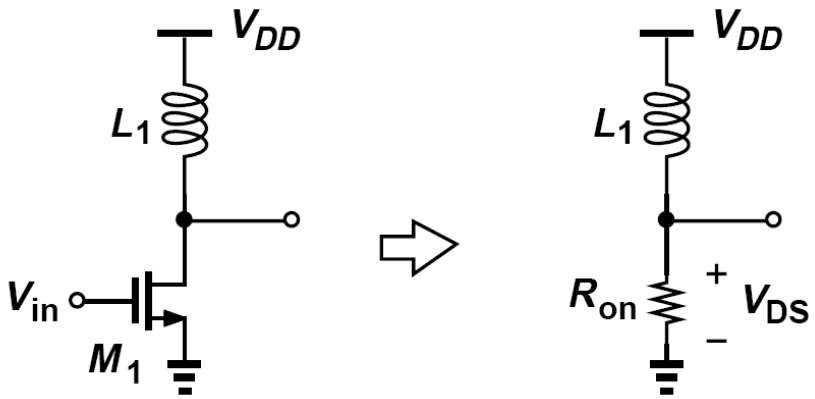


Ref., Year	P_{out} [dBm]	V_{DD} [V]	DE [%]	PAE [%]	f [GHz]	Tech. [nm]	BW [GHz]
[4] 2010	+21.6	1.9	64.0	52.0	1.92	130	0.3[a]
[2] 2010	+25.1	2.0	-	40.6	2.40	32	1.0[a]
[3] 2011	+25.2	2.5	-	55.2	2.25	90	1.0[b]
[1] 2009	+28.1	2.4	-	19.7	2.25	45	0.6[b]
This work	**+32.0**	**5.5**	**20.1**	**15.3**	**1.85**	**130**	**0.9[b]**

(a) 1 dB bandwidth (BW)
(b) 3 dB bandwidth (BW)

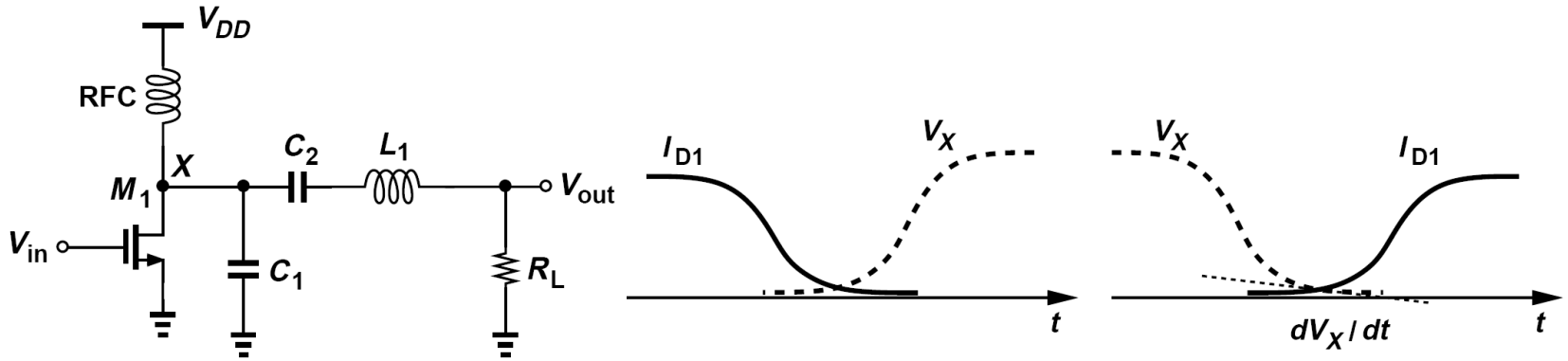
The transistor as a switch

- Operate the output transistor as switch, "on/off"!
- We can achieve 100 % efficiency if:
  1. M_1 sustains a small voltage when it carries current
  2. M_1 carries a small current when it sustains a finite voltage,
  3. the transition times between on/off states are minimized



Class E

- Output matching: the switched transistor is not a current source, as in the class A-C amplifiers.
- In class E amplifiers, higher order networks for the load are used to create freedom to shape the switch voltage to have zero voltage and zero slope when it turns on.



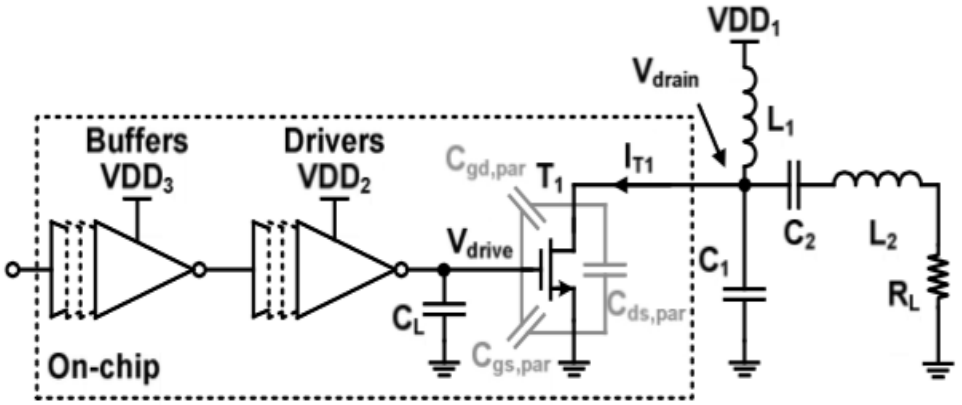
Class E

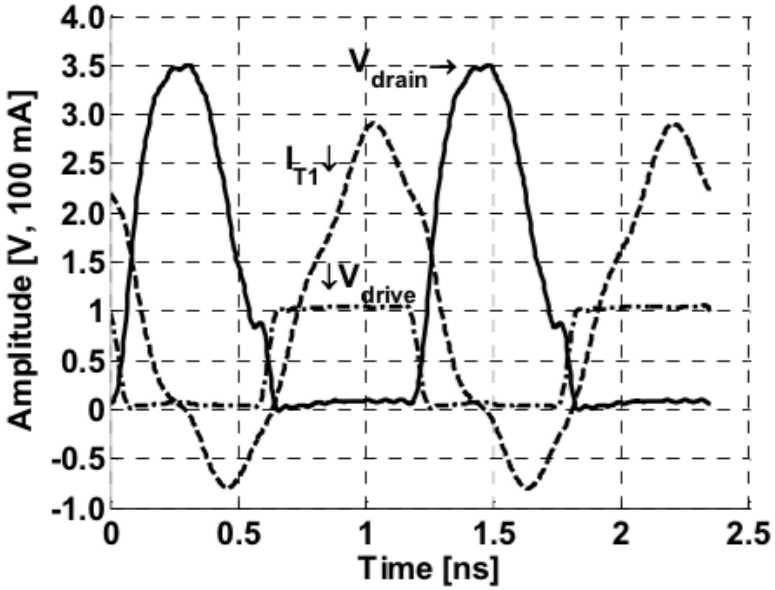
- Turn-off losses reduce the efficiency and degrade the power capability.
- Losses in the output network also reduce the efficiency.

- Because of high stress on devices (3.5 x V_{DD}), they are not suitable for scaling trends toward low-power and low breakdown voltages in advanced processes.
- But the class E amplifier can be improved (finite L to V_{DD}) to only have about 2.5 x V_{DD}.

Class E in 130 nm CMOS

Fritzin et al., 2010

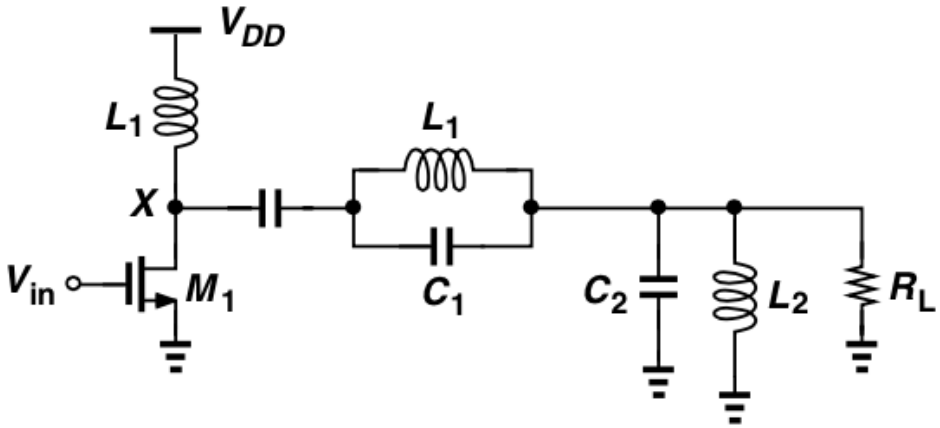


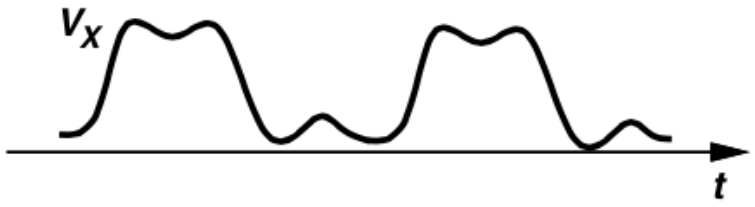


	Simulations	Measurements
f [MHz]	850	850
VDD_1 [V]	1.4	1.4
Pout [dBm]	+22.6	+22.2-22.8
DE [%]	61	57-60

Class F

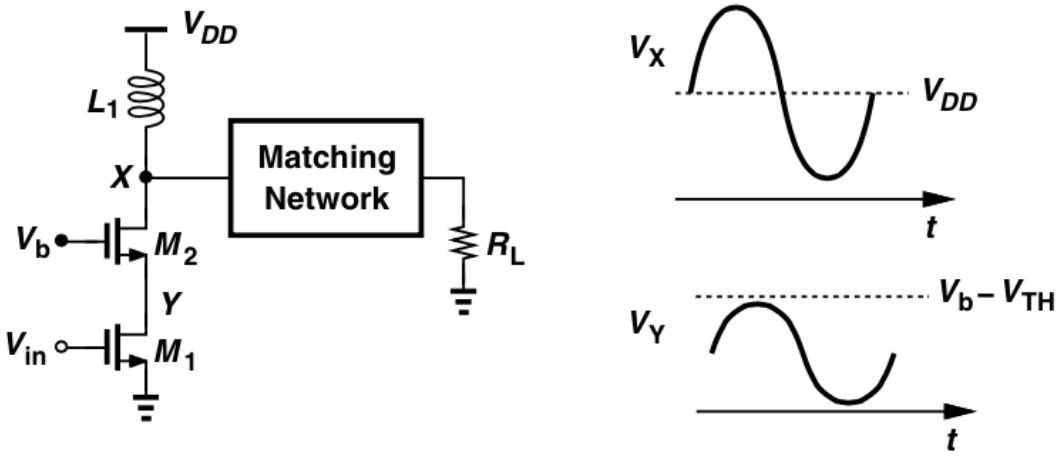
- To overcome the problems of class E, harmonic termination (typically 2nd + 3rd harmonic) can be used to create sharper switching.
- Called class F amplifier.
- A transmission line is typically used for discrete devices, but for IC, LC tanks are used.





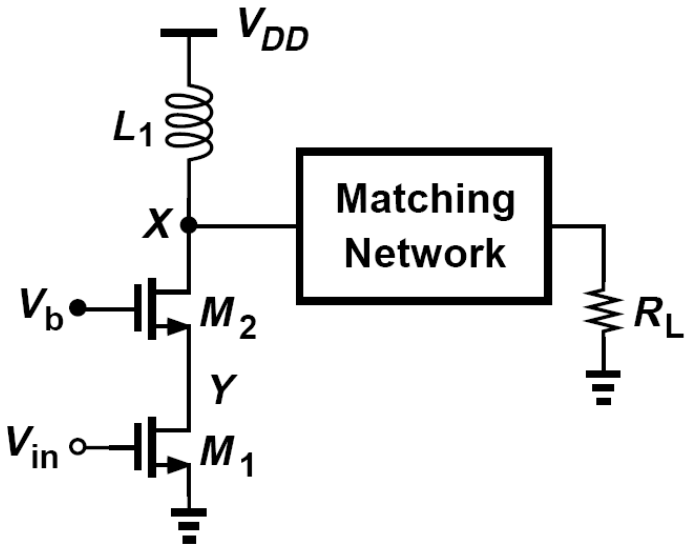
Higher supply: cascode stage

- With a cascode, we can operate the PA at higher supply voltage => high P_{out}.
- The voltage stress on the devices will be relaxed; the cascode device “shields” the input transistor as V_x rises, keeping the drain-source voltage of M_1 less than V_b-V_{TH2}.



Example 12.14

- Determine the maximum terminal-to-terminal voltage differences of M_1 and M_2 in a cascode stage. Assume V_{in} has a peak amplitude of V_0 and a dc level of V_m, and V_X has a peak amplitude of V_p (and a dc level of V_{DD}).



Example 12.14

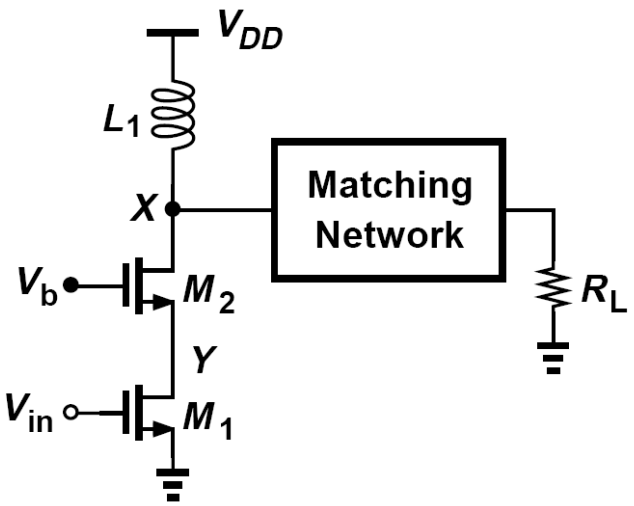
- Transistor M1 experiences maximum V_{DS} as V_{in} falls to V_m - V_0. If M_1 nearly turns off, then $V_{DS1} \approx V_b$ - V_{TH2}, $V_{GS1} \approx V_m$ - V_0, and $V_{DG1} = V_b$ - V_{TH2} - (V_m - V_0). For the same input level, the drain voltage of M_2 reaches its maximum of $V_{DD} + V_p$, creating

$$V_{DS2} = V_{DD} + V_p - (V_b - V_{TH2})$$

and

$$V_{DG2} = V_{DD} + V_p - V_b$$

- Also, the drain-bulk voltage of M_2 reaches V_{DD} + Vp.



Higher supply: cascode

- Cascodes with more stacked devices.
- Limited by max drain-substrate voltage on uppermost transistor.
- Need careful "internal" matching (C2-C4).
- In practice limited to 3-4 stacked devices.

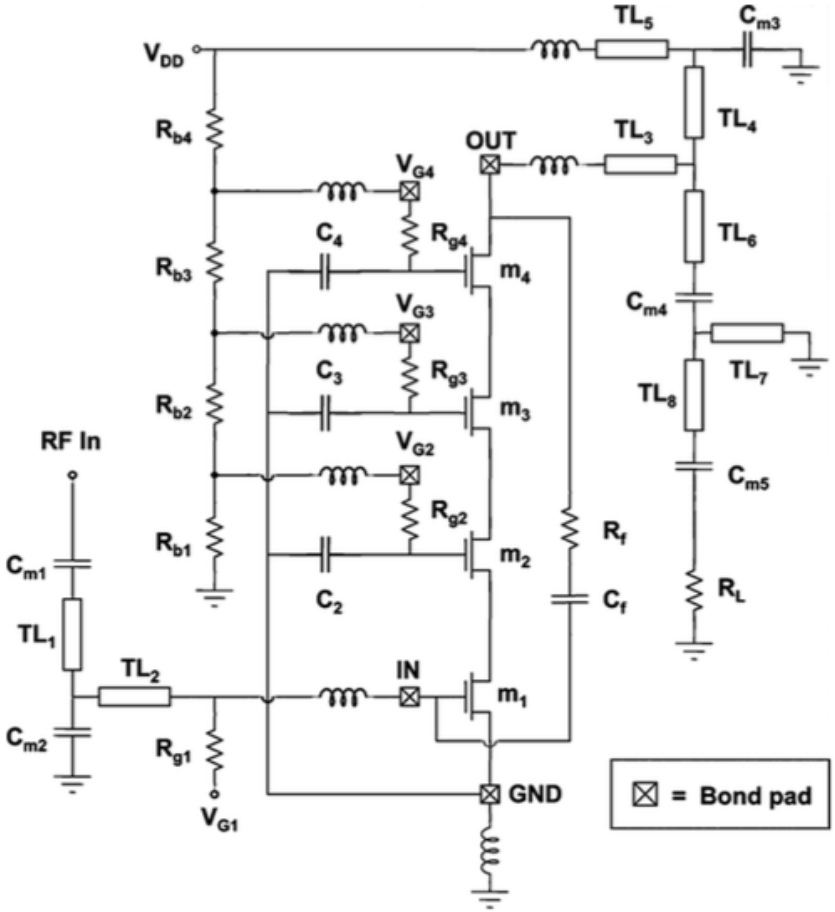
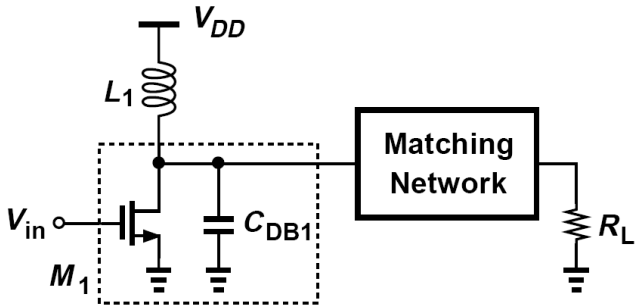
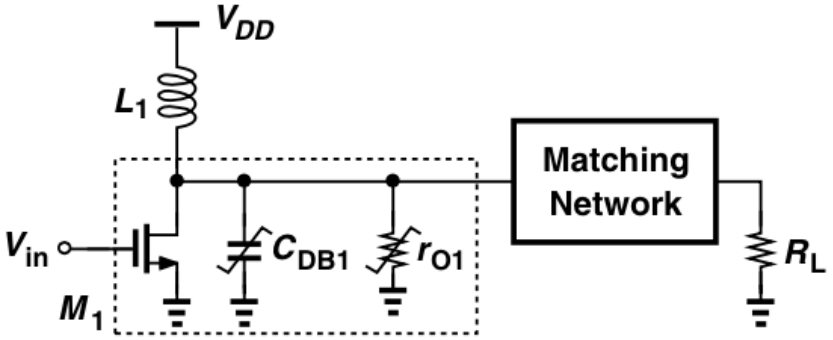


Fig. 3. Circuit schematic of the single-stage stacked-FET PA.

Large signal matching

- PA input is mainly linear => matching network can be designed using conjugate matching.
- PA output resistance AND cap varies with signal => conjugate matching does not work.
- AND (shown in book (12.60)-(12.62)), matching for maximum power transfer does not correspond to maximum efficiency!





Large signal matching

- For the general case of a nonlinear complex output impedance, a small-signal approximation of the impedance in the midrange of the output voltage and current can be used to obtain rough values for the matching network components.
- Modifying these values for maximum large-signal efficiency requires a great deal of trial and error, especially if the package parasitics must be taken into account.

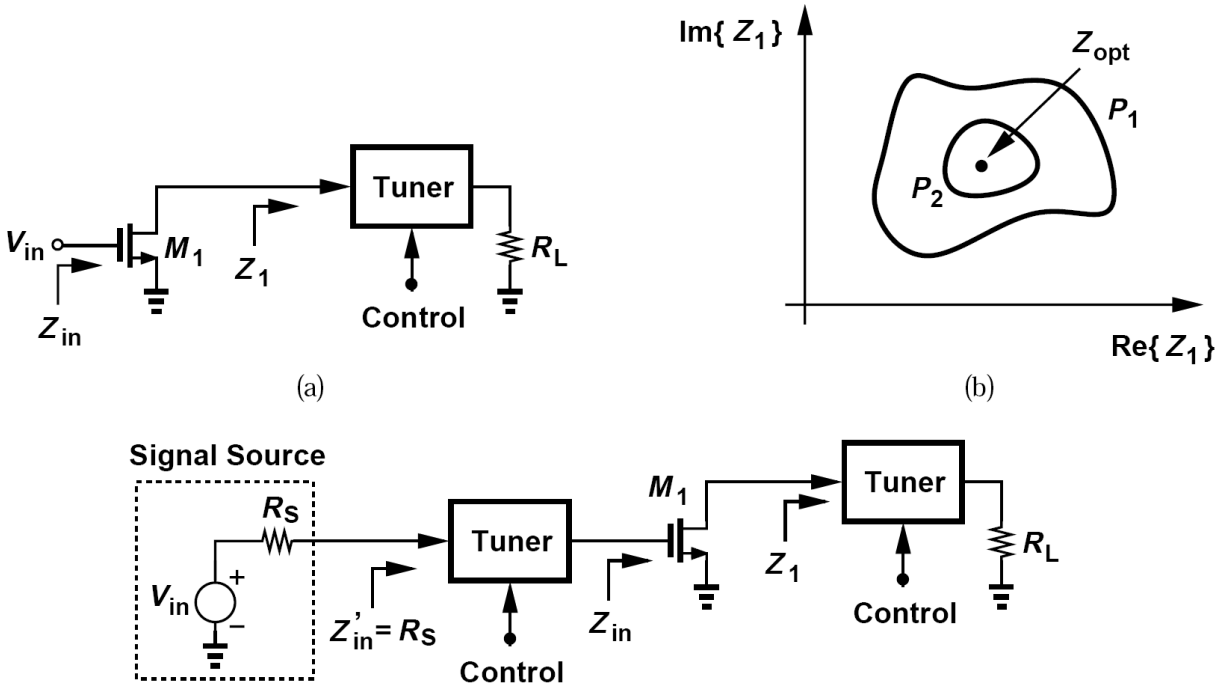
15.2 GENERAL CONSIDERATIONS

Contrary to what one's intuition might suggest, the maximum power transfer theorem is largely useless in the design of power amplifiers. One minor reason is that it

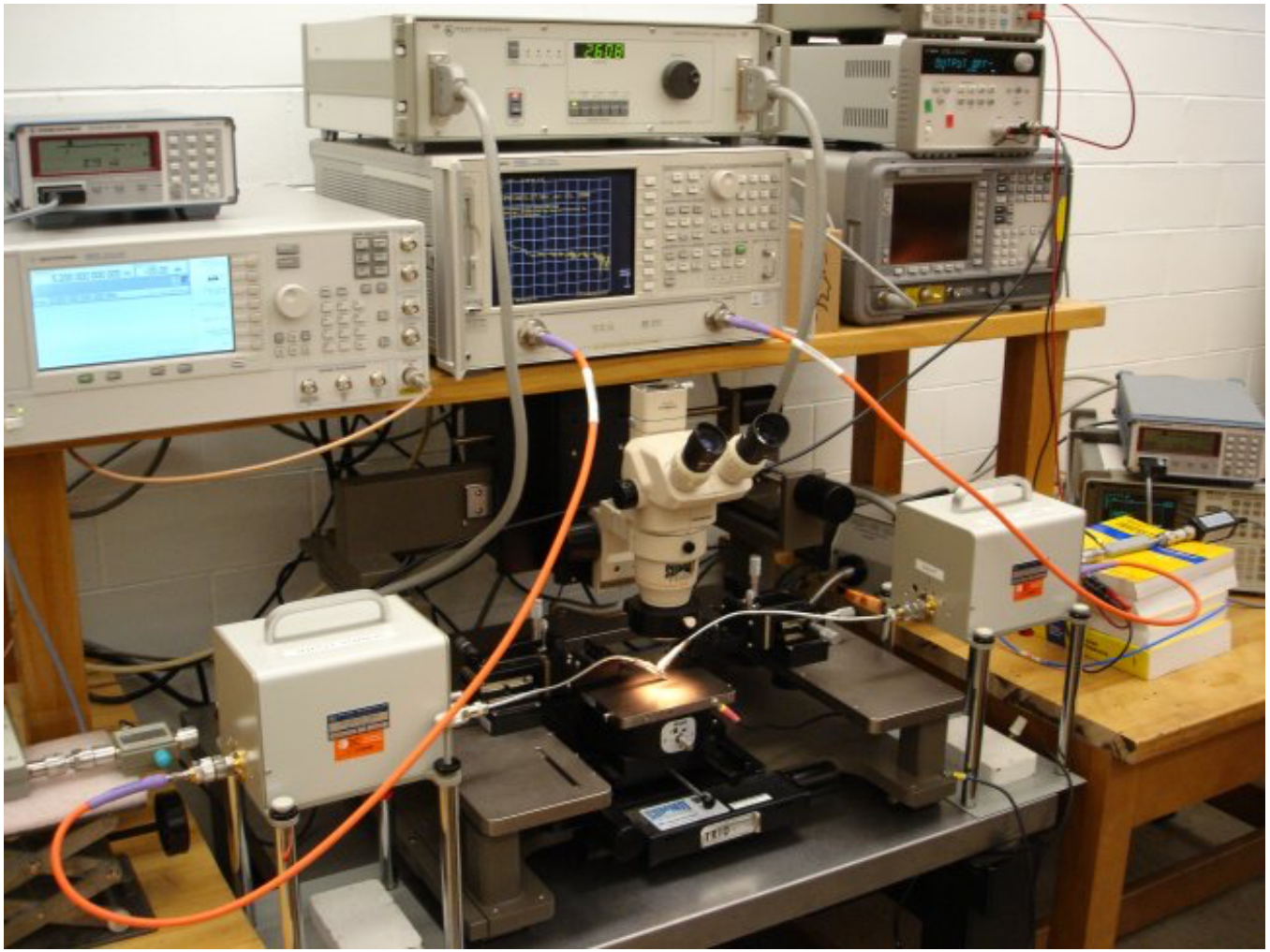
Lee's book

Load-pull measurements

- To find optimum load and source impedances, load-pull measurements are performed.



Load-pull measurements



Load-pull measurements

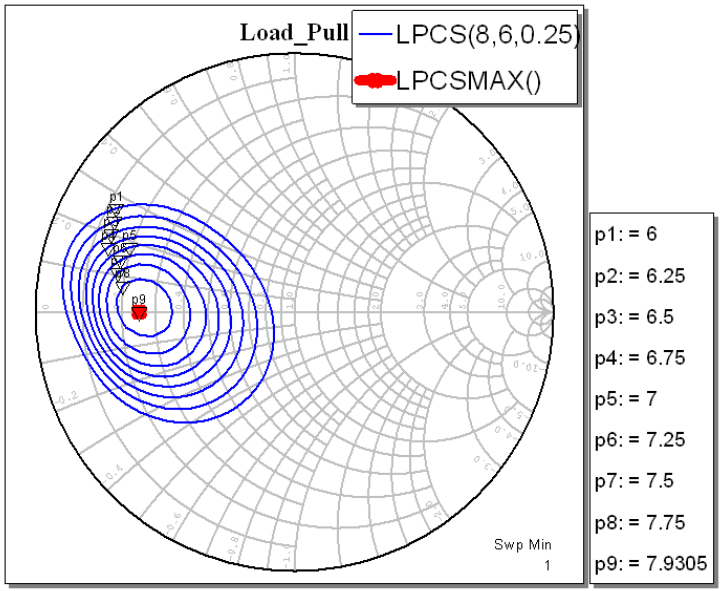


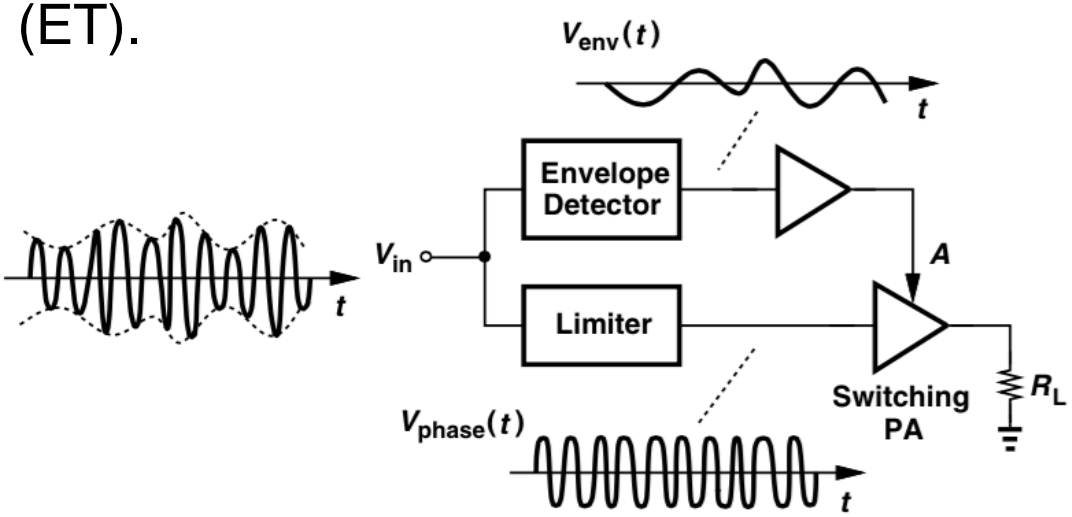
TABLE II
SUMMARY OF 2.45 GHZ RESULTS

V_D [V]	I_{DQ} [mA]	Γ_S	Γ_L	G_T [dB]	P_{SAT} [dBm]	PAE [%]
3.3	150	0.90 / 172°	0.82 / 162°	19.5	26.5	52
3.3	448	0.87 / 175°	0.83 / 171°	15.8	28.4	43
5.0	500	0.90 / 170°	0.83 / 168°	18.9	30.5	40

Johansson et al., 2013

Polar modulation

- Any bandpass signal can be represented as $V_{in}(t) = V_{env}(t) * \cos[\omega_0 t + \phi(t)]$, we can decompose $V_{in}(t)$ into an envelope signal and a phase signal, amplify each separately, and combine the results at the end.
- Polar modulation, envelope elimination and restoration (EER), envelope tracking (ET).

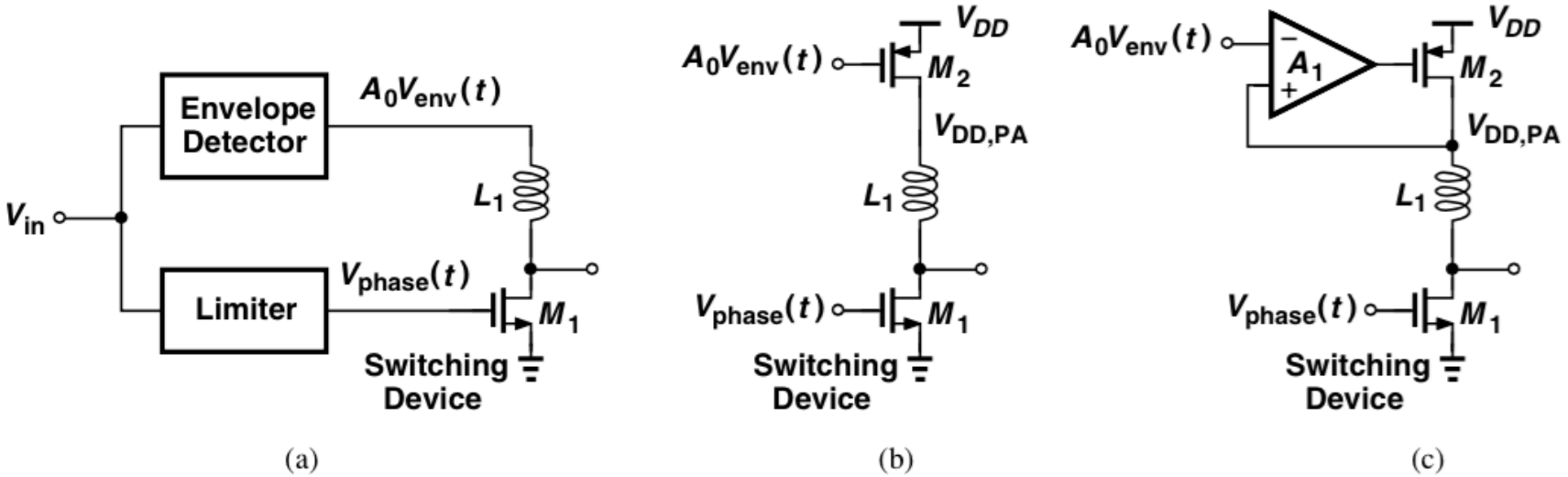


Polar modulation

(a) The large current flowing through this stage requires a buffer in this path, but efficiency considerations demand minimal voltage headroom consumption by the buffer.

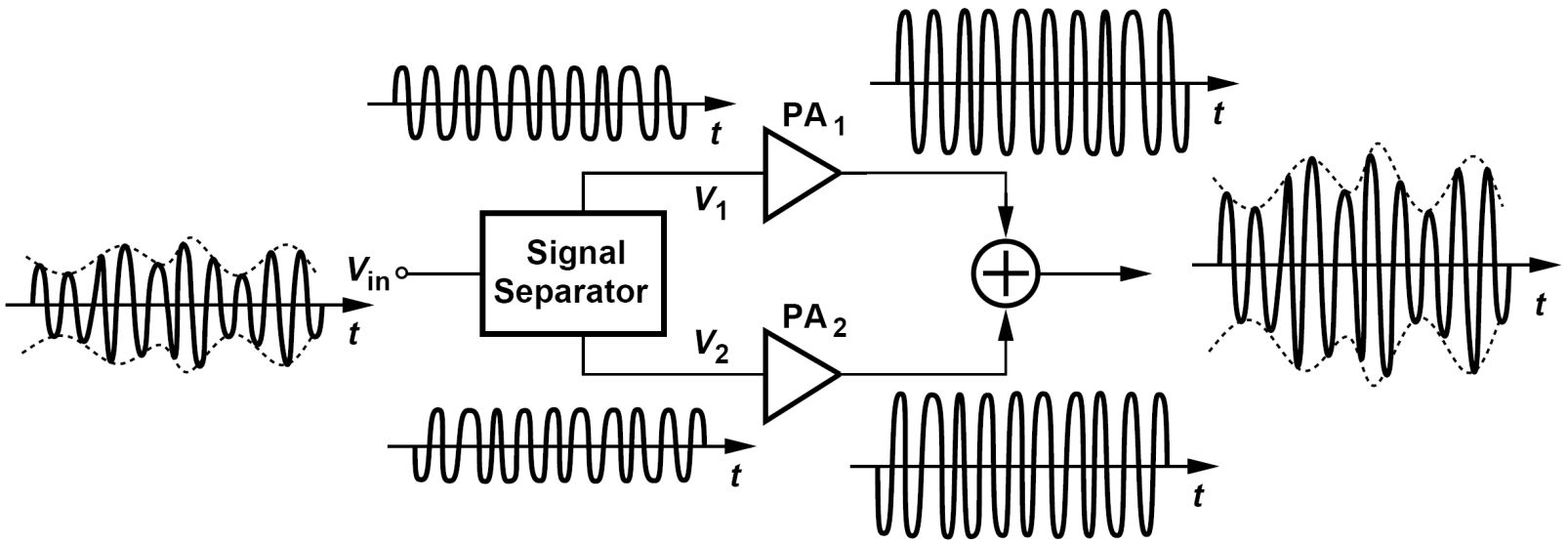
(b) No guarantee that VDD,PA tracks $A_0V_{env}(t)$ faithfully.

(c) Stage is modified to a closed-loop control .



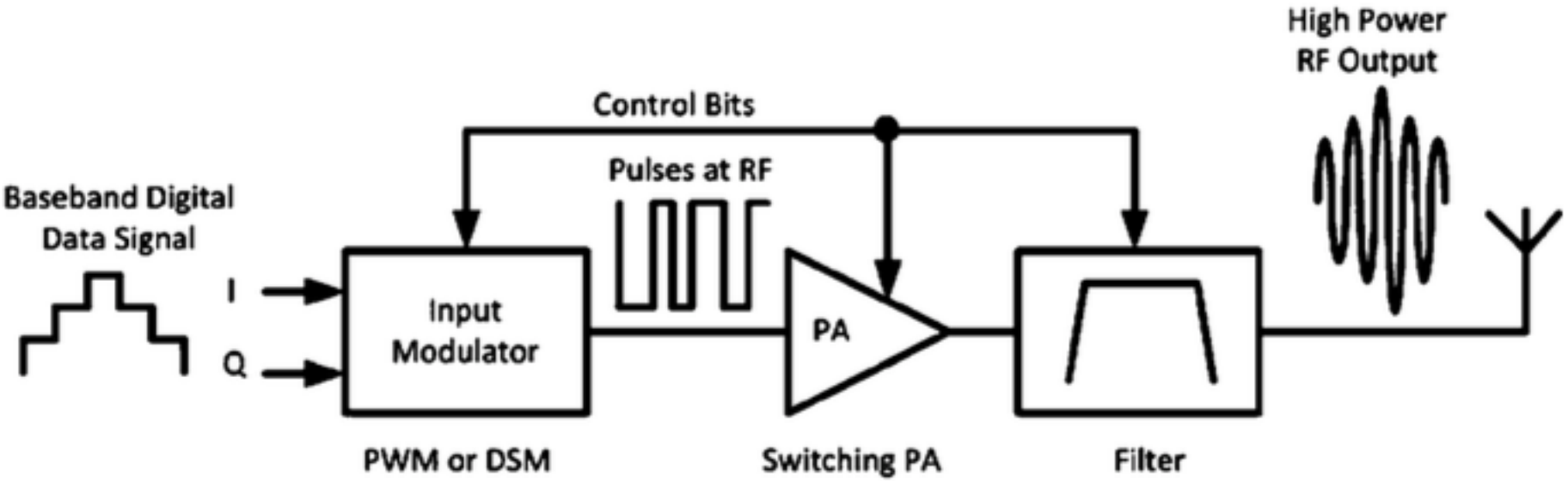
Outphasing

- It is possible to avoid envelope variations in a PA by decomposing a variable-envelope signal into two constant-envelope waveforms.
- Outphasing, "linear amplification with nonlinear components (LINC)", Chireix.



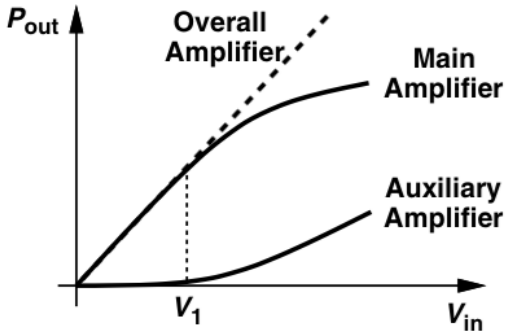
Pulse-width modulation

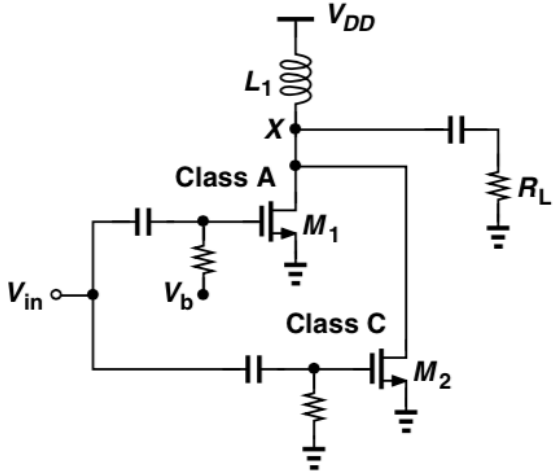
- Conventional PWM can be adopted for RF.
- It is also possible to do the PWM at IF and upconvert it to RF.
- Research (PhD student Fahim Ul-Haque) @ LiU for CMOS-IC.



Doherty amplifier

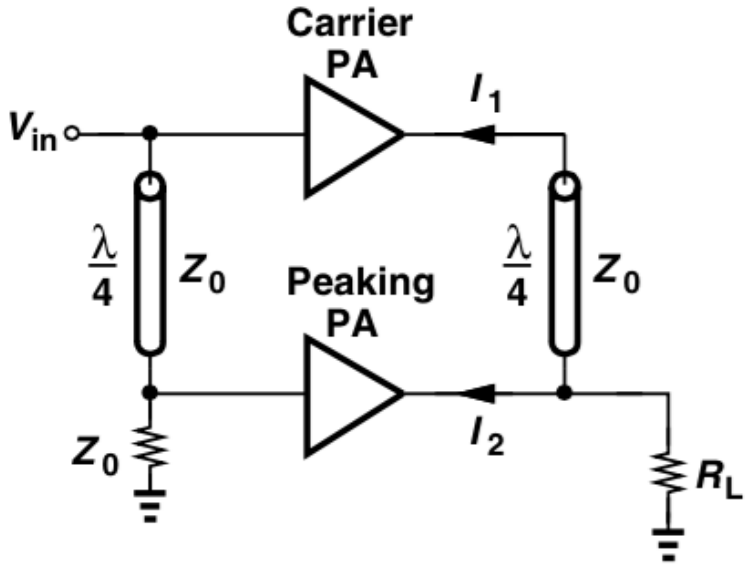
- If an auxiliary transistor is introduced that provides gain only when the main transistor begins to compress, then the overall gain can remain relatively constant for higher input and output levels.
- Almost all basestation amplifier designs use Doherty to increase the efficiency.
- Linearity is not so good, but fixed with pre-distortion.

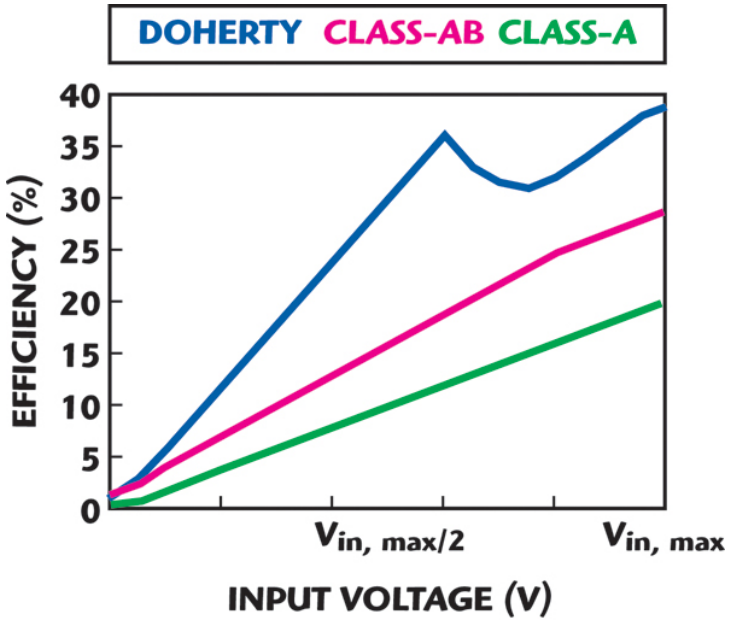




Doherty amplifier

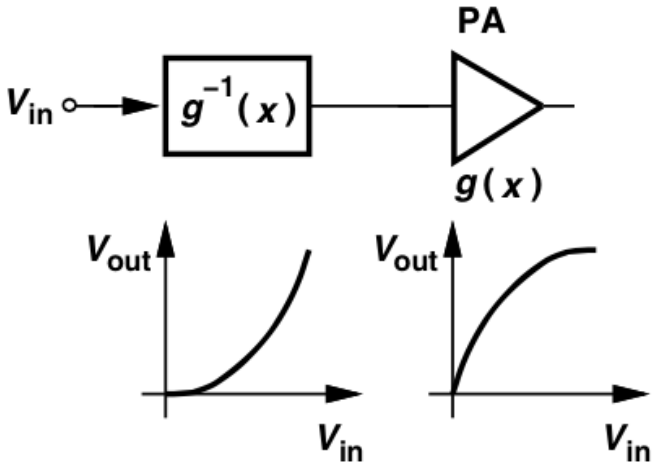
- Implementation requires λ/4 delay line, which is tricky to implement on-chip without losses, and may be too large at lower frequencies.
- Main advantage: better efficiency in the "back-off" region.

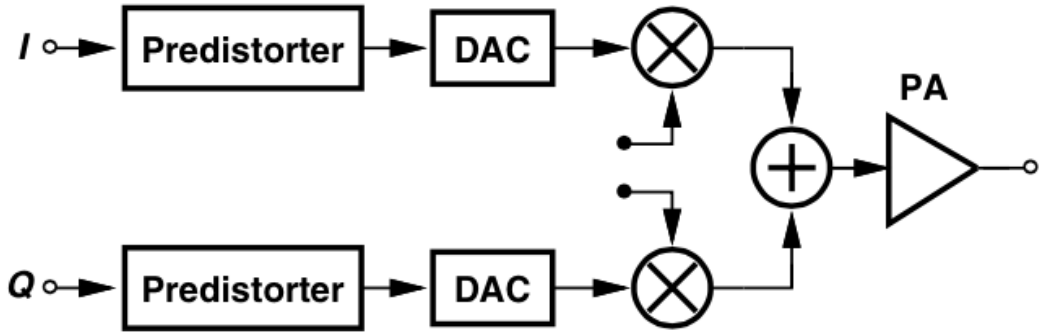




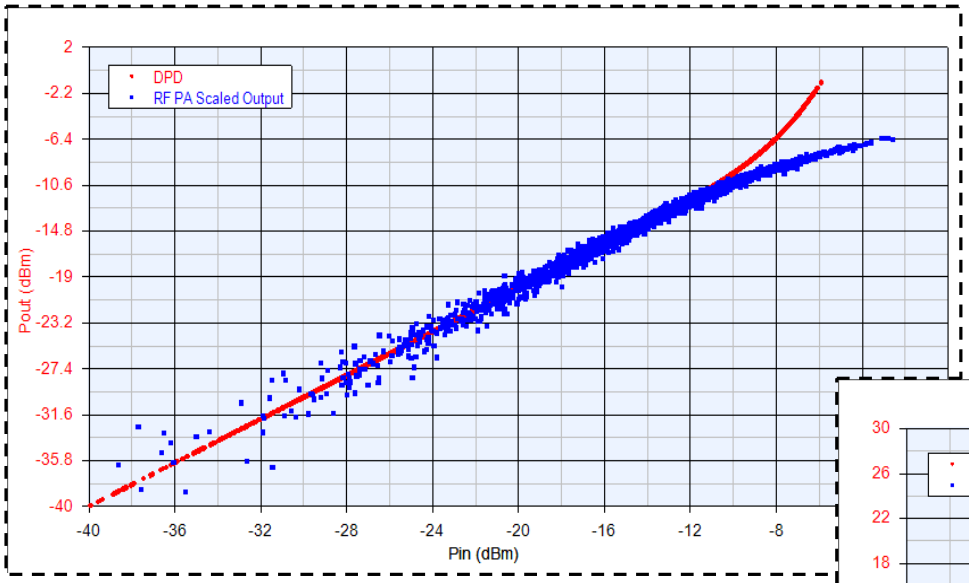
Pre-distortion (DPD)

- There are many linearization techniques, the most popular (especially in basestations) is pre-distortion.

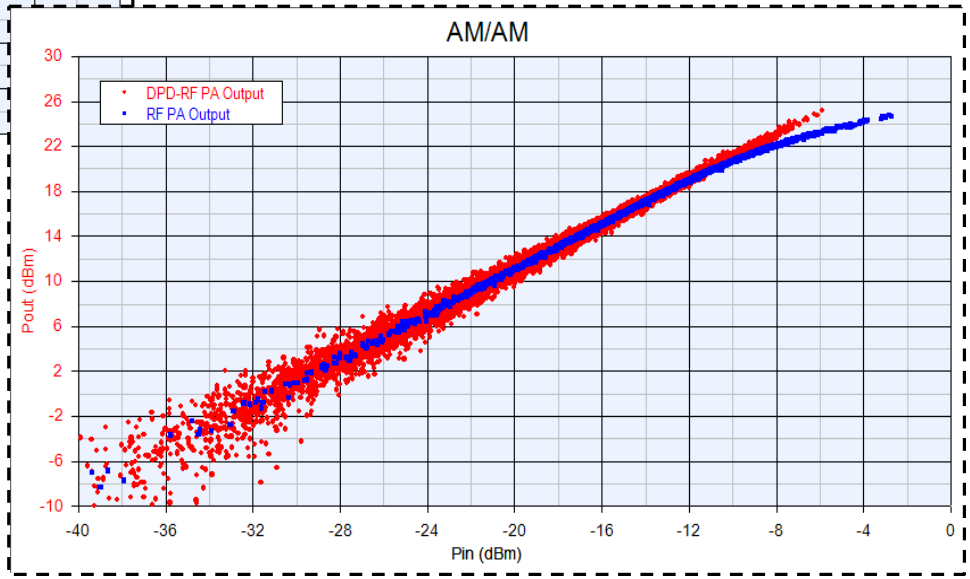




Pre-distortion (DPD)



Blue = undistorted
Red = added distortion



Blue = undistorted
Red = resulting after adding