Solutions to
Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date:	Mars 10, 2004
Time:	14 – 18
Place:	KÅR
Max. no of points:	70; 50 from written test, 5 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design. Dictionaries.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Large-signal analysis

The circuit in the figure is to be used in an analog circuits.

a) Derive the voltage V_x as a function of the output voltage, but not as a function of the input voltage. Hint: $I_{R1} = I_{R2}$.

The current through the resistors are

$$I_{R1} = V_x/R_1 \tag{1.1}$$

$$I_{R2} = (V_{DD} - V_{out})/R_2 \tag{1.2}$$

where the voltage V_x is the voltage at the source of the transistor. These current should be equal which results in the expression for the output voltage as

$$V_x = \frac{R_1}{R_2}(V_{DD} - V_{out}) \tag{1.3}$$

b) Derive the output voltage as a function of the input voltage when the transistor is saturated.

The currents through the transistors are given by Eq. (1.1) and Eq. (1.2). In the saturation region the current through the transistor is given by (when the bulk effect and channel-length modulation is neglected)

$$\begin{aligned} I_M &= \alpha(V_{GS} - V_T)^2 = \alpha(V_{in} - V_x - V_T)^2 \\ &= \alpha(V_A - V_x)^2 \end{aligned} \tag{1.4}$$

where V_x is the voltage at the source of the transistor and $V_A = V_{in} - V_T$. All the currents should be equal and we can for example use the Eq. (1.1), Eq. (1.3), and Eq. (1.4) to solve the voltage at node V_x. This voltage can than be converted to the output voltage by utilizing Eq. (1.3). First setting the right-hand side of Eq. (1.1) equal to the right-hand side of Eq. (1.4) gives

$$V_x/R_1 = \alpha(V_A - V_x)^2 \tag{1.5}$$

Solving for V_x in this equation gives after some manipulations

$$V_x = V_A + \frac{1}{2\alpha R_1} \pm \frac{1}{2\alpha R_1}\sqrt{1 + 4V_A\alpha R_1} \tag{1.6}$$

The positive solution is not correct since we know that the transistor is saturated, i.e., $V_{in} - V_x > V_T \Rightarrow V_A = V_{in} - V_T > V_x$. Hence, the V_x voltage is

$$V_x = V_A + \frac{1}{2\alpha R_1} - \frac{1}{2\alpha R_1}\sqrt{1 + 4V_A\alpha R_1} \tag{1.7}$$

The output voltage can be expressed as

$$V_{out} = V_{DD} - \frac{R_2}{R_1}V_x = V_{DD} - \frac{R_2}{R_1}\left(V_A + \frac{1}{2\alpha R_1} - \frac{1}{2\alpha R_1}\sqrt{1 + 4V_A\alpha R_1}\right)$$

c) Derive the output voltage as a function of the input voltage when the transistor is operating in the linear region.

The currents through the devices are given by

$$I_{R1} = V_x/R_1 \tag{1.8}$$

$$I_{R2} = (V_{DD} - V_{out})/R_2 \tag{1.9}$$

$$I_{D,\,linear} = \beta\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{1.10}$$

We know that the currents should be equal. This results in

$$(V_{DD} - V_{out})/R_2 = \beta\left[(V_{in} - V_x - V_T)(V_{out} - V_x) - \frac{(V_{out} - V_x)^2}{2}\right]$$

where

$$V_x = \frac{R_1}{R_2}(V_{DD} - V_{out}) \tag{1.11}$$

which results in

$$\frac{V_{DD} - V_{out}}{R_2} = \beta\left[\left(V_{in} - \frac{R_1}{R_2}(V_{DD} - V_{out}) - V_T\right)\left(V_{out}\left(1 + \frac{R_1}{R_2}\right) - \frac{R_1}{R_2}V_{DD}\right)\right] - \beta\frac{\left(V_{out}\left(1 + \frac{R_1}{R_2}\right) - \frac{R_1}{R_2}V_{DD}\right)^2}{2}. \tag{1.12}$$

d) Determine the input voltage, V_{in}, for which the transistor switches from operating in the saturation region to the linear region.

The voltage at node V_x equals

$$V_x = \frac{R_1}{R_2}(V_{DD} - V_{out}) \tag{1.13}$$

Further, in order for the transistor to operate just between the saturation and the linear region we know that

$$V_{DS} = V_{GS} - V_T \Rightarrow V_{out} - V_x = V_{in} - V_x - V_T \Rightarrow V_{out} = V_{in} - V_T \equiv V_A$$

Further, the current through the transistor in saturation and through the resistors are given by

$$I_D = \alpha(V_{GS} - V_T)^2 = \alpha(V_A - V_x)^2 = \alpha(V_{out} - V_x)^2 \tag{1.14}$$

$$I_{R1} = V_x / R_1 \tag{1.15}$$

$$I_{R2} = \frac{V_{DD} - V_{out}}{R_2} = \frac{V_{DD} - V_A}{R_2} \tag{1.16}$$

Combining Eq. (1.13), Eq. (1.14), and Eq. (1.16) gives

$$\frac{V_{DD} - V_{out}}{R_2} = \alpha\left(V_{out}\left(1 + \frac{R_1}{R_2}\right) - \frac{R_1}{R_2}V_{DD}\right)^2 \tag{1.17}$$

This equation can be reformulated to

$$V_{out}^2\left(1 + \frac{R_1}{R_2}\right)^2 - V_{out}\left(\left(1 + \frac{R_1}{R_2}\right)\frac{R_1}{R_2}V_{DD} + \frac{1}{\alpha R_2}\right) + \left(\frac{R_1}{R_2}\right)^2 V_{DD}^2 - \frac{V_{DD}}{R_2} = 0$$

2. Small-signal analysis

The transistor in the circuit shown in the figure is biased in the saturation region. Neglect the influence of all internal parasitics in the transistor.

a) Draw the small-signal model for the circuit. Do not neglect the bulk effect.

The small-signal model of the amplifier is shown in Figure 2.1

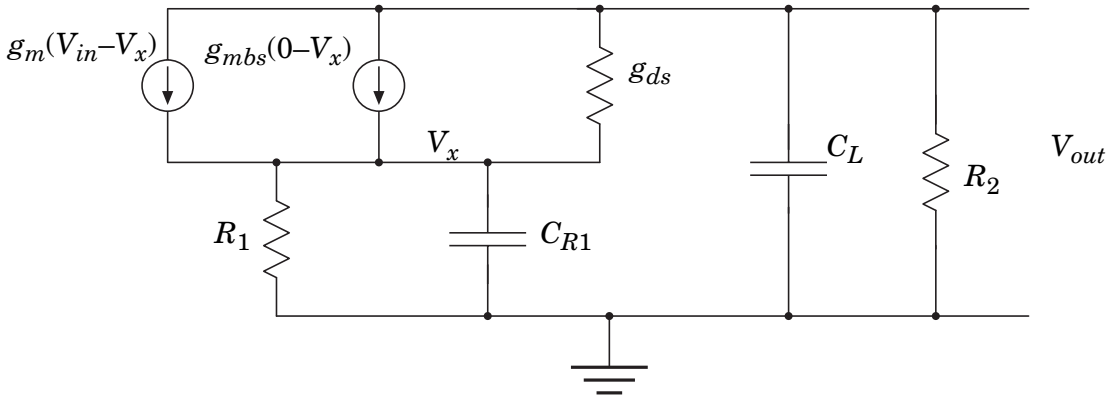

Figure 2.1 The small-signal model of the source-degenerated common-source amplifier.

b) Derive the transfer function of the circuit, i.e., $H(s) = V_{out}(s)/V_{in}(s)$.

Using nodal analysis of the circuit in the nodes V_x and V_{out} gives the equations

$$V_x(G_1 + sC_{R1}) + (V_x - V_{out})g_{ds} - g_m(V_{in} - V_x) - g_{mbs}(-V_x) = 0$$

$$(V_{out} - V_x)g_{ds} + g_m(V_{in} - V_x) + g_{mbs}(-V_x) + V_{out}(G_2 + sC_L) = 0$$

From the first equation we can solve for V_x. This results in

$$V_x = \frac{g_{ds}V_{out} + g_m V_{in}}{G_1 + g_{ds} + g_m + g_{mbs} + sC_{R1}} \tag{2.1}$$

Inserting this into the second equations gives

$$V_{out}(g_{ds} + G_2 + sC_L) + g_m V_{in} - (g_{ds} + g_m + g_{mbs})\frac{g_{ds}V_{out} + g_m V_{in}}{G_1 + g_{ds} + g_m + g_{mbs} + sC_{R1}} = 0$$

This can be simplified to

$$V_{out}(g_{ds}(G_1 + sCR_1) + (G_2 + sC_L)(G_1 + g_{ds} + g_m + g_{mbs} + sC_{R1})) + V_{in}g_m(G_1 + sC_{R1}) = 0$$

Hence, the transfer function is given by

$$\frac{V_{out}}{V_{in}} = -\frac{g_m(G_1 + sC_{R1})}{g_{ds}(G_1 + sC_{R1}) + (G_2 + sC_L)(G_1 + g_{ds} + g_m + g_{mbs} + sC_{R1})}$$
$$= -\frac{g_m(G_1 + sC_{R1})}{a + bs + cs^2} \tag{2.2}$$

where

$$\begin{aligned} a &= G_1 g_{ds} + G_2(G_1 + g_{ds} + g_m + g_{mbs}) \\ b &= C_{R1}(g_{ds} + G_2) + C_L(G_1 + g_{ds} + g_m + g_{mbs}) \\ c &= C_L C_{R1} \end{aligned} \tag{2.3}$$

c) Derive approximate expressions for the DC gain, first pole, second pole, zeros, and the output resistance as a function of, e.g., the small-signal parameters, resistances, and capacitances. Assume that $C_L \gg C_{R1}$ and $G_1, G_2 \gg g_m$

The DC gain is

$$A_0 = \left.\frac{V_{out}}{V_{in}}\right|_{s=0} = -\frac{g_m G_1}{a} \approx -\frac{g_m G_1}{G_1 G_2} \approx -\frac{g_m}{G_2} \tag{2.4}$$

The poles are well separated since $C_L \gg C_{R1}$ and $G_1 \approx G_2$. Hence, the approximate formula

$$\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right) \approx 1 + \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \tag{2.5}$$

is a good approximation of the location of the poles. This results in the fact

that the first pole is located at

$$p_1 \approx \frac{a}{b} = \frac{G_1 g_{ds} + G_2(G_1 + g_{ds} + g_m + g_{mbs})}{C_{R1}(g_{ds} + G_2) + C_L(G_1 + g_{ds} + g_m + g_{mbs})} \approx \frac{G_2}{C_L} \quad (2.6)$$

while the second pole is

$$p_2 \approx \frac{b}{c} = \frac{C_{R1}(g_{ds} + G_2) + C_L(G_1 + g_{ds} + g_m + g_{mbs})}{C_L C_{R1}} \approx \frac{G_2}{C_L} + \frac{G_1}{C_{R1}} \approx \frac{G_1}{C_{R1}}$$

The zero is expressed as

$$z = \frac{G_1}{C_{R1}} \quad (2.7)$$

Note that the second pole and the first zero is not located on top of each other, but they are close to each other.

To compute the output resistance we need to setup the problem once again. This time the input voltage is zero while we apply a voltage source at the output of the gain stage. We like to compute the current that this voltage source delivers to the circuit in order to obtain the output resistance. We reformulate the nodal analysis equations from assignment b.

$$V_x G_1 + (V_x - V_{out})g_{ds} - g_m(-V_x) - g_{mbs}(-V_x) = 0$$

$$(V_{out} - V_x)g_{ds} + g_m(-V_x) + g_{mbs}(-V_x) + V_{out}G_2 = I_{out}$$

Solving for V_x from the first equation yields

$$V_x = \frac{g_{ds}V_{out}}{G_1 + g_{ds} + g_m + g_{mbs}} \quad (2.8)$$

Inserting it into the second equation and solving for V_{out} results in

$$V_{out}(g_{ds} + G_2) - \frac{g_{ds}V_{out}}{G_1 + g_{ds} + g_m + g_{mbs}}(g_{ds} + g_m + g_{mbs}) = I_{out}$$

$$\frac{V_{out}}{I_{out}} = \frac{G_1 + g_{ds} + g_m + g_{mbs}}{g_{ds}G_1 + G_2(G_1 + g_{ds} + g_m + g_{mbs})} \approx \frac{1}{G_2} \quad (2.9)$$

3. Macro blocks

In an analog circuit, the building block shown in Figure 3.1 is found. The OP amp is assumed to be ideal except that it has finite DC gain, A_0, and a nonzero output resistance, R_{out}.

a) Derive the transfer function from the input to the output of the circuit, $H(s) = V_{out}(s)/V_{in}(s)$.

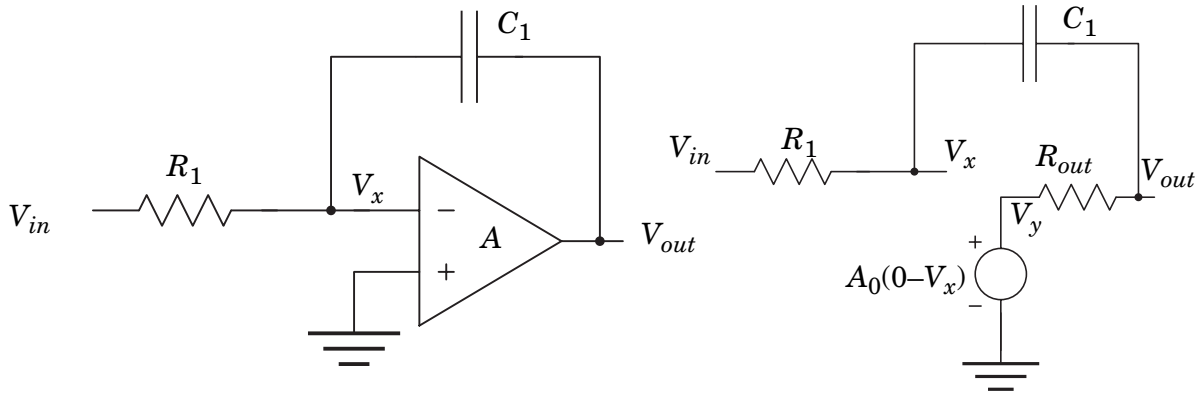

Figure 3.1 A Miller integrator. a) Amplifier description, b) Macro model description.

The transfer function can be computed by nodal analysis in the nodes V_x and V_{out}.

$$\frac{V_{in} - V_x}{R_1} + (V_{out} - V_x)sC_1 = 0 \tag{3.1}$$

$$(V_x - V_{out})sC_1 + \frac{(V_y - V_{out})}{R_{out}} = 0 \tag{3.2}$$

Further,

$$V_y = -A_0 V_x \tag{3.3}$$

Combining Eq. (3.2) and Eq. (3.3) results in

$$V_x(sC_1 - A_0 G_{out}) = V_{out}(sC_1 + G_{out}) \tag{3.4}$$

$$V_x = \frac{V_{out}(sC_1 + G_{out})}{(sC_1 - A_0 G_{out})} \tag{3.5}$$

Inserting it into Eq. (3.1) gives the transfer function.

$$V_{in}G_1 = -V_{out}\left(sC_1 + (G_1 + sC_1)\frac{sC_1 + G_{out}}{A_0G_{out} - sC_1}\right) \tag{3.6}$$

$$\begin{aligned}\frac{V_{out}}{V_{in}} &= -\frac{(A_0G_{out} - sC_1)G_1}{(G_1 + sC_1)(G_{out} + sC_1) + sC_1(A_0G_{out} - sC_1)} = \\ &= -\frac{(A_0G_{out} - sC_1)G_1}{(G_1G_{out} + sC_1(G_{out}(1 + A_0) + G_1))} = \\ &= -\frac{(G_{out} - sC_1/A_0)G_1}{\frac{G_1G_{out}}{A_0} + sC_1\left(\left(1 + \frac{1}{A_0}\right)G_{out} + \frac{G_1}{A_0}\right)}\end{aligned} \tag{3.7}$$

b) Derive the transfer function, $H(s) = V_{out}(s)/V_{in}(s)$, for the circuit when the DC gain is infinite and the output resistance is nonzero.

In the case where A_0 is infinite we can either use Eq. (3.7) or compute the transfer function from the schematic in Figure 3.1. In this case we derive the result from Eq. (3.7). This results in

$$\left.\frac{V_{out}}{V_{in}}\right|_{A_0 \to \infty} = -\frac{G_{out}G_1}{sC_1G_{out}} = -\frac{1}{sR_1C_1} \tag{3.8}$$

which is a regular inverting integrator. Hence, a large gain of the amplifier decreases the influence of the output resistance.

c) Derive the transfer function, $H(s) = V_{out}(s)/V_{in}(s)$, of the circuit when the output resistance is zero and the DC gain is finite.

Here we can also derive the transfer function directly from the model in Figure 3.1, but in this case we use the formula in Eq. (3.7).

$$\begin{aligned}\left.\frac{V_{out}}{V_{in}}\right|_{R_{out} \to 0} &= \left.-\frac{(G_{out} - sC_1/A_0)G_1}{\frac{G_1G_{out}}{A_0} + sC_1\left(\left(1 + \frac{1}{A_0}\right)G_{out} + \frac{G_1}{A_0}\right)}\right|_{G_{out} \to \infty} = \\ &= \left.-\frac{(1 - sC_1/A_0/G_{out})G_1}{\frac{G_1}{A_0} + sC_1\left(\left(1 + \frac{1}{A_0}\right) + \frac{G_1}{A_0G_{out}}\right)}\right|_{G_{out} \to \infty} = -\frac{G_1}{\frac{G_1}{A_0} + sC_1\left(1 + \frac{1}{A_0}\right)} = \\ &= -\frac{1}{\frac{1}{A_0} + sC_1R_1\left(1 + \frac{1}{A_0}\right)}\end{aligned} \tag{3.9}$$

This is an integrator which has a pole at low frequencies due to the finite gain of the amplifier.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1, i.e., time t, $t + 2\tau$, $t + 4\tau$, is shown in the figure. The value of V_1 changes only at time t, $t + 2\tau$, $t + 4\tau$, and so on, i.e., $V_1(t) = V_1(t + \tau)$.

a) Express the output voltage, $V_{out}(z)$, for clock phase 1 of the switched

capacitor circuit shown in the figure. Assume that the OTA is ideal.

Starting by assigning positive charge at the left plate of capacitor C_1 and to the right of capacitor C_2 and C_3. The next step is to express the charge at the capacitors.

At time t

$q_1(t) = 0$, $q_2(t) = C_2 V_{out}(t)$, $q_3(t) = C_3 V_{out}(t)$

time $t + \tau$

$q_1(t + \tau) = C_1 V_{in}(t + \tau)$, $q_2(t + \tau) = 0$, $q_3(t + \tau) = C_3 V_{out}(t + \tau)$

and at time $t + 2\tau$

$q_1(t + 2\tau) = 0$, $q_2(t + 2\tau) = C_2 V_{out}(t + 2\tau)$, $q_3(t + 2\tau) = C_3 V_{out}(t + 2\tau)$

The charge conservation equations are

$$q_3(t) = q_3(t + \tau) \tag{4.1}$$

$$q_1(t + \tau) + q_2(t + \tau) + q_3(t + \tau) = \\ = q_1(t + 2\tau) + q_2(t + 2\tau) + q_3(t + 2\tau) \tag{4.2}$$

The Eq. (4.1) results in

$$C_3 V_{out}(t) = C_3 V_{out}(t + \tau) \tag{4.3}$$

which states that the output voltage is kept constant between clock phase 1 to 2.

Furthermore, Eq. (4.2) results in

$$C_1 V_{in}(t + \tau) + C_3 V_{out}(t) = C_2 V_{out}(t + 2\tau) + C_3 V_{out}(t + 2\tau)$$

We also know that $V_{in}(t) = V_{in}(t + \tau)$ which yield that

$$C_1 V_{in}(t) + C_3 V_{out}(t) = (C_2 + C_3) V_{out}(t + 2\tau)$$

Performing a Z-transformation on this equation gives the results

$$V_{out}(z)((C_2 + C_3)z - C_3) = C_1 V_{in}(z) \tag{4.4}$$

rearranging the equation yields

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1}{C_2 + C_3} \frac{1}{z - \dfrac{C_3}{C_2 + C_3}} \tag{4.5}$$

which is a common noninverting lossy accumulator.

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully.

The parasitics of interest are shown in

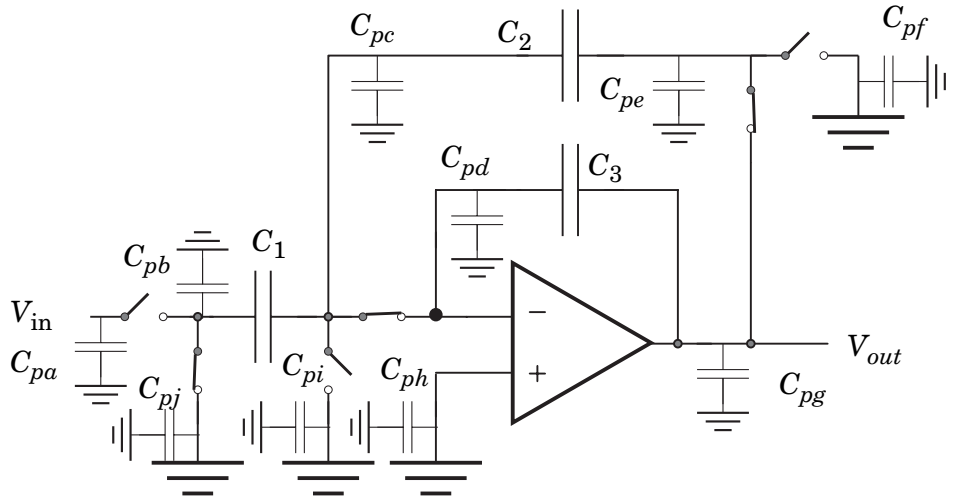

Figure 4.1 The SC circuit with capacitive parasitics due to the capacitor and the switches.

C_{pa} does not alter the transfer function since it is always connected to the ideal input source.

C_{pb} does not change the transfer function since it is shorted to ground in one clock phase and connected to ground and the input source in the other clock phase.

C_{pc} The voltage in node where this parasitic is connected is always virtual ground or ground. Hence, the transfer function will not be changed.

C_{pd} Connected between ground and virtual ground which results in no change in the transfer function

C_{pe} Connected between ground and ground or output of the OPamp and ground. No effect on the transfer function.

C_{pg} Connected between output node of OPamp to ground. No changes in the transfer function.

C_{ph}, C_{pi}, C_{pj}, C_{pf} Connected between ground and ground not changing the transfer function.

Hence, the circuit is insensitive to capacitive parasitics, when the transfer function is of concern, but the settling time will be affected.

c) Express the output voltage, $V_{out}(z)$, for clock phase 1 of the switched capacitor circuit shown in the Figure. Assume that the OTA suffers from an offset voltage.

Starting by assigning positive charge at the left plate of capacitor C_1 and to the right of capacitor C_2 and C_3. The next step is to express the charge at the capacitors.

At time t

$q_1(t) = -C_1V_{os}$, $q_2(t) = C_2(V_{out}(t) - V_{os})$, $q_3(t) = C_3(V_{out}(t) - V_{os})$

time $t + \tau$

$q_1(t+\tau) = C_1V_{in}(t+\tau)$, $q_2(t+\tau) = 0$, $q_3(t+\tau) = C_3(V_{out}(t+\tau) - V_{os})$

and at time $t + 2\tau$

$q_1(t+2\tau) = -C_1V_{os}$,

$q_2(t+2\tau) = C_2(V_{out}(t+2\tau) - V_{os})$, $q_3(t+2\tau) = C_3(V_{out}(t+2\tau) - V_{os})$

The charge conservation equations are

$$q_3(t) = q_3(t+\tau) \tag{4.6}$$

$$q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) = \\ = q_1(t+2\tau) + q_2(t+2\tau) + q_3(t+2\tau) \tag{4.7}$$

The Eq. (4.1) results in

$$C_3(V_{out}(t) - V_{os}) = C_3(V_{out}(t+\tau) - V_{os}) \tag{4.8}$$

which states that the output voltage is kept constant between clock phase 1 to 2.

Furthermore, Eq. (4.2) results in

$$C_1V_{in}(t+\tau) + C_3(V_{out}(t+\tau) - V_{os}) = -C_1V_{os} + (C_2+C_3)(V_{out}(t+2\tau) - V_{os})$$

We also know that $V_{in}(t) = V_{in}(t+\tau)$ which yield that

$$C_1V_{in}(t) + C_3V_{out}(t) + (C_1+C_2)V_{os} = (C_2+C_3)V_{out}(t+2\tau)$$

Performing a Z-transformation on the above equations results in

$$V_{out}(z)((C_2+C_3)z - C_3) = C_1V_{in}(z) + (C_1+C_2)V_{os} \tag{4.9}$$

rearranging the equation yields

$$V_{out}(z) = \frac{1}{C_2+C_3}\frac{1}{z - \frac{C_3}{C_2+C_3}}(C_1V_{in}(z) + (C_1+C_2)V_{os}) \tag{4.10}$$

which is a common noninverting lossy accumulator which is not offset compensated.

5. A mixture of questions

a) The current in a special CMOS transistor is given by

$$I = \alpha(V_{GS} - V_T)^{\gamma}(1 + \lambda(V_{DS} - V_{GS} + V_T)) \tag{5.1}$$

Derive approximate expressions for the transconductance and the output conductance as a function of the current through the device, but not as a function of any voltages. For the computation of the transconductance assume that the λ parameter is zero.

The transconductance is given by (since the λ parameter is neglected)

$$g_m = \frac{\partial I}{\partial V_{GS}} = \alpha\gamma(V_{GS} - V_T)^{\gamma-1} = \gamma\alpha^{2-\gamma}(\alpha^{\gamma-1}(V_{GS} - V_T)^{\gamma-1}) = \gamma\alpha^{2-\gamma}I^{\frac{\gamma-1}{\gamma}}$$

The g_{ds} parameter is

$$g_{ds} = \frac{\partial I}{\partial V_{DS}} = \lambda\alpha(V_{GS} - V_T)^{\gamma} \approx \lambda I \tag{5.2}$$

b) State three techniques to increase the DC gain in the common-source amplifier shown in the figure. Both changes to the topology and the design parameters are allowed.

There are several techniques

Add cascodes

Add cascodes plus gain boosting

Increase the size of the input transistor

Decrease the current

c) Derive the input and output ranges of the amplifier shown in the figure. Express the them in relevant design parameters (I_{D6}, α_i, ...).

Starting from the CMR and with the maximum input voltage we see that this voltage is

$$V_{in,\,max} = V_{DD} - V_{SG3} - V_{DS1} + V_{GS1} = V_{DD} - \sqrt{\frac{I_{bias}}{2\alpha_3}} - V_{T3} + V_{T1}$$

The minimum input voltage is determined the path gnd->M7->M8->M5->M1 which results in

$$V_{in,\,min} = V_{GS7} + V_{GS8} - V_{GS5} + V_{DS5} + V_{GS1} =$$
$$\sqrt{\frac{I_{bias}}{\alpha_7}} + V_{T7} + \sqrt{\frac{I_{bias}}{\alpha_8}} + V_{T8} - V_{T5} + \sqrt{\frac{I_{bias}}{2\alpha_1}} + V_{T1} \tag{5.3}$$

$$CMR = [V_{in,\,min}; V_{in,\,max}] \tag{5.4}$$

The output range is determined in a similar manner

$$V_{out,\,max} = V_{DD} - V_{SD4} = V_{DD} - \sqrt{\frac{I_{bias}}{2\alpha_4}} \tag{5.5}$$

$$V_{out,\,min} = V_{GS7} + V_{GS8} - V_{GS5} + V_{DS5} + V_{DS1} =$$
$$= \sqrt{\frac{I_{bias}}{\alpha_7}} + V_{T7} + \sqrt{\frac{I_{bias}}{\alpha_8}} + V_{T8} - V_{T5} + \sqrt{\frac{I_{bias}}{2\alpha_1}} \tag{5.6}$$

$$OR = [V_{out,\,min}; V_{out,\,max}] \tag{5.7}$$