Correct(?) Solutions to Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	April 15, 2002
Time:	14 - 18
Place:	T1 and T2
Max. no of points:	70; 50 from written test, 15 for project, and 5 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Exercise

1. Basic CMOS building blocks

The circuit shown in the figure is to be designed in a special process where the threshold voltages and the channel length modulations are equal for the pmos and nmos transistors.

a) Design the circuit to achieve the voltages $V_{out} = V_{in} = V_{DD}/2$ when $V_{DD} > 2V_T$.

When both transistors are operating in the saturation region then is the current given by.

$$I_{D1} = \alpha_1(V_{in} - V_T)^2(1 + \lambda V_{out}) \quad (1.1)$$

$$I_{D2} = \alpha_2(V_{DD} - V_{in} - V_T)^2(1 + \lambda(V_{DD} - V_{out})) \quad (1.2)$$

Further, the input and output voltages equals $V_{DD}/2$ and the equations can be simplified to

$$I_{D1} = \alpha_1(V_{DD}/2 - V_T)^2(1 + \lambda(V_{DD}/2)) \quad (1.3)$$

$$I_{D2} = \alpha_2(V_{DD}/2 - V_T)^2(1 + \lambda(V_{DD}/2)) \quad (1.4)$$

The currents must be equal since KCL must be met. The currents are equal if $\alpha_1 = a_2$.

b) Sketch the output voltage, V_{out}, as a function of the input voltage, V_{in}, for $0 < V_{in} < V_{DD}$. Indicate the operation regions of both transistor in the graph.

For smaller input voltages than V_T the transistor M_1 will be cut-off and no current will flow through that transistor. The transistor M_2 will operate in the saturation region. The output voltage will be close to V_{DD}.

Increasing the input voltage will bias transistor M_1 in the linear (triode) region and the current will increase. Transistor M_2 will still operate in the saturation region. The output voltage will start to decrease.

Both transistors will be in saturation when the input voltage is even higher. The output voltage will then decrease quickly.

A further increase will bias transistor M_2 in the linear region and M_1 will still be in saturation. The output voltage will start to decrease slower than when both transistors are operating in the saturation region.

The last case is when the input voltage is larger that $V_{DD} - V_T$ when transistor M_2 will operate in the cut-off region and M_1 in the saturation region. Here will the output voltage be very close to zero.

The transfer function is shown in Figure 1.1.

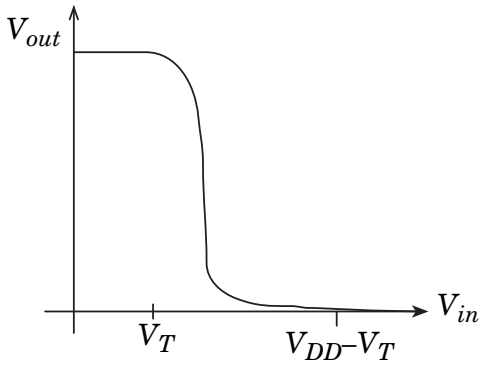

Figure 1.1 The transfer function of the CMOS inverter.

c) Express the output voltage as a function of the input voltage when both transistors are operating in the saturation region.

The currents through transistor M_1 and M_2 is given in (1.1) and (1.2). KCL states that I_{D1} must equal I_{D2}. This gives the following equation.

$$\alpha_1(V_{in} - V_T)^2(1 + \lambda V_{out}) = \alpha_2(V_{DD} - V_{in} - V_T)^2(1 + \lambda(V_{DD} - V_{out})) \quad (1.5)$$

Solving for V_{out} gives

$$V_{out} = \frac{\alpha_2(V_{DD} - V_{in} - V_T)^2 - \alpha_1(V_{in} - V_T)^2}{\lambda(\alpha_2(V_{DD} - V_{in} - V_T)^2 + \alpha_1(V_{in} - V_T)^2)} \quad (1.6)$$

2. Small signal analysis

Assume that all transistors are biased so that they are operating in the saturation region. Neglect the influence of the parasitics capacitances.

a) What do we call the circuit shown in the figure?

The circuit is called a common-source gain stage with cascodes.

b) Draw the small signal equivalent for the amplifier.

The small signal scheme for the amplifier is shown in Figure 2.1

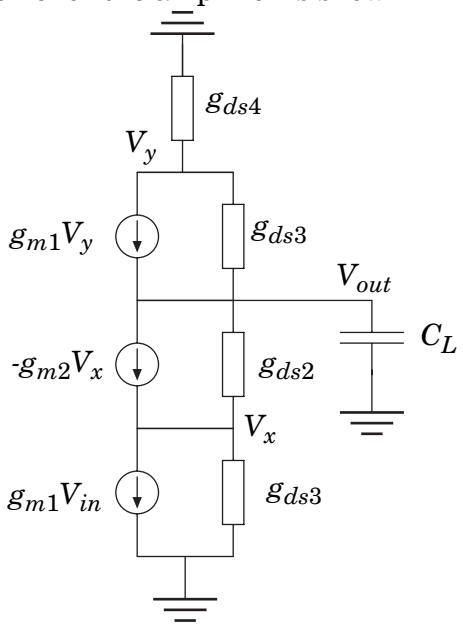

Figure 2.1 The small signal scheme of a cascode amplifier.

c) Derive the transfer function, $v_{out}(s)/v_{in}(s)$, of the circuit.

The transfer function can be found in several different ways, for example by using the nodal analysis in the nodes, using the fact that for a single stage amplifier the gain is given by the transconductance of the input transistor divided by the output conductance of output admittance of the circuit, or by using KVL in the circuit. Here the solution is given by using the fact that the transfer function is given by the input transconductance over the output conductance.

Since the bulk and the source of each transistor is connected to the same potential no g_{mbs} factor will appear in the expression below.

Starting to compute the output impedance of a cascode as shown in Figure

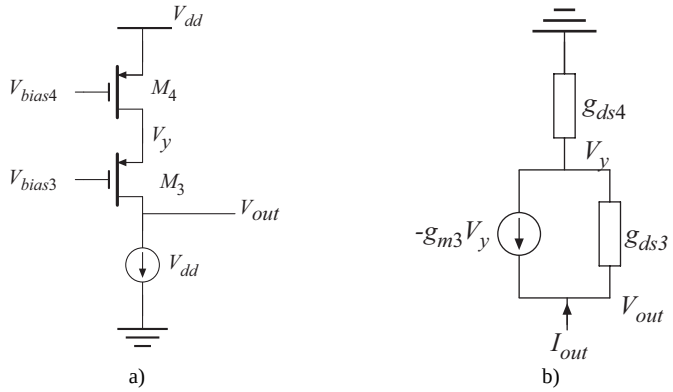

Figure 2.2 a) A cascode transistor. b) The ESSS of the circuit.

2.2a with the ESSS as shown in Figure 2.2b. The current delivered by the output voltage source is

$$I_{out} = V_y g_{ds4} = -g_{m3}V_y - g_{ds3}(V_y - V_{out}) \tag{2.1}$$

The output resistance is

$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{g_{m3} + g_{ds3} + g_{ds4}}{g_{ds3}g_{ds4}} \approx \frac{g_{m3}}{g_{ds3}g_{ds4}} = \frac{A_3}{g_{ds4}} \tag{2.2}$$

where A_3 is the gain of the transistor M_3. The two transistors above can be replaced by a resistor with the values of A_3/g_{ds4} when we are computing the DC characteristics.

The simplified ESSS of the amplifier is shown in Figure 2.3. The DC gain

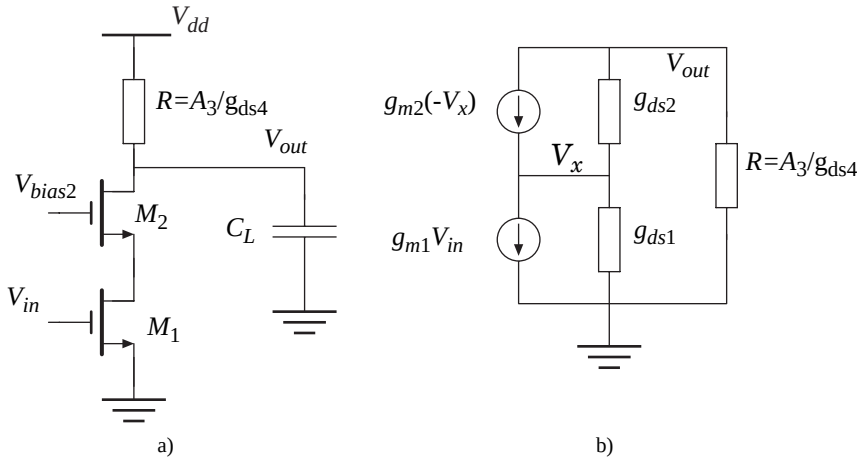

Figure 2.3 a) Equivalent low frequency cascode amplifier. b) ESSS of the simplified amplifier.

can be found from the following equations.

$$g_{m1}V_{in} + V_x g_{ds1} + g_{m2}V_x + (V_x - V_{out})g_{ds2} = 0 \tag{2.3}$$

$$(-g_{m2})V_x + (V_{out} - V_x)g_{ds2} + V_{out}(G + sC_L) = 0 \tag{2.4}$$

Solving for V_{out} gives the following DC gain.

$$\begin{aligned}\frac{V_{out}}{V_{in}} &= -\frac{g_{m1}(g_{m2} + g_{ds2})}{g_{ds1}g_{ds2} + (G + sC_L)(g_{ds1} + g_{ds2} + g_{m2})} \approx \\ &\approx -\frac{g_{m1}}{\frac{g_{ds1}g_{ds2}}{g_{m2}} + G + sC_L} = -\frac{g_{m1}}{\frac{g_{ds1}g_{ds2}}{g_{m2}} + \frac{g_{ds3}g_{ds4}}{g_{m3}} + sC_L} \\ &\approx -\frac{g_{m1}}{\frac{g_{ds1}g_{ds2}}{g_{m2}} + \frac{g_{ds3}g_{ds4}}{g_{m3}}} \frac{1}{1 + \frac{s}{\left(\frac{g_{ds1}g_{ds2}}{g_{m2}} + \frac{g_{ds3}g_{ds4}}{g_{m3}}\right)/C_L}}\end{aligned} \tag{2.5}$$

The DC gain can be expressed as g_{m1}/g_{out} where the output conductance is the sum of the conductances seen from the output to ground and from the output to the positive supply voltage (the parallel connection of the two output resistances seen up and down from the output). The cascode transistors are used to enhance the output resistance by the gain of the cascode transistors, i.e. g_{m2}/g_{ds2} and g_{m3}/g_{ds3} respectively.

The first pole is extracted from Eq. (2.5) according to

$$p_1 \approx \left(\frac{g_{ds1} g_{ds2}}{g_{m2}} + \frac{g_{ds3} g_{ds4}}{g_{m3}} \right) / C_L \tag{2.6}$$

d) What will happen to the output impedance if ...

... the current through the gain stage is increased?

... the width of transistor M_2 is decreased?

... the width of transistor M_1 is decreased?

Also, describe the impact on the bandwidth and the DC gain for each modification of the circuit.

The small signal parameters can be expressed by the large signal parameters through the derivative of the drain current. These small signal parameters can be expressed as a function of the drain current of the transistor. These parameters can approximately be expressed as

$$g_{ds} \approx \lambda I_D \tag{2.7}$$

$$g_m \approx \sqrt{2K \frac{W}{L} I_D} \tag{2.8}$$

The output impedance can then be approximated to

$$R_{out} = \frac{1}{\frac{g_{ds1} g_{ds2}}{g_{m2}} + \frac{g_{ds3} g_{ds4}}{g_{m3}}} \propto \frac{1}{\frac{I_D^2 \lambda^2}{\sqrt{\frac{W_2}{L} I_D}} + \frac{I_D^2 \lambda^2}{\sqrt{\frac{W_3}{L} I_D}}} \propto \frac{1}{\lambda^2 I_D^{3/2}} \frac{1}{\sqrt{\frac{L}{W_2}} + \sqrt{\frac{L}{W_3}}} \tag{2.9}$$

The DC gain is

$$A_0 = -\frac{g_{m1}}{g_{out}} \propto -\frac{\sqrt{\frac{W_1}{L} I_D}}{\lambda^2 I_D^{3/2} \left(\sqrt{\frac{L}{W_2}} + \sqrt{\frac{L}{W_3}} \right)} = -\frac{\sqrt{W_1}}{\lambda^2 I_D L \left(\frac{1}{W_2} + \frac{1}{W_3} \right)} \tag{2.10}$$

The bandwidth of the circuit can approximately be expressed as

$$\omega_{-3dB} = p_1 = \frac{g_{out}}{C_L} \propto \frac{\lambda^2 I_D^{3/2}}{C_L} \left(\sqrt{\frac{L}{W_2}} + \sqrt{\frac{L}{W_3}} \right) \tag{2.11}$$

The variations the performance due the changed currents and transistor

Table 1: The performance metrics variations

	R_{out}	DC gain	Bandwidth
Increased I_D	Decreased	Decreased	Increased
Decreased W_2	Decreased	Decreased	Increased
Decreased W_1	Unchanged	Decreased	Unchanged

widths are shown in Table 1 on page 7.

3. Operational amplifier

The transfer function for the circuit shown in the figure can be expressed as in (3.1). The amplifier is assumed to have infinite input impedance and zero output impedance.

$$H(s) = \frac{v_{out}(s)}{v_{in}(s)} = K(s)\frac{A(s)}{1+\beta(s)A(s)} \tag{3.1}$$

a) Derive the transfer function of the circuit shown in the figure and identify the factors $K(s)$ and $\beta(s)$.

The output voltage from the amplifier is given by $V_{out} = -A(s)V_-$ which can be formulated as $V_- = -V_{out}/A(s)$. The current through impedance Z_1 equals

$$I_{Z1} = \frac{V_{in} - V_-}{Z_1} \tag{3.2}$$

and the current through impedance Z_2 is

$$I_{Z2} = \frac{V_- - V_{out}}{Z_2} \tag{3.3}$$

No current is flowing into the operational amplifier since it has infinite input impedance, thereby must $I_{Z1} = I_{Z2}$. Solving for V_{out} gives

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{Z_1\left(\frac{1}{A(s)}\left(\frac{1}{Z_1}+\frac{1}{Z_2}\right)+\frac{1}{Z_2}\right)} = -\frac{Z_2}{Z_1+Z_2}\frac{A(s)}{1+\frac{Z_1}{Z_1+Z_2}A(s)} \tag{3.4}$$

From this expression $K(s)$ and $\beta(s)$ can be found.

$$K(s) = -\frac{Z_2}{Z_1+Z_2} \tag{3.5}$$

$$\beta(s) = \frac{Z_1}{Z_1 + Z_2} \tag{3.6}$$

b) b) Assume that $Z_1 = R_1$, $Z_2 = R_2$, which yields a constant β, and that

$$A(s) = \frac{A_0}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \tag{3.7}$$

where the poles are well separated, i.e., $|p_2| \gg |p_1|$. Determine the feed-back factor to get $\phi_m = 75°$ where $\phi_m = 180° + \arg(\beta \cdot A(j\omega_u))$ and ω_u is defined by $|\beta \cdot A(j\omega_u)| = 1$
Hint: Assume that

$$\arg\left(1 + j\frac{\omega_u}{p_1}\right) = 90° \tag{3.8}$$

The phase margin of an amplifier is given by the loop gain, $LG(s) = \beta(s)A(s)$, of the feedback. It is easy to show that for a resistive feedback the worst case appears when $\beta = 1$ and thereby $LG(s) = A(s)$.
The phase margin is given by

$$\phi_m = 180 - \text{atan}\left(\frac{\omega_u}{p_1}\right) - \text{atan}\left(\frac{\omega_u}{p_2}\right) = 180 - 90 - \text{atan}\left(\frac{\omega_u}{p_2}\right) \tag{3.9}$$

Solving for $\phi_m = 75°$ gives $\omega_u = p_2 \tan(15) \approx 0.268 p_2$, where ω_u is the unity-gain frequency for the loop-gain. Hence, the solution to the following equation is of interest.

$$|\beta A(j\omega_u)| = 1 \tag{3.10}$$

which can be expressed as

$$\beta |A(j\omega_u)| = 1 \tag{3.11}$$

since the feed back factor, β, is a real number larger that zero. The feed back factor is given by

$$\begin{aligned}\beta &= \frac{1}{|A(j\omega_u)|} = \frac{\left|1 + j\frac{p_2 \tan(15)}{p_1}\right| |1 + j\tan(15)|}{|A_0|} \\ &= \frac{\sqrt{1 + \left(\frac{p_2 \tan(15)}{p_1}\right)^2}\sqrt{1 + \tan^2(15)}}{|A_0|}\end{aligned} \tag{3.12}$$

to assure that the phase margin of the system is 75 degrees.

4. Switched capacitor

A switched capacitor circuit in clock cycle 1 is shown in the figure. The input signal is constant on the time interval
$V(t + (2n + 1)\tau) = V(t + (2n + 2)\tau)$.

a) Derive the transfer function for the switched capacitor circuit shown in Figure 4.1, i.e., $V_3(z) = \alpha V_1(z) + \beta V_2(z)$. Assume that the OTA is ideal.

The circuit in the two different clock cycles is shown in

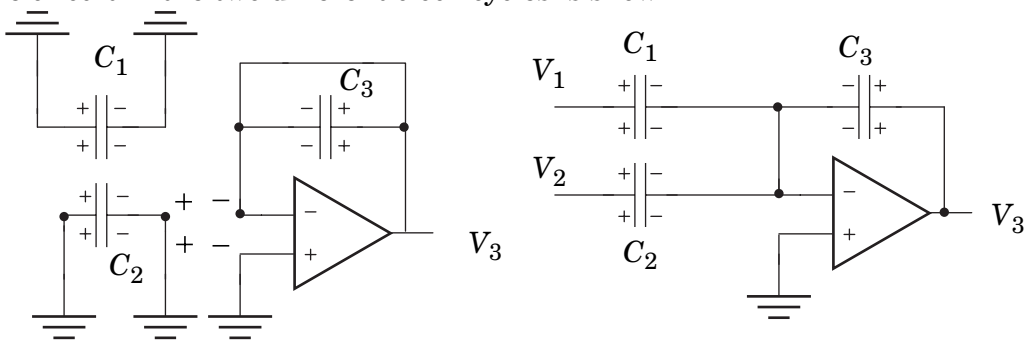

Figure 4.1 The circuit in both clock cycles.

Charge analysis

time t:

$$q_1(t) = 0,\ q_2(t) = 0,\ q_3(t) = 0, \tag{4.1}$$

time t+τ:

$$q_1(t + \tau) = V_1(t + \tau)C_1,\ q_2(t + \tau) = V_2(t + \tau)C_2,$$
$$q_3(t + \tau) = C_3V_3(t + \tau) \tag{4.2}$$

time t+2τ:

$$q_1(t + 2\tau) = 0,\ q_2(t + 2\tau) = 0,\ q_3(t + 2\tau) = 0 \tag{4.3}$$

The charge conservation equation is

$$q_1(t) + q_2(t) + q_3(t) = q_1(t + \tau) + q_2(t + \tau) + q_3(t + \tau) \tag{4.4}$$

Using Eq. (4.4) together with the expression above gives

$$0 = C_1V_1(t + \tau) + C_2V_2(t + \tau) + C_3V_3(t + \tau) \tag{4.5}$$

Since the input signal is constant in the interval $t + (2n + 1)\tau$ to $t + (2n + 2)\tau$ then $V_1(t + \tau) = V_1(t + 2\tau), V_2(t + \tau) = V_2(t + 2\tau)$, and $V_3(t + \tau) = V_3(t + 2\tau)$. This gives

$$C_1V_1(t + 2\tau) + C_2V_2(t + 2\tau) + C_3V_3(t + 2\tau) = 0 \tag{4.6}$$

Computing the transfer function for clock cycle can be done by Z transforming Eq. (4.6).

$$V_3(z) = -\frac{C_1}{C_3}V_1(z) - \frac{C_2}{C_3}V_2(z) \tag{4.7}$$

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully.

The circuit with all parasitics is shown in Figure 4.2.

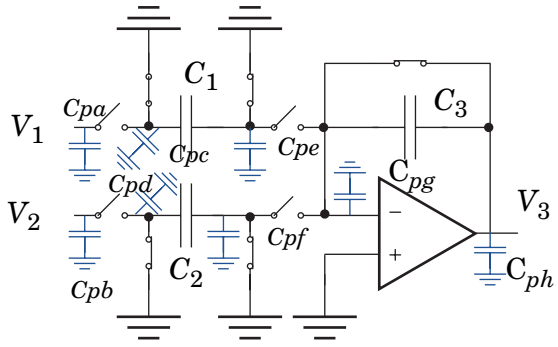

Figure 4.2 The SC circuit with capacitive parasitics.

C_{pa} and C_{pb} are connected to the input source which is assumed to be ideal thereby not changing the transfer function.

C_{pc} and C_{pd} Not changing the transfer function since it is connected to ground with both terminals or between ground and the ideal input source.

C_{pe} and C_{pf} Connected to between ground and virtual ground or between ground and ground.

C_{pg} is connected to the virtual ground and ground and thereby not changing the transfer function.

C_{pg} is connected to the ideal OTA output which does not change the transfer function.

Hence, the circuit is not sensitive to capacitive parasitics.

c) Assume that the OTA suffers from finite gain, A. Derive the output voltage $V_2(z)$ as a function of relevant circuit parameters.

The voltage at the negative input terminal is denoted as V_x. In clock cycle 2 is

$$V_x = -\frac{V_3(t+\tau)}{A} \tag{4.8}$$

Charge analysis

time t:

$$q_1(t) = 0,\ q_2(t) = 0,\ q_3(t) = 0, \tag{4.9}$$

time t+τ:

$$\begin{aligned} q_1(t+\tau) &= C_1(V_1(t+\tau) - V_x(t+\tau)), \\ q_2(t+\tau) &= C_2(V_2(t+\tau) - V_x(t+\tau)), \\ q_3(t+\tau) &= C_3(V_3(t+\tau) - V_x(t+\tau)) \end{aligned} \tag{4.10}$$

time t+2τ:

$$q_1(t+2\tau) = 0,\ q_2(t+2\tau) = 0,\ q_3(t+2\tau) = 0 \tag{4.11}$$

The charge conservation equation is

$$q_1(t) + q_2(t) + q_3(t) = q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) \tag{4.12}$$

Since the input signal is constant in the interval $t + (2n+1)\tau$ to $t + (2n+2)\tau$ then $V_1(t+\tau) = V_1(t+2\tau)$, $V_2(t+\tau) = V_2(t+2\tau)$, and $V_3(t+\tau) = V_3(t+2\tau)$. This gives

$$C_1\left(V_1(t+2\tau) + \frac{V_3(t+2\tau)}{A}\right) + \left(V_2(t+2\tau) + \frac{V_3(t+2\tau)}{A}\right)C_2 + C_3V_3(t+2\tau)\left(1+\frac{1}{A}\right) = 0$$

The gives the following expression

$$-C_1V_1(t+2\tau) - V_2(t+2\tau)C_2 = V_3(t+2\tau)\left(\left(1+\frac{1}{A}\right)C_3 + \frac{C_2}{A} + \frac{C_1}{A}\right) \tag{4.13}$$

computing the transfer function by using the Z transform.

$$V_3(z) = -\frac{C_1V_1(z) + V_2(z)C_2}{C_3}\frac{1}{1+\frac{1}{A}\left(1+\frac{C_1}{C_3}+\frac{C_2}{C_3}\right)} \tag{4.14}$$

The transfer function is changed when the gain of the OTA/OP is changed.

5. A mixture of questions

a) Linus has designed an operational transconductance amplifier, OTA, but he needs it to drive resistive load and, therefore, he needs to design an operational amplifier, OP. How can he transform the OTA into an OP?

He have to design an output stage with low output resistance to be able to drive resistive load. This can be accomplished by either adding a buffer as the last stage or by decreasing the output resistance of the last stage by for example increasing the current.

b) What type of circuit is shown in the figure?

It is a continuos-time active-RC integrator.

c) Derive an expression for the slew rate in the circuit shown in the figure.

The slew rate expresses the maximum derivative of the output voltage with respect to the time.

$$SR = max\left|\frac{dV_{out}}{dt}\right| = min\left(\frac{max(I_2)}{C_2}, \frac{max(I_1)}{C_1}H\right) \tag{5.1}$$

where H is the transfer function from the top node of C_1 to the output. In this case H is given by

$$H = \frac{g_{m2}}{g_{ds2}} \tag{5.2}$$

The slew rate is given by

$$SR = min\left(\frac{max(I_2)}{C_2}, \frac{max(I_1)}{C_1}\frac{g_{m2}}{g_{ds2}}\right) \tag{5.3}$$

d) Describe the benefits and drawbacks of a fully differential compared to a single-ended circuit.

A fully differential gain stage is less sensitive to power supply variations and noise. Further, even order harmonic distortion will be cancelled or at least much smaller at the fully differential output.

The drawbacks is the extra power that is consumed since we need to have a larger bias circuit and also more current can be consumed in the extra branched needed. Another part is the design of a common-mode feed back circuit.

e) Express the output range, OR, and the common-mode range, CMR, for the differential gain stage using relevant design parameters such as α, I_D.

The minimum input voltage is determined by

$$V_{in,\,min} = V_{gs3} + V_{sd,\,sat1} - V_{sg1} = \sqrt{\frac{I_{D3}}{\alpha_3}} + V_{T3} - V_{T1} \tag{5.4}$$

The maximum input voltage is given by

$$V_{in,\,max} = V_{DD} - V_{sdsat,\,5} - V_{sg1} = V_{DD} - \sqrt{\frac{I_{D5}}{\alpha_5}} - \sqrt{\frac{I_{D1}}{\alpha_1}} - V_{T1} \tag{5.5}$$

The minimum output voltage is

$$V_{out,\,min} = V_{dssat,\,4} = \sqrt{\frac{I_{D4}}{\alpha_4}} \tag{5.6}$$

The maximum output voltage is

$$V_{out,\,max} = V_{DD} - V_{sdsat,\,5} - V_{sdsat,\,2} = V_{DD} - \sqrt{\frac{I_{D5}}{\alpha_5}} - \sqrt{\frac{I_{D2}}{\alpha_2}} \tag{5.7}$$

The output range is given by

$$OR = [V_{out,\,min}, V_{out,\,max}] \tag{5.8}$$

and the common-mode range is

$$CMR = [V_{in,\,min}, V_{in,\,max}] \tag{5.9}$$