Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date:	April 22, 2004
Time:	14 – 18
Place:	U14
Max. no of points:	70; 50 from written test, 5 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design. Dictionaries.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Exercise

1. Large-signal analysis

The three amplifiers shown in Figure 1.1 are commonly used in for example operational amplifiers. In this exercise the analysis of these amplifier is considered. Assume that all transistor should operate in the saturation region.

a) Determine the width-over-length ratios of the two transistors in Figure 1.1a for a given output range OR, $V_{out,DC} = (OR_{min} + OR_{max})/2$, and current through the transistors I. Do not neglect the channel-length modulation nor the body effect. (2p)

b) Determine the width-over-length ration of the common drain circuit shown in Figure 1.1b so that the following specification is met. The voltages $V_{in,DC}$, $V_{out,DC}$, V_{bias}, and the current through the transistors I are given. Do not neglect the channel-length modulation nor the body effect. (2p)

c) Determine the input range of the common-drain amplifier shown in Figure 1.1b for the same parameters as in exercise 1b. Neglect the channel-length modulation, but not the body effect. (This exercise can be solved even though exercise 1b is not solved.) (2p)

d) Determine the width-over-length ratio for the transistors in the amplifier in Figure 1.1c to meet the following specification. The current through the transistors, I, and the voltages $V_{in,DC}$, $V_{out,DC}$, V_{bias1}, and V_{bias2} are given. Do not neglect the channel-length modulation nor the body effect. (2p)

e) Determine the output range of the amplifier shown in Figure 1.1c for the same parameters as in exercise 1d (This exercise can be solved even though exercise 1d is not solved.) (2p)

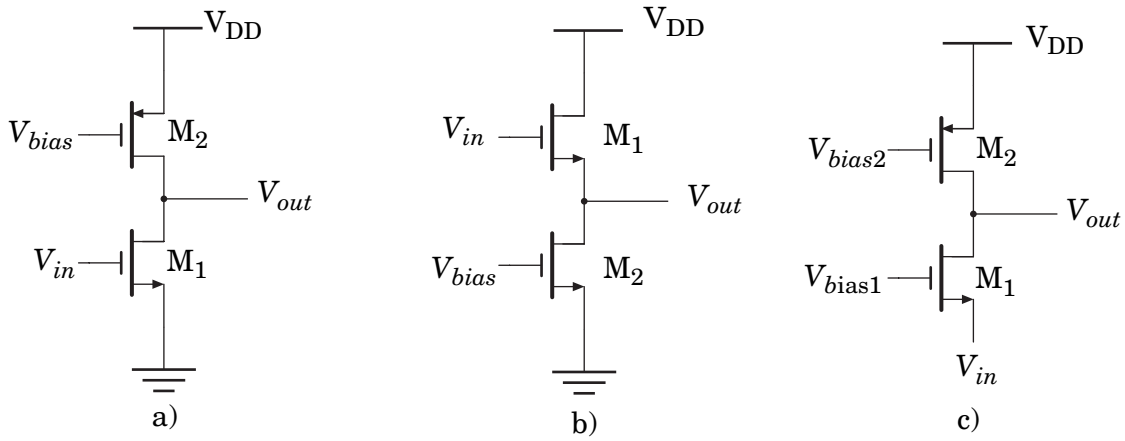

Figure 1.1 Simple amplifiers commonly used as building block in op amps.

2. Small-signal analysis

The transistors in the circuit shown in Figure 2.1 are biased in the saturation region. Neglect the influence of all internal parasitics in the transistors.

a) Compute the transfer function of the circuit shown in Figure 2.1a, $H(s) = V_{out}(s)/V_{in}(s)$. Do not neglect the bulk effect. (3p)

b) Express the DC gain and unity-gain frequency of the circuit shown in Figure 2.1a in terms of relevant design parameters (α, I_{bias}, ...). (2p)

c) Derive the transfer function of the circuit shown in Figure 2.1b, i.e., $H(s) = V_{out}(s)/V_{in}(s)$. Do not neglect the bulk effect. The gain A_I is a negative, real constant. (3p)

d) Express the DC gain and unity-gain frequency of the circuit shown in Figure 2.1b in terms of relevant design parameters (α, I_{bias}, ...). (2p).

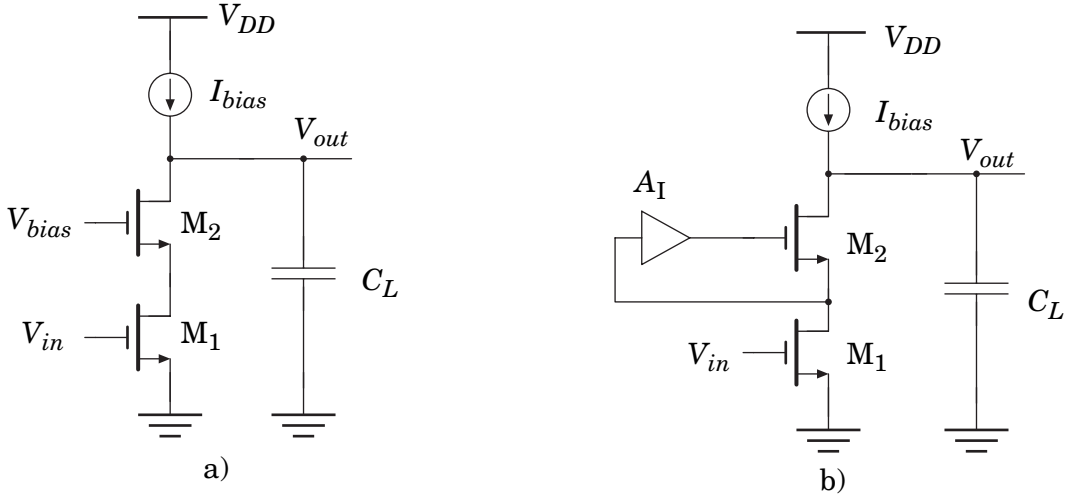

Figure 2.1 Two amplifier structures implemented in using MOS transistors.

3. Operational amplifiers

The trend is to decrease the minimum feature sizes in modern CMOS process. This causes the low-frequency gain of a single transistor to decrease. If high DC gain is required in a modern process a multi-stage amplifier may be a good choice. In this exercise, a small-signal equivalent of the differential response of a three stage amplifier shown in Figure 3.1a is considered. The common-mode gain is zero. Throughout this exercise, assume that $C_L \gg C_1 = C_2 = C$, $R_1 = R_2 = R_L = R$.

a) Derive the transfer function from the input to the output of the circuit shown in Figure 3.1a, i.e., $H(s) = V_{out}(s)/V_{in,\,diff}(s)$. (2p)

b) Compute an approximative expression for the unity-gain frequency given that the higher-order poles are located at much higher frequency than the unity-gain frequency. Motivate your solution. (1p)

c) The amplifier is connected in a close-loop configuration as shown in Figure 3.1b. For such a circuit, the transfer function can be given in the form

$$H(s) = \frac{A(s)}{1 + \beta A(s)} \tag{3.1}$$

where β is the feedback factor and $A(s)$ is the gain of the amplifier. Determine the feedback factor for the circuit shown in Figure 3.1b.(1p)

d) For the circuit in Figure 3.1b compute an analytic expression for the factor K, which relates the second pole p_2 and the unity-gain frequency ω_u, in the expression $p_2 = K \cdot \omega_u$ in order to obtain a specific phase margin, i.e., compute $K = f(\phi_m)$. Assume that at the unity-gain frequency the first pole has caused a –90 degree phase shift. (2p)

e) Compute the value of the K factor to obtain a phase margin of 45 and 75 degrees, respectively. (2p)

f) Is the approximation in 3b good for the two cases in exercise 3e? Motivate your answer carefully. (2p)

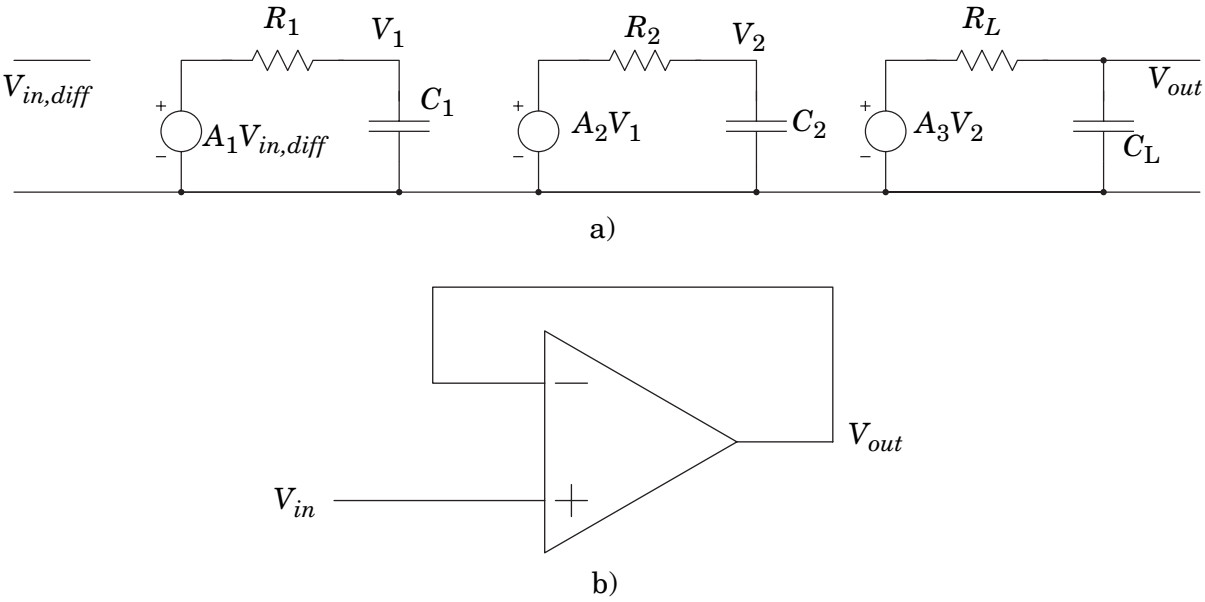

Figure 3.1 a) A small-signal model of the differential gain of a three stage amplifier. b) The three stage amplifier in a feedback configuration.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1, i.e., time t, $t + 2\tau$, $t + 4\tau$, etc. is shown in Figure 4.1.

a) Express the output voltage, $V_{out}(z)$, as a function of the input voltages, $V_1(z)$ and $V_2(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the operational amplifier is ideal. (4p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (2p)

c) Express the output voltage, $V_{out}(z)$, as a function of the input voltages, $V_1(z)$ and $V_2(z)$ for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA has finite gain, A. (4p)

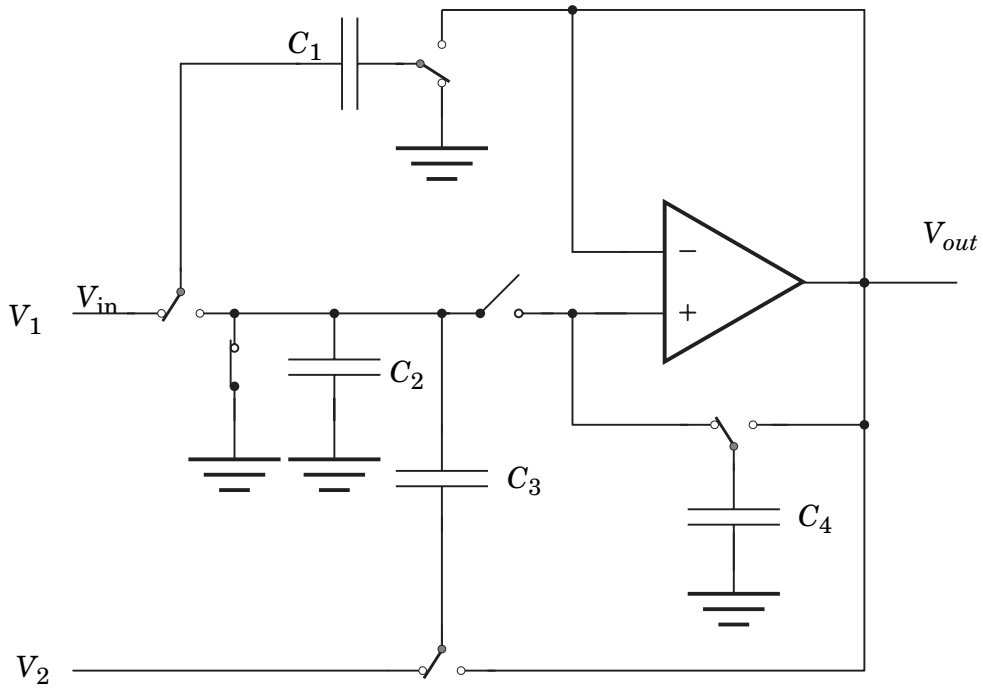

Figure 4.1 A switched-capacitor circuit in clock phase 1.

5. A mixture of questions

a) Design the circuit shown in Figure 5.1 so that $V_{in,\,DC} = V_{out,\,DC} = V_{DD}/2$. Draw the small-signal model for this circuit and compute its DC gain. (3p)

b) State one reason why it is uncommon to use the minimum channel length of a transistor in an analog circuit. (1p)

c) State benefits and drawbacks of using a fully differential compare with a single-ended circuit structure in an integrated analog circuit. (3p)

d) Compute the input impedance of the circuit shown in Figure 5.2, i.e., $Z_{in}(s) = V_{in}(s)/I_{in}(s)$. Assume that the operational amplifier is ideal. Further, select appropriate components (resistor or capacitors, but not inductors) for the impedances, Z_i, so that the circuit realizes an inductor. (3p)

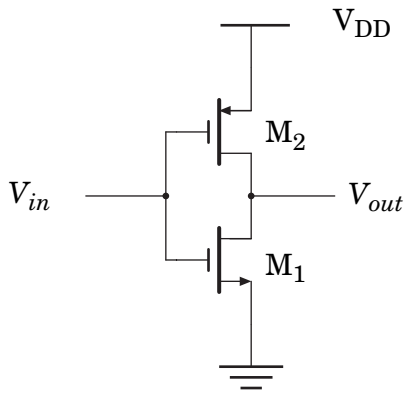

Figure 5.1 A CMOS inverter used as a analog amplifier

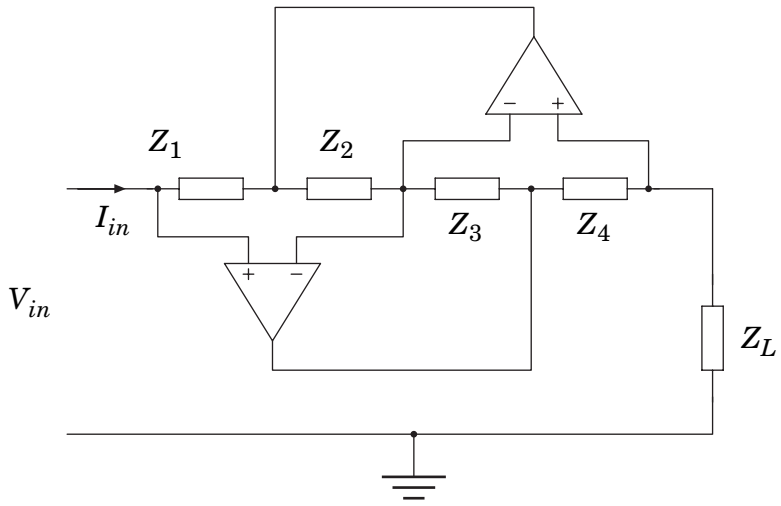

Figure 5.2 A circuit that can be used to realize an inductor.

Transistor formulas and noise

CMOS transistors

Current and threshold voltage formulas and operating regions for an NMOS transistor

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

All regions:

$$V_T = V_{T,0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$