# Written Test
# TSEI30,
# Analog and Discrete-time Integrated Circuits

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| Date | Mars 12, 2003 |
| Time: | 14 – 18 |
| Place: | U1 and T2 |
| Max. no of points: | 70;<br>50 from written test,<br>5 for project, and 15 for assignments. |
| Grades: | 30 for 3, 42 for 4, and 56 for 5. |
| Allowed material: | All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design |
| Examiner: | Lars Wanhammar. |
| Responsible teacher: | Robert Hägglund.<br>Tel.: 0705 - 48 56 88. |
| Correct (?) solutions: | Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor. |

## Good Luck!

# Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

# Exercise

**1. Large-signal analysis**

a) Sketch the output voltage as a function of the input voltage ($V_{out} = f(V_{in})$) for the input voltage between ground and the power supply voltage. (3p)

b) Determine the operation region of the transistor in the different parts of the figure sketched in a). (3p)

c) Determine the input and output voltage when the transistor switches from operating in the saturation region to operate in the linear region. Neglect the influence of the channel-length modulation. (4p)

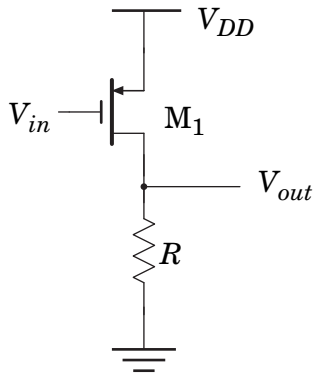


***Figure 1.1*** A simple amplifier structure with resistive load.

## 2. Small-signal analysis

The circuit shown in Figure 2.1 should be used as a key component in an amplifier. In order to understand its limitation we need to analyze its small-signal behavior. Do **not** neglect the influence of the bulk effect.

a) The circuit can be decomposed into two different parts, i.e., the PMOS transistor and the resistor $R_1$ (shown in Figure 2.1 b) and the NMOS transistor and the resistor $R_2$. The PMOS transistor and $R_1$ can in a small-signal sense be reduced to a resistor (as shown in Figure 2.1 c). Derive an expression for the equivalent resistor, $R_{eq}$. (4p)

b) Derive the small-signal gain and the first pole of the amplifier shown in Figure 2.1 a), where the PMOS transistor and $R_1$ is substituted with an equivalent resistance, $R_{eq}$. The expressions should be functions containing $R_{eq}$. (6p)

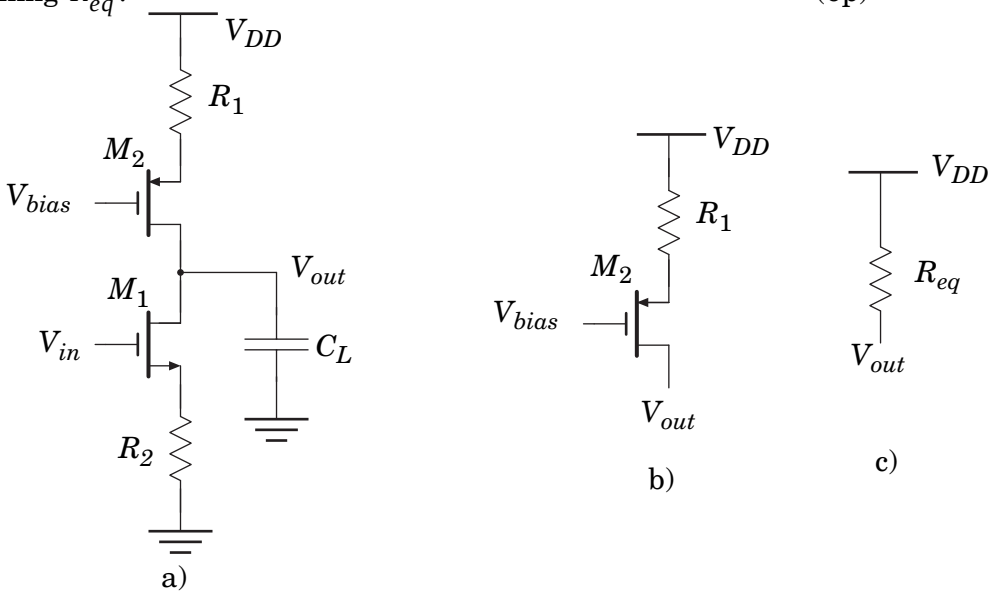


***Figure 2.1*** An amplifier. a) The whole amplifier. b) The PMOS and resistor part. c) The equivalent small-signal circuit of b).

## 3. Macro blocks

The amplifier shown in Figure 3.1 is an operational amplifier. Its transfer function is

$$A(s) = \frac{A_0}{1 + \frac{s}{p_1}} \tag{3.1}$$

a) Derive the transfer function from the input to the output of the circuit, $H(s) = V_{out}(s)/V_{in}(s)$. (4p)

b) The transfer function of the circuit can be written in the form

$$H(s) = K\frac{A(s)}{1 + \beta(s)A(s)} \tag{3.2}$$

derive the feed back factor $\beta(s)$. (4p)

c) Derive the transfer function of the building block in Figure 3.1 when $A(s) \to \infty$. (2p)

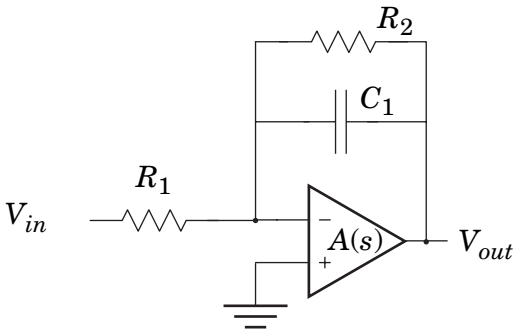


***Figure 3.1*** An active-RC circuit.

## 4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1 is shown in Figure 4.1. The value of $V_2$ changes only at time $t$, $t + 2\tau$, $t + 4\tau$, and so on, i.e., $V_2(t) = V_2(t + \tau)$.

a) Express the output voltage, $V_{out}(z)$, for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA is ideal. (4p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (2p)

c) The amplifier has a finite gain, $A$. Derive the output voltage, $V_{out}(z)$, for clock phase 1. (4p)

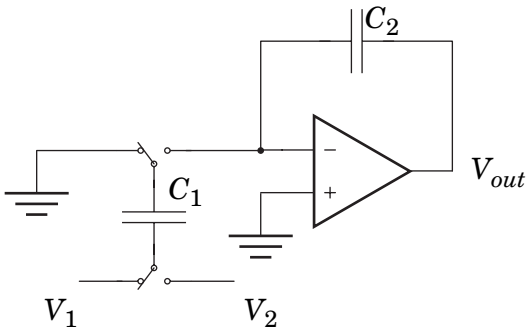


***Figure 4.1*** A switched-capacitor circuit in clock phase 1.

## 5. A mixture of questions

a) Derive the common-mode and output ranges of the circuit shown in Figure 5.1. (4p)

b) The output of a fully differential circuit can be written as

$$V_{out,\,p} = a_p(V_{in,\,p} - V_{in,\,n}) + b_p(V_{in,\,p} - V_{in,\,n})^2 + c_p(V_{in,\,p} - V_{in,\,n})^3$$

$$V_{out,\,n} = a_n(V_{in,\,n} - V_{in,\,p}) + b_n(V_{in,\,n} - V_{in,\,p})^2 + c_n(V_{in,\,n} - V_{in,\,p})^3$$

where $a_p \approx a_n$, $b_p \approx b_n$, and $c_p \approx c_n$ (in a perfectly matched circuit, the equality in the equations holds, but here we have a small mismatch.)

Derive the differential and the common-mode output voltage. From your result, what are the benefits of using fully differential compared to single-ended structures? (4p)

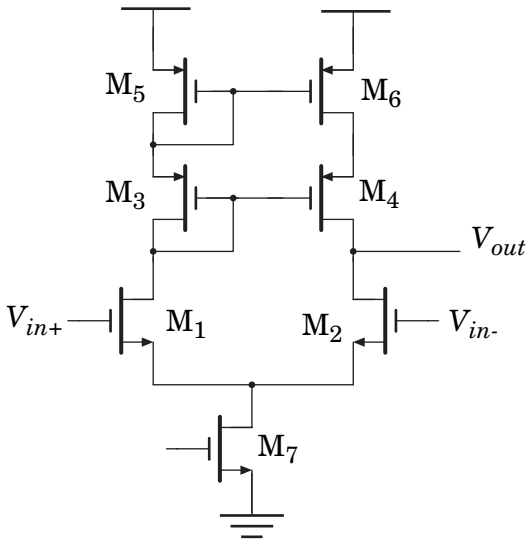


***Figure 5.1*** A CMOS amplifier circuit.

c) In analog circuit design it is not common to use the minimum channel length of the transistors. Give two reasons for this. (2p)

# Transistor formulas and noise

## CMOS transistors

### Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

### Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

## Circuit noise

### Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

### Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$