Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	August 26, 2002
Time:	14 - 18
Max. no of points:	70; 50 from written test, 5 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The NMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Exercise

1. Large signal modelling

a) Sketch the output voltage as s function of the input voltage for the circuit shown in Figure 1.1. The input voltage is in the interval between *gnd* and V_{DD}. (4p)

b) Derive the minimum and maximum voltage at the input so that the transistor operates in the saturation region. Express these voltages as functions of the power supply voltage, resistance, and transistor parameters but not the current through the transistor. To reduce the computation time in this exercise, ignore the channel-length modulation. (6p)

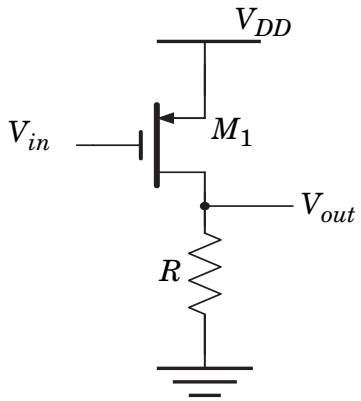

Figure 1.1 A simple gain stage.

2. Basic building block

A common source amplifier with two cascodes is shown in Figure 2.1 where V_{b1} and V_{b2} are bias voltages.

a) Derive the DC gain of the circuit shown in Figure 2.1. (4p)

b) Describe one way to double the DC gain without increasing the total size of the amplifier. How much must the parameters be increased/ decreased? (4p)

c) Compare this structure with a gain boosted single cascoded common source amplifier. What are the benefits and drawbacks of each structure? (2p)

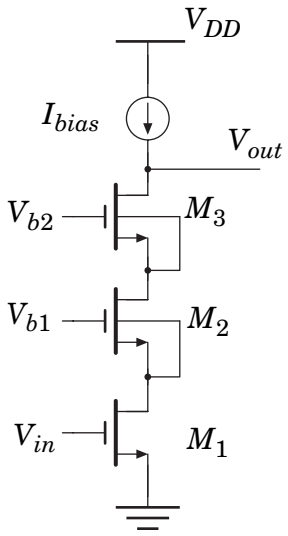

Figure 2.1 A CMOS gain stage.

3. An operational amplifier in a context

a) Derive the DC gain and the poles of the circuit shown in Figure 3.1. Assume that $C_1 R_1 > 1/p_1$. Motivate all your approximations carefully. The gain of the amplifier is given by: (6p)

$$A(s) = \frac{A_0}{1 + \frac{s}{p_1}}$$

b) Derive an expression for the phase at the unity-gain frequency of the closed loop system (V_{out}/V_{in}). Use design parameters as R_1, C_1, A_0, p_1, ... (4p)

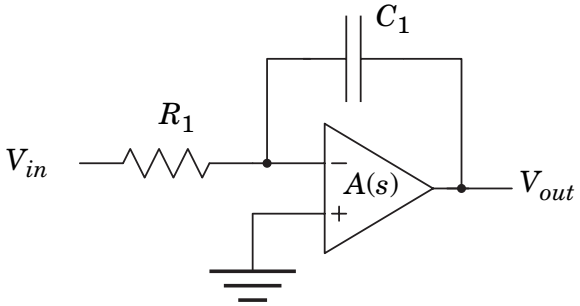

Figure 3.1 An operational amplifier in a context.

4. An SC circuit

A switched capacitor circuit in clock cycle 1 is shown in Figure 4.1.

a) Derive the transfer function for the clock cycle 1 of the switched capacitor circuit shown in Figure 4.1, i.e., $V_{out}(z)/V_{in}(z)$. Assume that the OTA is ideal except that it suffers from an offset voltage, V_{os}. (8p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (2p)

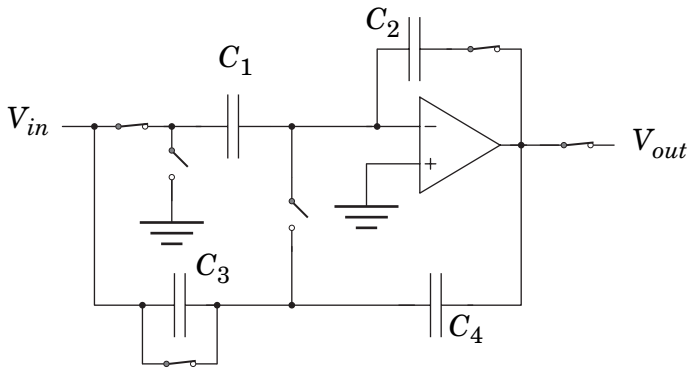

Figure 4.1 A switched capacitor circuit.

5. A mixture of questions

a) In a transconductance-C filter we need to match two capacitors of the values, 100pF and 150pF, respectively. What do you have to do to achieve accurate matching? Sketch a "floor plan" of the capacitor-array to achieve accurate matching between the capacitors. (3p)

b) A differential gain stage as the one shown in Figure 5.1 is to be implemented on silicon. In what types of processes (p-substrate and n-well, n-substrate and p-well, twin well process) is it possible to implement this amplifier? (2p)

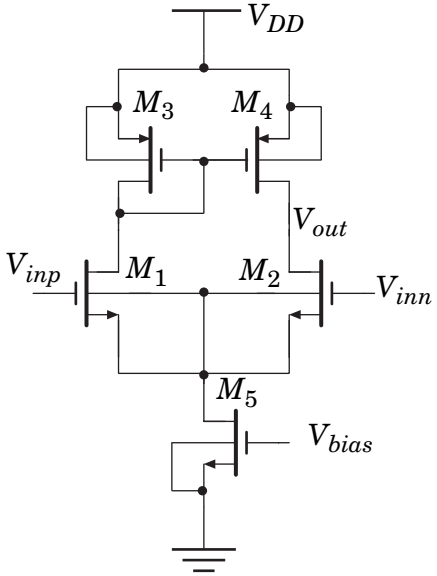

Figure 5.1 A differential gain stage.

c) Derive the power supply rejection ratio from the positive power supply of the amplifier shown in Figure 5.2. Neglect the influence of the capacitive parasitics. (3p)

d) Why do we design the transistors in Figure 5.2 to operate in the saturation region? (1p)

e) What is a CMFB circuit? Why and when do we use such circuits? (1p)

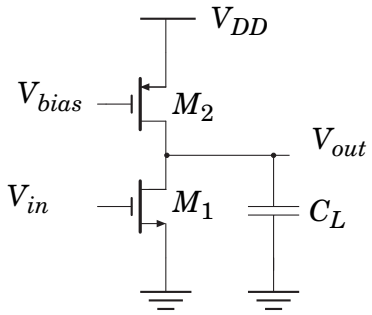

Figure 5.2 A basic building block.

Transistor formulas and noise

NMOS transistor

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$