Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	April 15, 2002
Time:	14 - 18
Place:	T1 and T2
Max. no of points:	70; 50 from written test, 15 for project, and 5 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Exercise

1. Basic CMOS building block

The circuit shown in Figure 1.1 is to be designed in a special process where the threshold voltages and the channel length modulations are equal for the pmos and nmos transistors.

a) Design the circuit to achieve the voltages $V_{out} = V_{in} = V_{DD}/2$ when $V_{DD} > 2V_T$. (4p)

b) Sketch the output voltage, V_{out}, as a function of the input voltage, V_{in}, for $0 < V_{in} < V_{DD}$. Indicate the operation regions of both transistor in the graph. (4p)

c) Express the output voltage as a function of the input voltage when both transistors are operating in the saturation region. (2p)

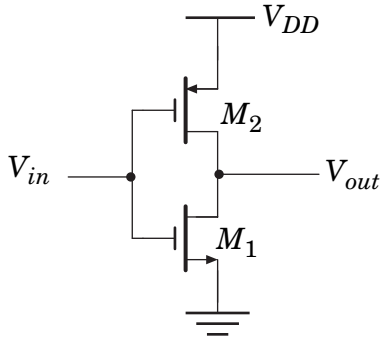

Figure 1.1 A CMOS amplifier.

2. Small signal analysis

Assume that all transistors, in Figure 2.1, are biased so that they are operating in the saturation region. Neglect the influence of the parasitic capacitances.

a) What do we call the circuit shown in Figure 2.1? (1p)

b) Draw the small signal equivalent for the amplifier. (1p)

c) Derive the transfer function, $v_{out}(s)/v_{in}(s)$, of the circuit. (3p)

d) What will happen to the output impedance if ...

... the current through the gain stage is increased?

... the width of transistor M_2 is decreased?

... the width of transistor M_1 is decreased?

Also, describe the impact on the bandwidth and the DC gain for each modification of the circuit. (5p)

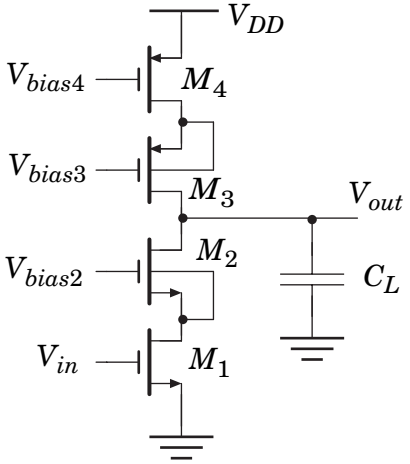

Figure 2.1 A CMOS gain stage.

3. Operational amplifier

The transfer function for the circuit shown in Figure 3.1 can be expressed as in (3.1). The amplifier is assumed to have infinite input impedance and zero output impedance.

$$H(s) = \frac{v_{out}(s)}{v_{in}(s)} = K(s)\frac{A(s)}{1+\beta(s)A(s)} \tag{3.1}$$

a) Derive the transfer function of the circuit shown in Figure 3.1 and identify the factors $K(s)$ and $\beta(s)$. (4p)

b) Assume that $Z_1 = R_1$, $Z_2 = R_2$, which yields a constant β, and that

$$A(s) = \frac{A_0}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} \tag{3.2}$$

where the poles are well separated, i.e., $|p_2| \gg |p_1|$. Determine the feedback factor, β, to get $\phi_m = 75°$ where $\phi_m = 180° + \arg(\beta \cdot A(j\omega_u))$ and ω_u is defined by $|\beta \cdot A(j\omega_u)| = 1$

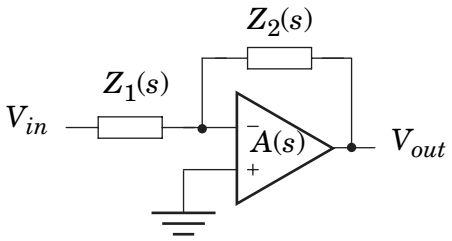

Figure 3.1 An operational amplifier in a feedback configuration.

Hint: Assume that

$$\arg\left(1 + j\frac{\omega_u}{p_1}\right) = 90° \tag{3.3}$$

(6p)

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4. Switched capacitor

A switched capacitor circuit in clock cycle 1 is shown in Figure 4.1. The input signal is constant on the time interval
$V(t + (2n + 1)\tau) = V(t + (2n + 2)\tau)$.

a) Derive the transfer function for the switched capacitor circuit shown in Figure 4.1, i.e., $V_3(z) = \alpha V_1(z) + \beta V_2(z)$. Assume that the OTA is ideal. The transfer function should only contain integer power of z. (4p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (2p)

c) Assume that the OTA suffers from finite gain, A. Derive the output voltage $V_3(z)$ as a function of relevant circuit parameters. (4p)

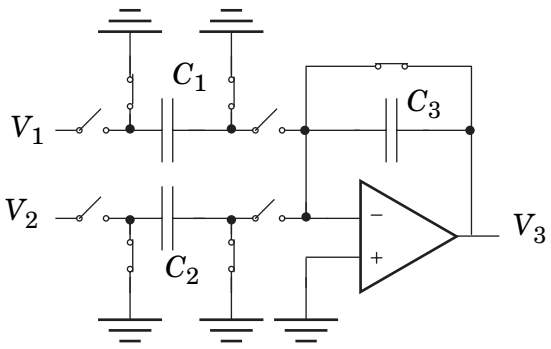

Figure 4.1 A switched capacitor circuit in clock phase 1.

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5. CMOS Building blocks

a) Linus has designed an operational transconductance amplifier, OTA, but he needs it to drive resistive load and, therefore, he needs to design an operational amplifier, OP. How can he transform the OTA into an OP? (2p)

b) What is the function of the circuit shown in Figure 5.1? (1p)

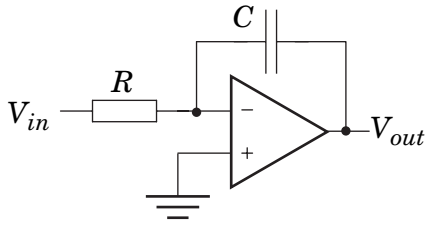

Figure 5.1 A circuit.

c) Derive an expression for the slew rate in the circuit shown in Figure 5.2. (2p)

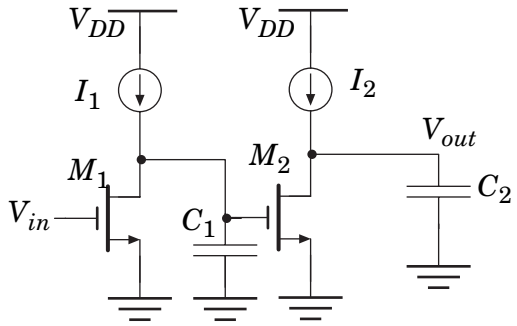

Figure 5.2 A CMOS circuit.

d) Describe the benefits and drawbacks of a fully differential compared to a single-ended circuit. (2p)

e) Express the output range, OR, and the common-mode range, CMR, for the differential gain stage shown in Figure 5.3 using relevant design parameters such as α, I_D. (3p)

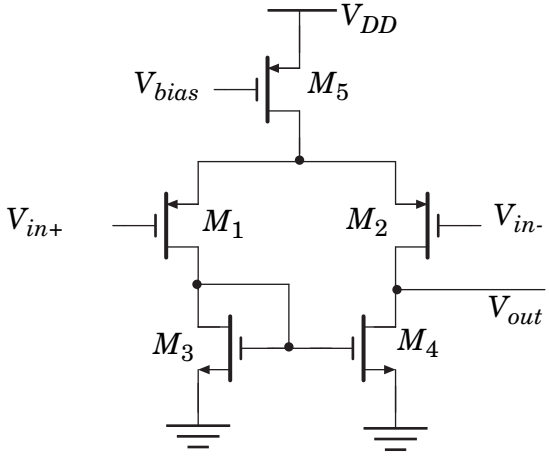

Figure 5.3 A single-ended differential gain stage.

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$