Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	March 13, 2002
Time:	8 - 12
Place:	Kårallen and U6
Max. no of points:	70; 50 from written test, 15 for project, and 5 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Exercise

1. Basic CMOS building block

a) Sketch the output voltage as a function of the power supply voltage, V_{DD}, for V_{DD} between 0 and 5 threshold voltages. The input voltage is a DC voltage, $V_{inDC} = V_{DD}/2$. (3p)

b) Determine the values of V_{DD} for which the transistor is operating in the

... cut-off region

... linear region

... saturation region. (5p)

c) State two reasons why we seldomly use amplifiers with resistive load in analog integrated circuits. (2p)

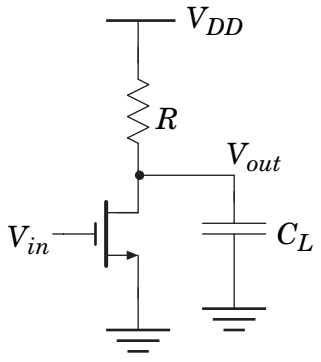

Figure 1.1 A CMOS gain stage.

2. Small signal analysis

Assume that all transistors are biased so that they are operating in the saturation region.

a) Derive the small signal transfer function from the input to the output. All parasitics except the source gate capacitor of transistor M_3 can be neglected. Express the DC-gain and the poles of the circuit. (4p)

b) Describe two ways to increase the phase margin. What will happen to the other performance parameters? (3p)

c) What is the range of the possible values for V_{bias2} to ensure that all transistors are operating in the saturation region? (3p)

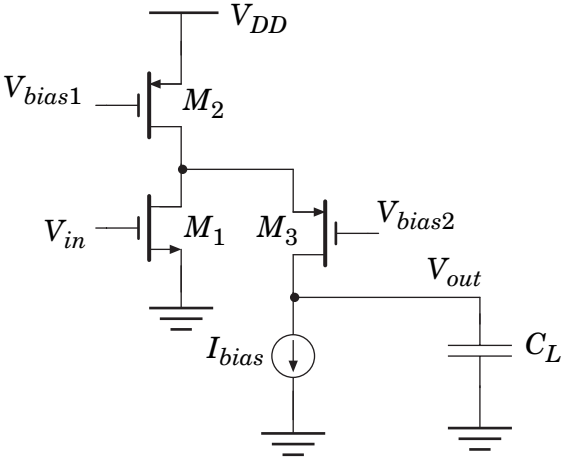

Figure 2.1 A CMOS gain stage.

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3. Operational amplifier

We have designed the following OTA in shown in Figure 3.1. All transistors are operating in the saturation region. The transfer function is given by

$$A(s) = \frac{\dfrac{g_{m8}}{g_{m4}}\dfrac{g_{m1}}{\dfrac{g_{ds8}g_{ds10}}{g_{m10}} + \dfrac{g_{ds12}g_{ds14}}{g_{m12}}}}{1 + \dfrac{sC_L}{\dfrac{g_{ds8}g_{ds10}}{g_{m10}} + \dfrac{g_{ds12}g_{ds14}}{g_{m12}}}} \tag{3.1}$$

No capacitive parasitics are taken into account.

a) Derive the common-mode and output ranges. Use relevant design parameters such as I, W, and L. (3p)

b) How do we increase the output resistance of the circuit? (3p)

c) This circuit is not the best circuit to be used when we want to drive small resistive loads. Why? (2p)

d) Assume that the amplifier is a one pole system with the following transfer function:

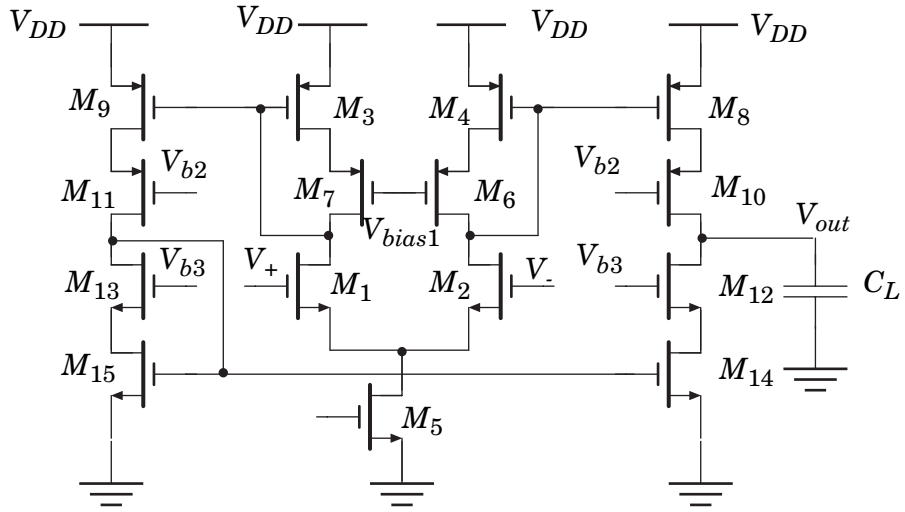

Figure 3.1 An operational transconductance amplifier.

$$A(s) = \frac{A_0}{1 + \frac{s}{p_1}} \tag{3.2}$$

Derive the expression for the unity-gain frequency. What will the DC gain be of closed loop system if the feedback factor $\beta = 0.5$ if $A_0 \gg 1$? (2p)

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4. Switched capacitor

A switched capacitor circuit in clock cycle 1 is shown in Figure 4.1.

a) Derive the transfer function for the switched capacitor circuit shown in Figure 4.1, i.e., $V_2(z)/V_1(z)$. Assume that the OTA is ideal. (4p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (2p)

c) Assume that the OTA suffers from an input offset voltage, V_{os}. Derive the output voltage $V_{out}(z)$ for the times t, $t + 2\tau$, $t + 4\tau$ and so on. (4p)

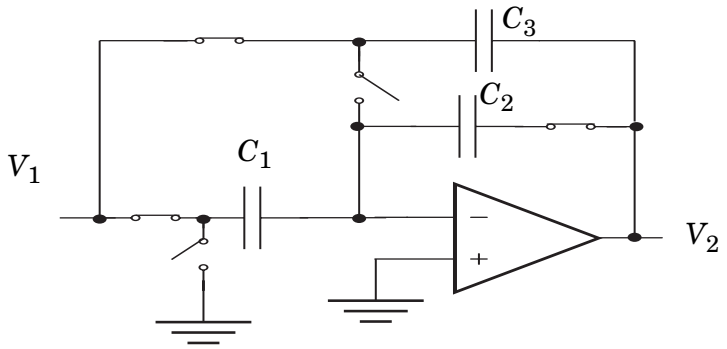

Figure 4.1 A switched capacitor circuit in clock phase 1.

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5. CMOS Building blocks

a) What is the difference between an operational amplifier and an operational transconductance amplifier? (1p)

b) Why do we like to bias all transistors so that they are operating in the saturation region? (1p)

c) Explain advantages and drawbacks of an active-RC integrator compared to a switched capacitor accumulator. (2p)

d) What is transistor matching? Describe two ways to improve the matching between two transistors. (2p)

e) The circuit shown in Figure 5.1a can be enhanced as shown in Figure 5.1b, how is the performance affected in Figure 5.1b compared to Figure 5.1a (gain, poles and zeroes)? (2p)

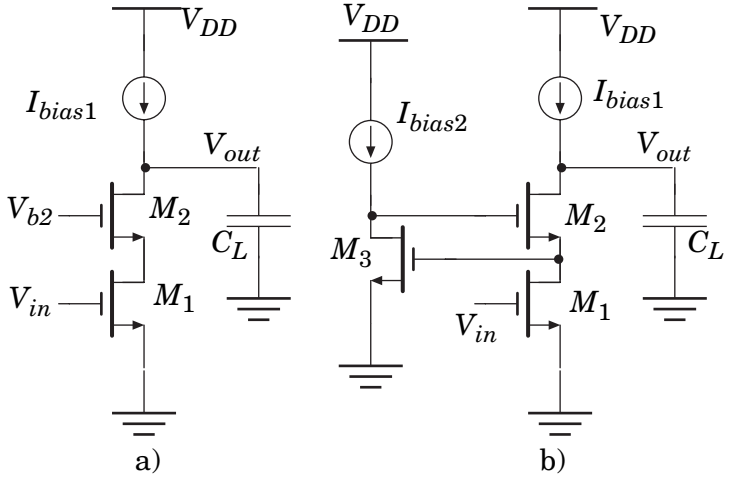

Figure 5.1 Two commonly used gain stages.

f) Linus needs to design a circuit with high gain. He has studied bipolar circuits. In bipolar technology the Darlington amplifier is a common way to increase the gain of the circuit. He is asking you if the circuit shown in Figure 5.2 (A Darlington amplifier where the bipolar transistors have been replaced by CMOS transistors) can be designed to have high gain. What would your recommendation be? (2p)

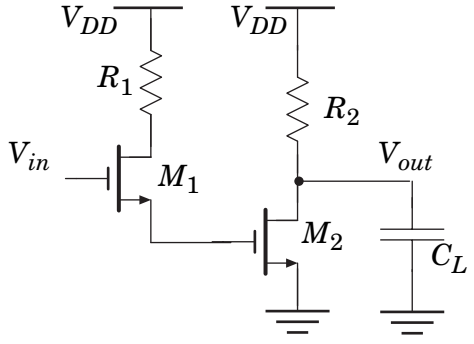

Figure 5.2 A CMOS circuit.

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$