Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	January 11, 2002
Time:	8 - 12
Place:	Kårallen
Max. no of points:	70; 50 from written test, 15 for project, and 5 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. Written material and downloaded web-material except old exams. No textbooks are allowed.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Exercise

1. Basic CMOS building block

a) Assume that a voltage source with an input resistance, R_{in}, as shown in Figure 1.1b is connected to the node V_1. Derive the transfer function from V_{in} to V_{out} in Figure 1.1. Assume that all transistors are operating in the saturation region. (3p)

b) What will happen with the gain and the first pole of the circuit in Figure 1.1 if the width of the transistor M_1 is made larger? (2p)

c) An ideal voltage source is connected to node V_1. Determine the operation regions of the transistor M_1 when node V_1 ramps from V_{dd} to ground. Assume that transistor M_2 operates as an ideal current source delivering the current I_{bias}. Explain how to find the input voltage where transistor M_1 starts to operate in the linear operation region. (3p)

d) Determine the maximum possible output swing for saturated transistors if the bias voltages V_{b1} and V_{b2} are connected to $V_{dd}/2$ and V_1 is connected to ground. (2p)

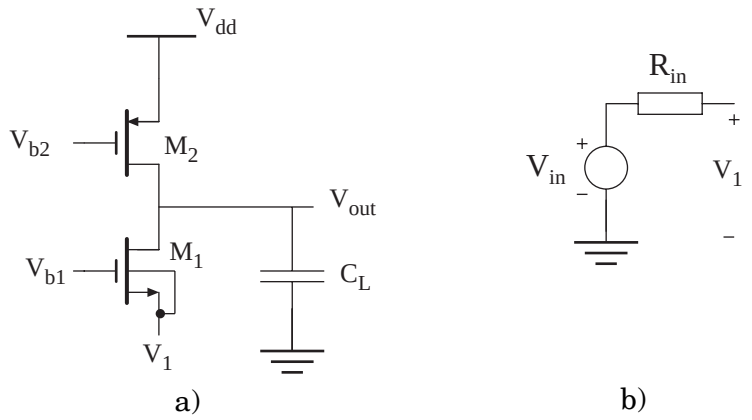

Figure 1.1 a) A CMOS gain stage. b) Input voltage source.

2. Operational amplifier

a) Derive the differential voltage DC-gain and the first pole of the circuit shown in Figure 2.1. No parasitic capacitances need to be considered. (4p)

b) The second pole arises from the parasitic capacitance in node V_x in Figure 2.1. The expression for this pole is $p_2 \approx g_{m7}/C_x$ where C_x is the parasitic capacitance in node V_x.

How do you increase the phase margin...

...if the area is limited?

...if the power is critical?

...if the unity-gain and power are critical?

In each case what are the drawbacks of the circuit performance? (4p)

c) What is slew-rate? Derive the slew-rate of the circuit in Figure 2.1. Motivate your solution carefully. (2p)

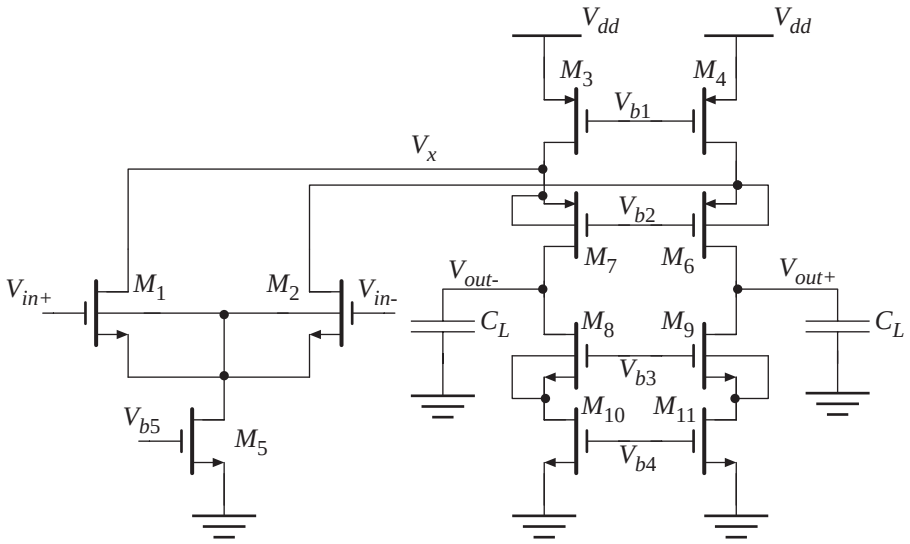

Figure 2.1 A folded cascode gain stage.

3. Noise in CMOS circuits

a) Derive the equivalent output noise of the circuit, shown in Figure 3.1, due to the thermal noise generated by the transistors M_1 and M_2. (5p)

b) Describe two ways to decrease the equivalent output noise by changing relevant design parameters. What will happen to the gain, the unity-gain and the slew-rate of the circuit? (5p)

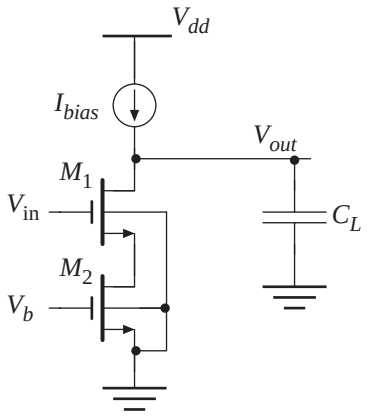

Figure 3.1 A noisy CMOS circuit.

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4. Switched capacitor

a) Derive the transfer function of the switched capacitor circuit shown in Figure 4.1, i.e, $V_2(z)/V_1(z)$. Assume that the operational transconductance amplifier is ideal. (3p)

b) Is the circuit insensitive to parasitics? Motivate your answer carefully. (1p)

c) Assume that the operational transconductance amplifier suffers from finite gain, A, and input offset voltage, V_{os}. Derive the transfer function. (3p)

d) Find the settling time constants, i.e. the speed of the circuit, for both clock phases. Neglect the influence of the switches. (3p)

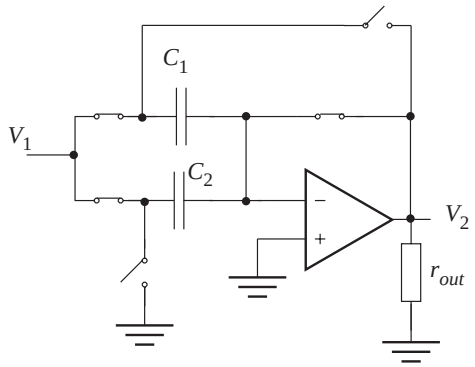

Figure 4.1 A switched capacitor circuit.

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5. CMOS Building blocks

a) In an active RC filter we need to have an operational amplifier with the following specification

Table 1: OPamp specification

Performance parameters	Values
A_0	80dB
f_u	100MHz
C_L	5pF
SR	80V/μs
OR	[0.5 - 2.8]V
CMR	[0.1 - 2.0]V
V_{dd}	3.3V
P_{diss}	<10mW

How would you design the operational amplifier?

Draw the block diagram of the operational amplifier and make a specification of each block in your design, like the one above and the name of the type of building block and the type of the input transistors. (3p)

b) The same task as in a) but here we have an operational transconductance amplifier that will be used in a SC-filter. (2p)

c) Derive the quotient between the output and input resistance of the current mirror shown in Figure 5.1a. An amplifier with gain A is connected between the input and the gate of the transistors. (2p)

d) Derive the PSRR from the positive supply of the circuit shown in Figure 5.1b. Do not forget to take the bulk-effect into account. No parasitics need to be taken into account. Sketch the magnitude of the PSRR with respect to the frequency. (3p)

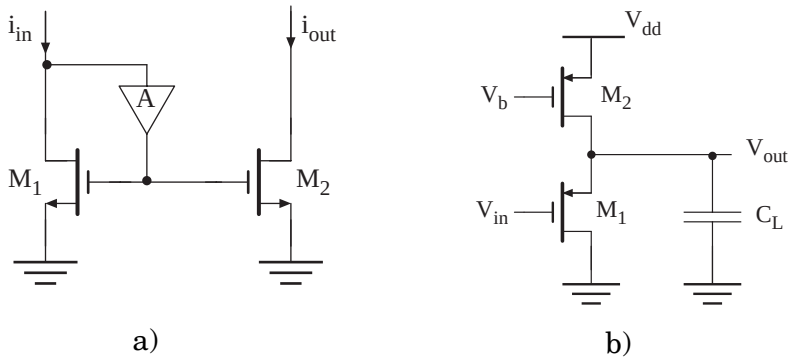

Figure 5.1 a) A CMOS current mirror. b) A CMOS circuit.

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$