

## Written Test

# TSEI30, Analog and Discrete-time Integrated Circuits

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Date: June 9, 2000

Time: 8 - 12

Place: Garnisonen

Max. no of points: 70;  
50 from written test,  
15 for project and 5 for oral test.

Grades: 30 for 3, 42 for 4, and 56 for 5.

Allowed material: No laptops. No text books, such as Johns & Martin "*Analog Integrated Circuit Design*". No dedicated compendia, such as Eriksson "*Aktiva RC-filter och SC-filter*". Pocket calculators are allowed. Written material, tables, downloaded web-material, etc., are allowed.

Examiner: Lars Wanhammar

Responsible teacher: J. Jacob Wikner.  
Tel.: 0705915938

Correct (?) solutions: Solutions and results will be displayed in July 2000.

**Good Luck!**

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## Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no on a brief question. Always motivate your answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

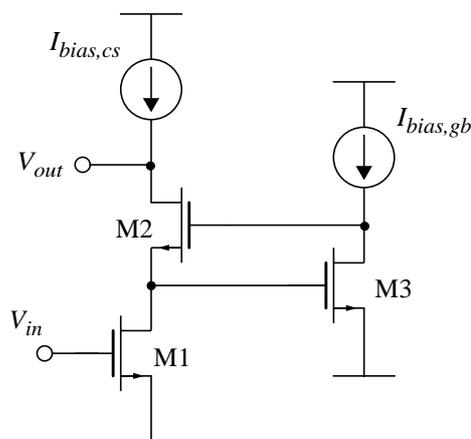
You may answer in Swedish, German, or English.

## Exercises

### 1. CMOS Building Blocks

Consider the CMOS building block in Figure 1. This is a gain-boosting circuit and from the name we obviously understand that the gain is increased. The current sources have an infinite output resistance.

- Express the small-signal gain from the input to the output ( $V_{in}$  to  $V_{out}$ ) as a function of the bias currents, transistor sizes and process parameters. (4p.)
- Find the possible maximum/minimum input and output voltages that keep the transistors in their saturation regions. What design parameters determine the swing? (4p.)
- How should you choose the DC voltage on the gate of M2 in order to maximize the gain? (2p.)



**Figure 1** Gain-boosting circuit.

10 points

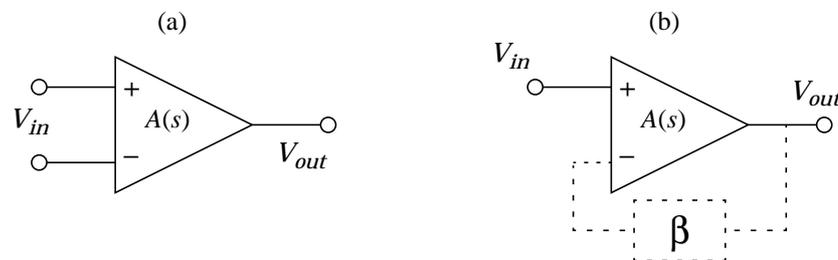
## 2. Operational Amplifier

Consider the operational amplifier in Figure 2 (a). Assume that its transfer function is given by

$$A(s) = \frac{A_0}{\left(1 + \frac{s}{p_1}\right) \cdot \left(1 + \frac{s}{p_2}\right)}$$

The poles are well separated but we do not know how  $p_2$  relates to the unity-gain frequency.

- Derive how  $p_2$  is a function of the unity-gain frequency. (2p.)
- Assume the OP is used in a feedback loop with the feedback factor  $\beta$  as shown in Figure 2 (b). Derive the total transfer function and find a closed expression on the phase margin. Sketch the phase margin as function of  $\beta$ . (5p.)
- In a switched-capacitor circuit, why should we choose a phase-margin higher than 70 degrees? (3p.)



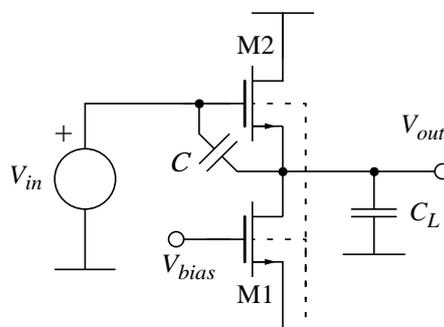
**Figure 2** Operational amplifier in (a) open-loop and (b) closed-loop.

10 points

## 3. Surprise - CMOS building block

Consider the circuit in Figure 3. The input voltage source has an output resistance  $R_s$ .

- Find the transfer function of the circuit. What is the DC gain? (3p.)
- Under what circumstances will the output impedance of the circuit become approximately inductive? Do not forget the parasitic capacitances. (7p.)



**Figure 3** CMOS circuit.

10 points

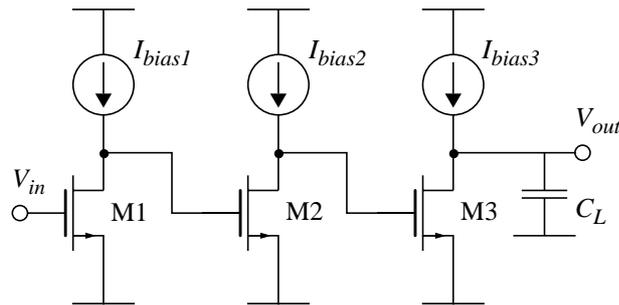
**4. Noise**

Consider the three-stage circuit in Figure 4. Only consider thermal noise from each transistor. The current sources are noise free. Let the output load capacitance be  $C_L$  and parasitic capacitances are only given by the gate-source capacitances.

a) Derive the total output noise power. (3p.)

b) Derive the total equivalent input-referred noise. Hence, assume no internal noise and only one noise source at the input transistor. (2p.)

c) Discuss – by using relevant circuit parameters – how you should minimize the output noise power and how it affects the gain and bandwidth of the circuit. (5p.)



**Figure 4** Noisy multi-stage circuit.

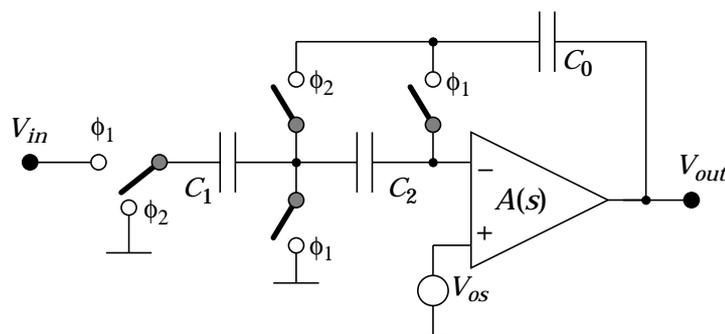
10 points

**5. Switched Capacitor**

Consider the switched-capacitor circuit in Figure 5. Assume that the operational amplifier has a finite gain and an input voltage offset error,  $V_{os}$ .

a) Find the transfer function of the circuit. Sketch the ideal output signal (infinite gain and no input offset voltage) and the non-ideal output signal, hence how does the finite DC gain and input offset voltage affect the result? (5p.)

b) What are the feedback factors at the two phases? Assume that the OP uses a differential stage at the input and **do not** forget parasitic capacitances. During which phase is the settling time constant smallest? (5p.)



**Figure 5** Switched-capacitor circuit.

10 points

## Transistor formulas and noise

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### CMOS transistors

#### Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \quad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \quad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \quad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

#### Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \quad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_G - V_T - V_D)$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} = \sqrt{\mu_0 C_{ox} \frac{W}{L} I_D} \quad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

### MOS transistor noise

#### Thermal noise

The thermal noise spectral density at the gate is  $\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$

#### Flicker noise

The flicker noise spectral density at the gate is  $\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$

#### Parasitics

In the saturation region, the parasitic capacitances on the MOS transistor are approximately given by

$$C_{gs} \approx \frac{2}{3} \cdot W \cdot \left( L + \frac{3}{2} \cdot L_{ov} \right) \cdot C_{ox}, \quad C_{gd} \approx WL_{ov} \cdot C_{ox}$$