Linköping University
INSTITUTE OF TECHNOLOGY

TSEI12, Analog Design, Second course, 2013-08-26

Written exam, TEN1

Date, time	**2014-03-19, 08.00 - 12.00**
Location(s)	G36
Responsible teacher	J Jacob Wikner, 070-5915938
Aid	Any written and printed material, including books and old exams. Note! No pocket calculators, no laptops, no iPods, no telephones, no internet connection.
Instructions	A maximum of 25 points can be obtained from the written exam. Three points can be obtained from quizzes. In total: 10 points are required to pass, 15 for a grade four, and 20 for a grade five. *x Hint! **Be strategic** when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...* Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" clear derivations are understood (and not only text). Note that the questions in the exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully! *x Notice that even though you may not fully know the answer, add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available within two weeks from exam date (hopefully...)

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1. CMOS, ETC. (5 P)

Consider the circuit in Figure 1.1 below. Derive, explain, and elaborate on the following:

1) The good-old story: Output impedance, DC gain, bandwidth, unity-gain frequency, i.e., the transfer function with identified components.

2) Now, when you did 1) why not present an AC signal schematic

3) Sketch the DC transfer characteristics as a function of V_{in} and V_{bias}. Indicate important break points in the graph. Indicate operating regions for the transistor.

4) In 3) - where do you want to put the DC operating point?

Assume all transistors operate in their saturation regions.

- *Minimize the number of parameters in your solutions and use large-signal parameters.*
- *Make valid assumptions and **motivate them well**.*
- *Illustrate your results with example values (e.g. in Volts) and diagrams.*

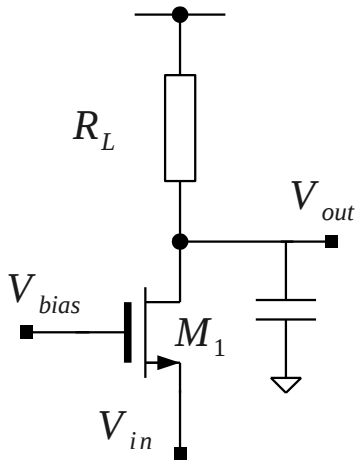

Figure 1.1: Some circuit with some stuff connected to it.

- *This exercise will show that you have understood basic operation regions. Obtainable voltage swings for a CMOS circuit, etc.*
- *Did you motivate all the assumptions well?!*

2. NOISE (5 P)

Consider the circuit in Figure 2.1. It is a you-know-what. All transistors are noisy. To save yourself time, make some educated assumption about bandwidth (which one?)

> Derive a compact expression of the **total output noise power**. Be a **bit creative** to save yourself some time and derive all gate transfer functions at the same time!

Make valid assumptions and motivate them well! Illustrate your results by sketching the corresponding PSD in different steps of your solutions.

- ***Finding a compact expressions implies: "Minimize the number of parameters in your expression".***

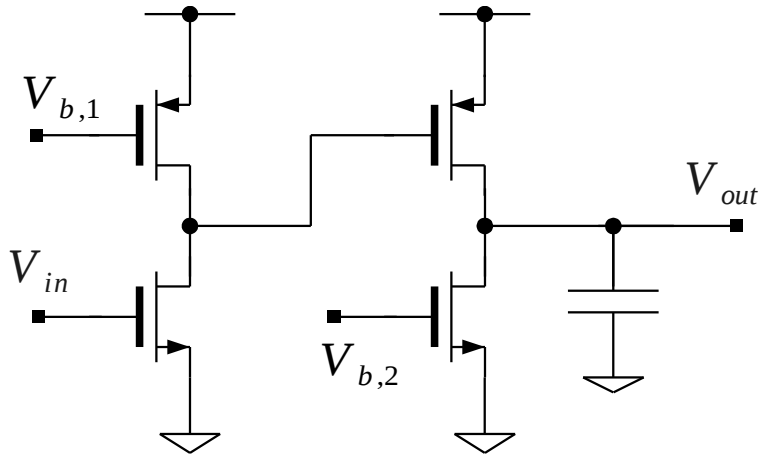

Figure 2.1: Phew! Four transistors...

- *Don't forget that you have to consider the **total noise power** at the output.*
  Hint: use noise brickwall bandwidth: $p_1/4$ (see for example the course books).
- *The noise voltage of a resistance is $v_R^2(f) = 4kTR$*
- *Can you spot the clever trick on the output? How to handle R_L ?*

3. OP/OTA, STABILITY (5 P)

Consider the configurations in Figure 3.1. There are a set of two-stage amplifiers (cascaded). You probably recognize the pictures from your material. Clearly we see different compensation methods.

We now want you to elaborate on the different compensation methods, when they are used, why, what the drawbacks are, etc. Make a nice table, indicated "properties", "pros", and "cons" with the structures. Introduce names, etc., to simplify the notations in your answers.

What are the resistors doing there in the lower two figures?

Your answers should of course be supported by diagrams as well as formulas.

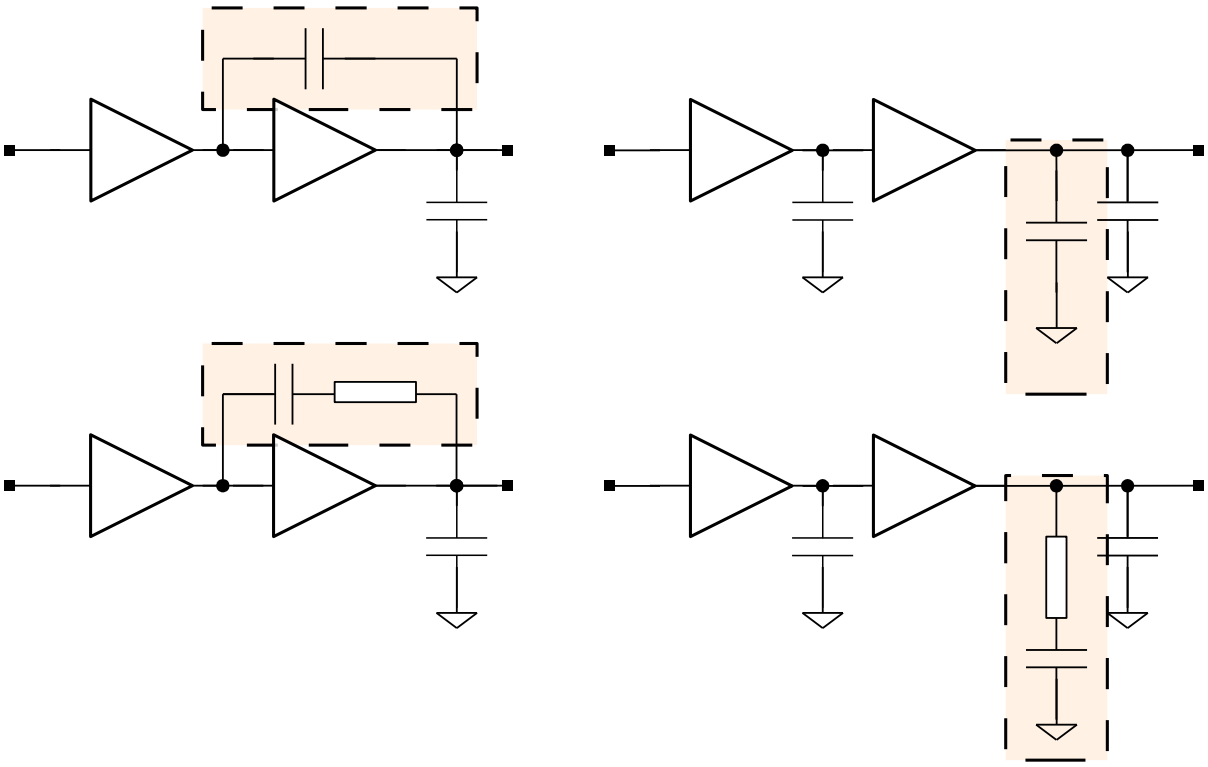

Figure 3.1: Different amplifier configurations.

- ✗ *And once again! Do not forget to present your results properly!*
- ✗ *Notice that you have quite some help in the handouts from the course...*

4. TRANSMISSION LINES (5 P)

Consider the circuit in Figure 4.1. It has a transmitter and a receiver on two chips. The transmission line is on a PCB with a good ground plane. The transmitter has an output resistance of R_{out} and the receiver has an input resistance of R_{in}. The transmission line has a characteristic impedance of Z_0. The length of the line is 8 cm, and the propagation speed through the line is $v = 2 \cdot 10^8$ m/s.

Further on, we also know that: $R_{out} = 150$ Ohm, $Z_0 = 50$ Ohm, and $R_{in} = 200$ Ohm. The transmitter will ideally output 1-V voltage pulses with a very short rise/fall time, internally.

1) Once the pulses start to be transmitted over the line, sketch the diagram showing the voltage at the receiver input **as function of time.**

2) What are the reflection coefficients at the receiver and transmitter?

You are allowed to modify the PCB in a way that you can add termination in series and parallel, both at source and sink.

3) Modify the PCB such that you have maximum power transfer from the transmitter to the receiver.

4) Modify the PCB such that you have a minimum number of reflected waves traveling back-and-forth.

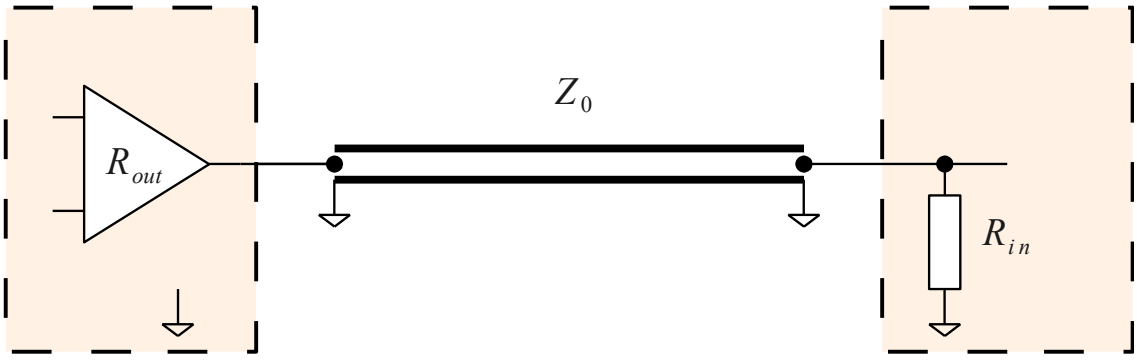

Figure 4.1: A circuit communicating with another circuit over a transmission line.

- *Just use approximate values... and sketch does not mean to draw with infinite accuracy...*

5. POWER SYSTEMS, TIMING, MISC (5 P)

ᵡ So we have seen this exercise a couple of times, but still, it makes sense to revisit it.

Consider the decoupling (bypass) capacitors in Figure 5.1. They are typically used to filter out any high-frequency noisy signals along a supply wire. In the figure, we also see the model of the decoupling capacitor with the nonideal components ESR and ESL.

Assume that we need a total capacitance value of C_{tot} . It could for example be done by adding two capacitors, C_0 and C_1 , such that $C_{tot}=C_0+C_1$. The C_0 and C_1 values can be different, but the ESR and ESL are the same for the two.

From the course, and course book, we know that we should make a certain choice on C_0 and C_1 for "best performance". But how and why?

1) How should we select C_0 and C_1 to form C_{tot} ?

2) ... but why?

Hint! Derive the total impedance between VDD and GND and observe the expression. You might have to do a certain assumption to be able to analyze the formulae. Notice that there might be quite a lot of scribbling to derive the expression, but they are straight-forward per se.

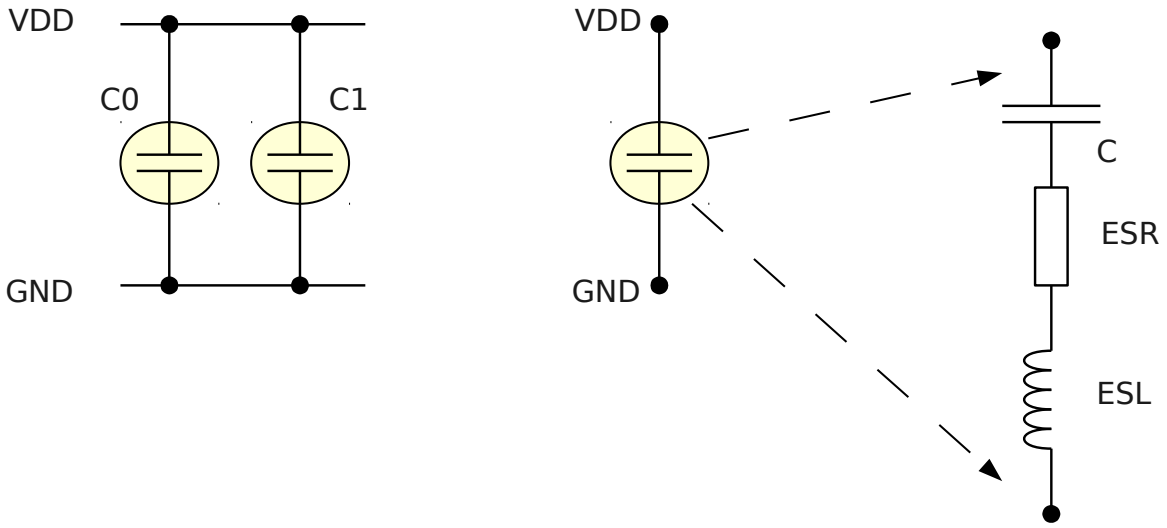

Figure 5.1: Two decoupling capacitors in parallel (left) and their model (right).