Written Test

Course code: TSEI05, Exam code: TEN1

Analog and Discrete-time Integrated Circuits (ISY)

Date:	August 22, 2009
Time:	14-18
Place:	TER1
Number of exercises:	5 (5 points max. for each exercise)
Grades:	10p for 3 (ECTS: C), 15p for 4 (ECTS: B), and 20p for 5 (ECTS:A).
Allowed material:	All types of calcuclators except laptops. All types of official tables and handbooks. Textbooks: Johns & Martin: Analog Integrated Circuit Design. Razavi: Design of Analog CMOS Integrated Circuits. Sedra&Smith: Microelectronic Circuits. Molin: Analog elektronik. Dictionaries.
Examiner and responsible teacher:	Sune Söderkvist
Course administrator:	Sune Söderkvist. Tel.: 281355, mail: sune@isy.liu.se
Visiting today:	Around 15.30 and 17.00 a.m.
Corrrect (?) solutions:	Solutions will be on the webb home page for the couse.

Graded exams are returned on examinator's office times, tuesdays and fridays at 11.00-13.00, during week no. 37 and 38.

Students instructions

- The CMOS transistor operation regions, small-signal parameters, and noise characteristics are found on the last page of this exam.
- Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas etc., otherwise no or fewer points will be given.
- You may write down your answers in Swedish or English.

Good Luck!

Exercise 1.

In this example we will study the small-signal properties of the capacitive-loaded amplifier in **Figure 1**. Assume that the transistors small-signal parameters are g_{m1}, g_{mbs1}, g_{ds1} and g_{m2}, g_{mbs2}, g_{ds2} respectively.
Sketch a small-signal equivalent circuit and determine an exact expression for the transfer function $H(s) = V_{out}(s)/V_{in}(s)$. The bulk effect can **not** be neglected. However, all capacitors but C_L can be neglected. Also, determine the DC gain.

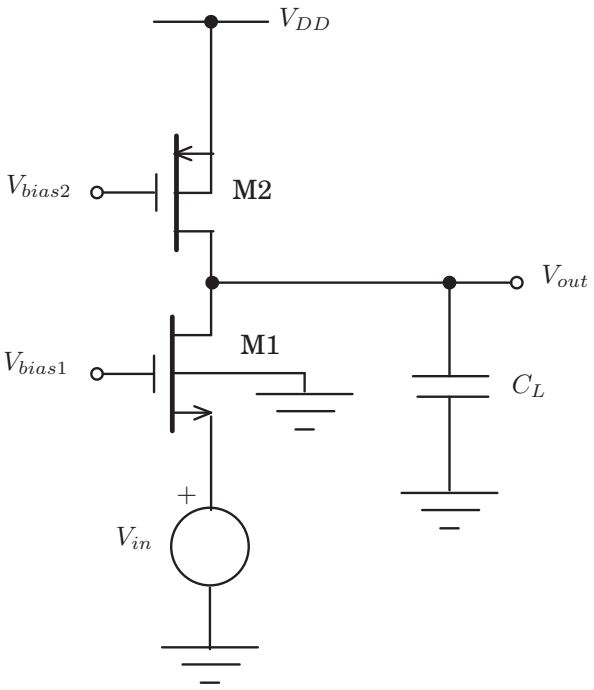

Figure 1: Gain stage.

Exercise 2.

Show that, for appropriate value of V_{bias}, equal voltage at the output and input can be obtained for the cascode stage i **Figure 2**. Assume that both transistors are operating in the saturated region. The channel-length modulation can be neglected.
The transistors **M1** and **M2** have threshold voltages V_{tn} and V_{tp} respectively.
The expression for V_{bias} may include V_{in}, V_{tn} and V_{tp}; no other voltages.

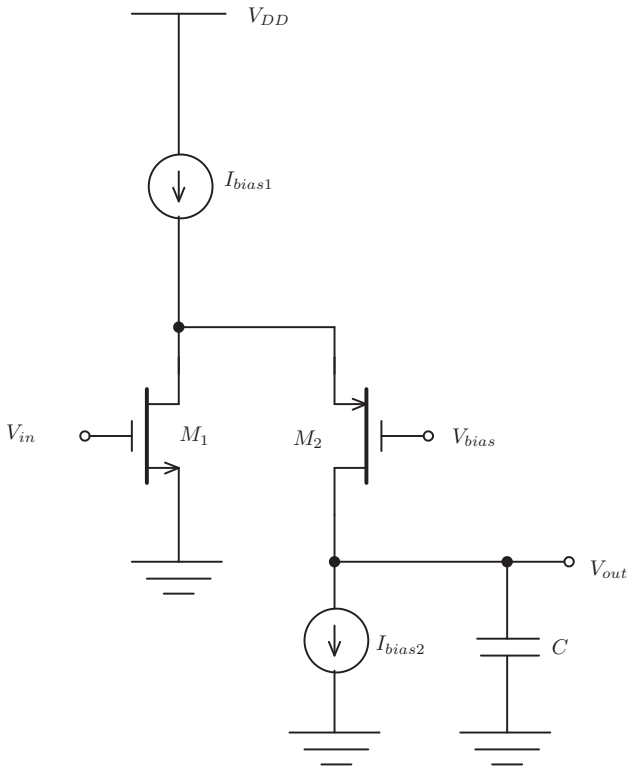

Figure 2: Folded cascode stage.

Exercise 3.

Derive the common-mode range, CMR, and the output range, OR, of the circuit in **Figure 3**. You don't know anything about the relationship between sizes of different transistors. Threshold voltages may be different for all transistors. Anyhow all transistors are saturated. The voltages should be expressed in currents I_{Di}, constants α_i, threshold voltages V_{tni} and V_{tpi}.

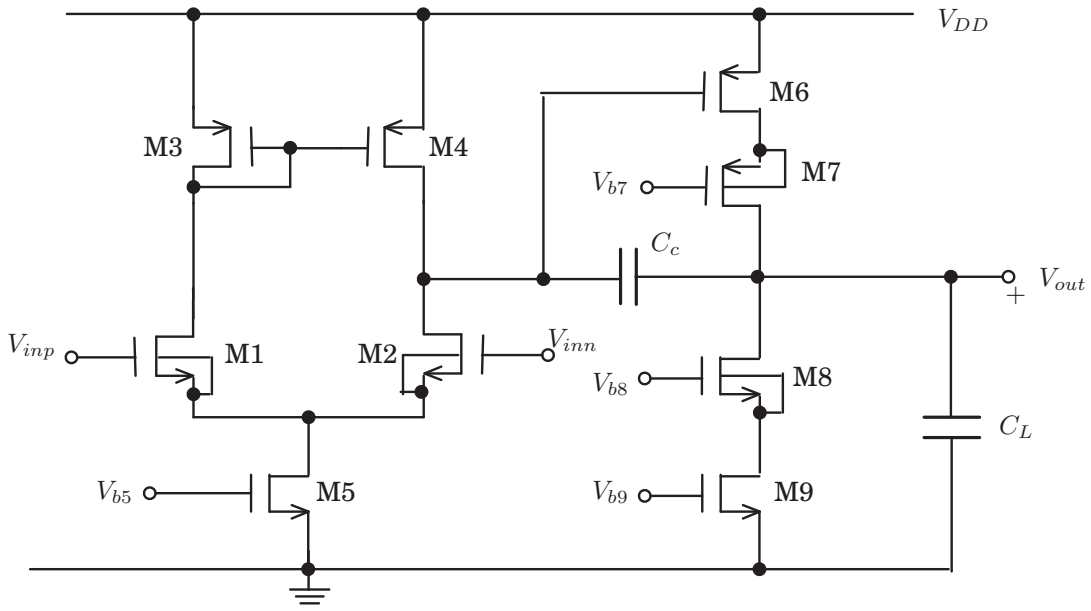

Figure 3: Transistor circuit.

Exercise 4.

Consider the two cascaded common-cource stages in **Figure 4**, where only the thermal noise generated in the transistors is of interest. The current sources are ideal and hence noiseless. Let the output load capacitance be given by C_L and parasitic capacitances are only given by gate-source capacitance, C_{gs2}, for **M2**. Further $I_{bias1} = I_{bias2} = I_{bias}$. The transistors are identical with the small signal parameters $g_{m1} = g_{m2} = g_m$ and $g_{ds1} = g_{ds2} = g_{ds}$. Both transistors operate in the saturation region.

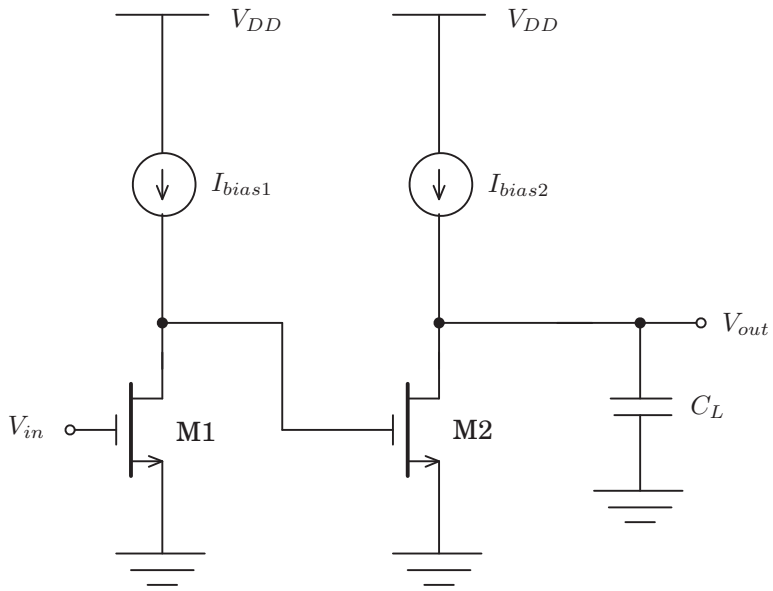

Figure 4: A noisy multi-stage amplifier.

Determine an expression for the spectral density R_{out} of the output thermal noise assuming that the noise from the transistors are uncorrelated.

Exercise 5.

Assume that the TV-signal comes by a 75 ohm wire from the antenna.
Your task here is to design a box that splits the signal into two rooms without giving any reflection. Are there any disadvantages with your construction?

Transistor formulas and noise

1 CMOS transistors

Current and threshold voltage formulas and operating regions for an NMOS transistor

Cut-off:	$V_{GS} < V_t$	$I_D \approx 0$
Linear:	$V_{GS} - V_t > V_{DS} > 0$	$I_D = \alpha(2(V_{GS} - V_t) - V_{DS})V_{DS}$
Saturation:	$0 < V_{GS} - V_t < V_{DS}$	$I_D = \alpha(V_{GS} - V_t)^2(1 + \lambda(V_{DS} - V_{eff}))$
	$V_{DSsat} = V_{eff} = V_{GS} - V_t$	
All regions:	$V_t = V_{t,0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})$	

Small-signal parameters

Linear:	$g_m \approx 2\alpha V_{DS}$	$g_{ds} \approx 2\alpha(V_{GS} - V_t - V_{DS})$
Saturation:	$g_m \approx 2\sqrt{\alpha I_D}$	$g_{ds} \approx \lambda I_D$

Constants: $\alpha = \frac{1}{2}\mu_{0n}C_{ox}\frac{W}{L}$ $\lambda = \sqrt{\frac{K_s\epsilon_0}{2qN_A\phi_0}} \cdot \frac{1}{L}$ $\gamma = \frac{\sqrt{2qN_AK_s\epsilon_0}}{C_{ox}}$

2 Circuit noise

Thermal noise in CMOS transistors
The thermal noise spectral density at the gate of a CMOS transistor is

$$V^2(f) = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Thermal noise in resistors
The thermal noise spectral density of a resistor is modeled as a parallel noise current source

$$I^2(f) = \frac{4kT}{R}$$

Flicker noise in CMOS transistors
The flicker noise spectral density at the gate of a CMOS transistor is

$$V^2(f) = \frac{K}{WLC_{ox}f}$$