TSEI05, Analog and Discrete-time Integrated Circuits, 2010-08-28
Written exam, TEN1

Date and time	2010-08-28, 14.00 - 18.00
Location(s)	TER2 (10 copies printed)
Responsible teacher	J Jacob Wikner, jacwi50, +46-70-5915938
Aid	**Any written and printed material, including books and old exams.** **Note! No pocket calculators, no laptops, no ipods, no telephones, no internet connection.**
Instructions	A maximum of 25 points can be obtained, 10 points are required to pass, 15 for a grade four, and 20 for a grade five. ✗ *Hint! **Be strategic** when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...* Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully! ✗ *Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.* ✗ *Read the tips! They are quite useful, actually!*
Results	Available by 2010-09-11 (hopefully...)

Outline

1. CMOS, PERFORMANCE, ETC. (5 P)

Consider the circuit in the figure below. An input signal is fed to the gate of the NMOS transistor. The DC output voltage, v_{out} - at the drain of the transistor - is fixed by a very, very, very, very large resistor, R_{set}. There is a capacitive load, C_L, between transistor drain and positive supply. The transistor operates in its saturation region. Further on, the input voltage is biased at

$$V_{IN}=V_{dd}/4 . \tag{1.1}$$

Now, assume that this amplifier has a certain slew rate of SR in its bias operating point. Sketch how the following parameters depend on slew rate if the **capacitance, C_L, is fixed**:

1) Transconductance g_m,
2) output conductance g_{ds},
3) DC gain $A_0=g_m/g_{ds}$,
4) dominant pole p_1, and
5) unity-gain frequency ω_u.

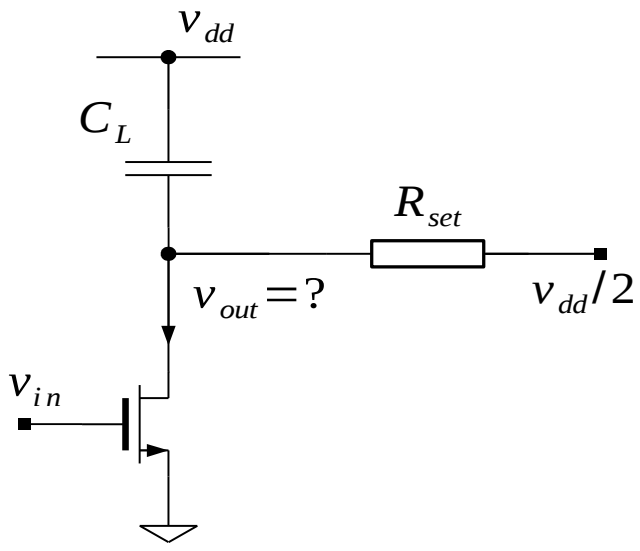

Figure 1.1: Common-something with some kind of load and stuff.

- *This exercise will show that you have understood basic small-signal properties and the relations between them. Make valid assumptions and motivate them well.*
- *Sketch is sketch.*
- *If capacitance is fixed, what does that imply on another important parameter*

(read current) for a given slew rate?

2. GAIN STAGES, SWING, ETC. (5 P)

Consider the circuit in Figure 2.1 which is some kind of circuit. It consists of one PMOS and four NMOS transistors. The input signal is connected to transistor M_0, the output is connected to the drain of M_4 and source of M_3.

1) What is this amplifier type called? Describe the benefits if there are any.

2) Find the minimum and maximum **output voltage levels** as a function of the input DC voltage for which all transistors are operating their saturation region.

Make valid assumptions and motivate them well in your solutions.

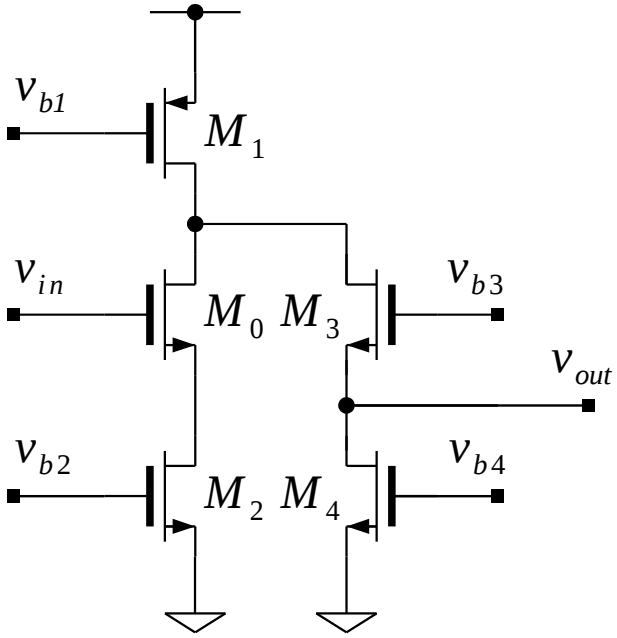

Figure 2.1: Some differential pair of some kind.

- *This exercise will show that you have understood the relation between schematics and small-signal expressions as well as large-signal operation.*
- *Spend some time deriving the small-signal schematics.*
- ***Remember**: You can **always do some suitable assumptions**, as long as you motivate them well!*
- *Don't forget to sanity check your results! Hint: what should the DC gain be for this kind of circuit?*

3. NOISE (5 P)

Consider the circuit in Figure 3.1 which consists of two transistors and some kind of load between them, Z_L:

$$Z_{out} = R_{out} \| C_{out} \tag{3.1}$$

The input voltage, v_{in}, is connected to the two gates and the output voltage, v_{out}, is the voltage across the Z_L.

Both transistors operate in their saturation region. Further assume that all transistors (well, the two of them) are noisy but the resistor, R_{out}, is noise free.

1) Derive the **total output noise power** of the circuit.

2) Also, sketch **how the total output noise power** depends on the resistance, R_{out} **!**

Once again, this is a rather standard exercise for which you will find answers in the books and your notes. Therefore, we **require clear illustrative solutions**.

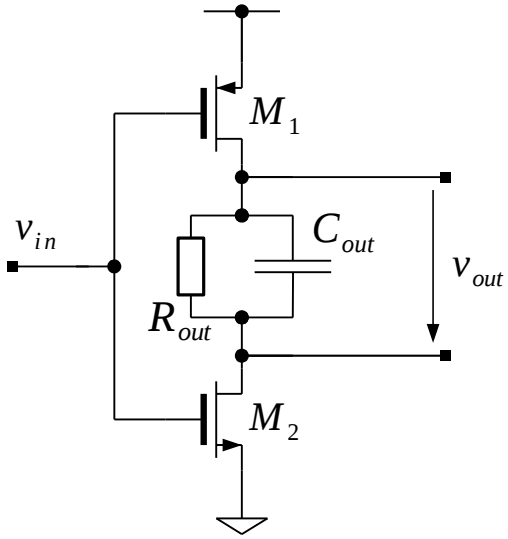

Figure 3.1: Phew! Two transistors...

- *Tip! Use the symmetries to speed up your conclusions.*
- *Don't forget that you have to consider the **total noise power** at the output. Hint: use the noise brickwall bandwidth: $p_1/4$ (see for exampleJohns & Martin).*

4. OP/OTA, FEEDBACK (5 P)

OK, so a question on feedback in amplifiers, etc. Consider the feedback configuration in Figure 4.1. It consists of a CMOS inverter with R_1 and R_2 as feedback components. So a couple of exercises for you:

1) What is the input impedance?

2) What is the output impedance?

3) For which values on C_{out} is the circuit stable?

Do **not** neglect the influence of the limited gain of the transistors.

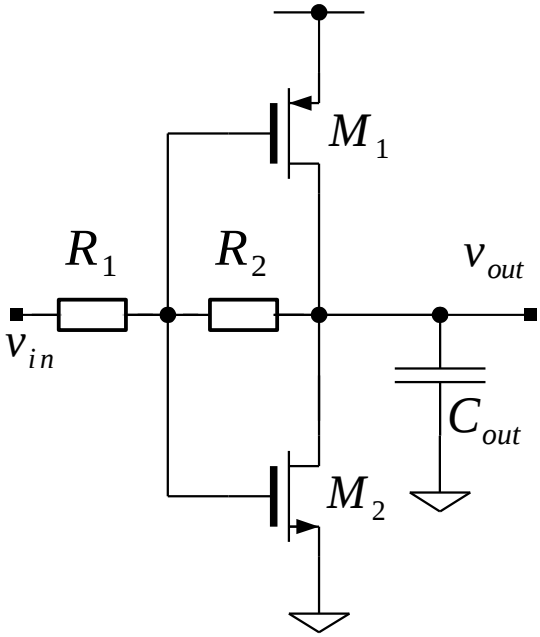

Figure 4.1: Transistors in a closed-loop gain configuration.

- *Once again! Any (reasonable) try to answer the question can give you credits!*
- *And once again! Do not forget to present your results properly!*
- *Use some of the derivations from Exercise 3!*
- *Remember that some of the answers are really simple...*

5. DATA CONVERTERS, ETC. (5 P)

Wow! Same question as in the last exam!!! Yippie! Then it should be easy since you probably have solved it during the Summer while studying for the exam! No, wait a minute ... only one of you asked for the solutions ... hmm. No worries, let's add a twist!

Assume that you have an N-bit D/A converter producing an output current between 0 and (approximately) I_0 A. For a standard, current-steering D/A converter, the analog output current (at a certain multiple of the sampling period) is given by

$$I_{out}(nT)=\left(x_0(nT)+x_1(nT)\cdot 2+x_2(nT)\cdot 2^2+\ldots+x_{N-1}(nT)\cdot 2^{N-1}\right)\cdot\frac{I_0}{2^N} \tag{5.1}$$

where $x_i(nT)$ are the digital control bits. This converter is illustrated by Figure 5.1.

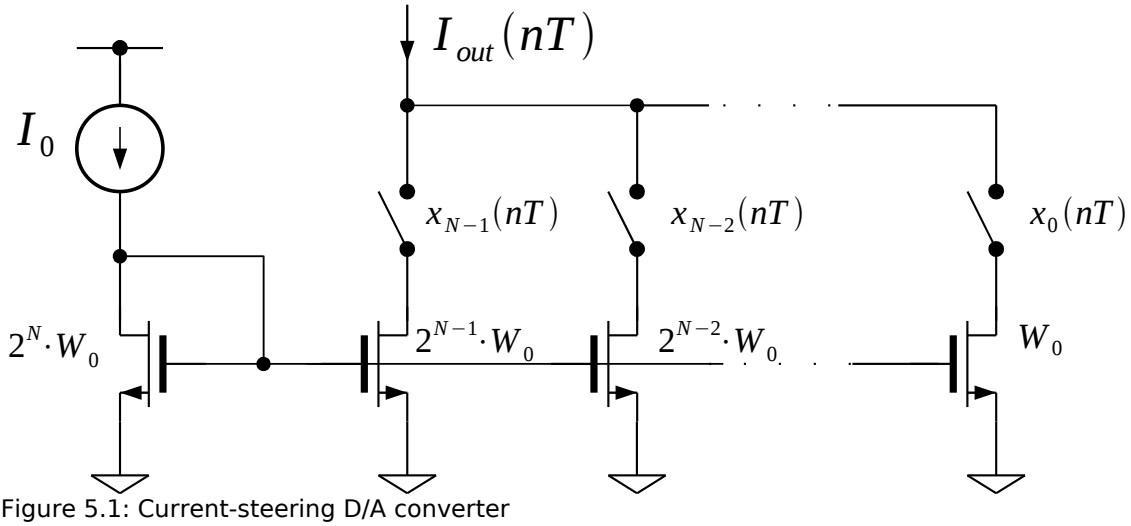

Figure 5.1: Current-steering D/A converter

Derive the **average output noise power** and assume that the output current is given by

$$I_{out}(nT)=\left(X_{DC}+X_{AC}\sin(\omega_0 nT)\right)\cdot\frac{I_0}{2^N} \tag{5.2}$$

where X_{DC} is the DC level of 2^{N-1} and $0<X_{AC}<2^{N-1}$ and assume thermal noise only, where $i_n=4kT\gamma g_m$. **Ignore the noise from the bias transistor.** Express the noise with a minimum of parameters to achieve full points.

Tips: The exercise is not as difficult as it first appears to be! Look at currents

only.

- ✗ *Motivate any assumptions!*
- ✗ *What is the average output current for a sinusoid with amplitude* X_{AC}*? That is, how many current sources are connected to the output in average for that sinusoid?*