101022X6

Q: Implement a static positive edge-triggered D flip-flop using transmission gates and inverters.

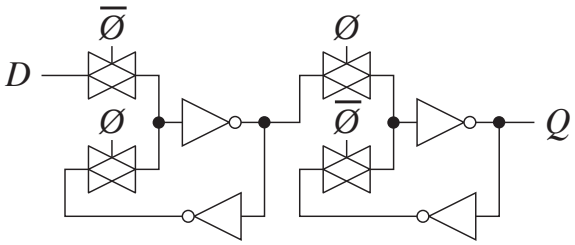
a) Draw the schematic of the flip-flop.

b) Discuss the impact of finite clock rise and fall times on the behavior of the flip-flop.

A: A static latch can be designed by connecting two transmission gates as a multiplexer that uses the clock $\emptyset$ to select the input or a feedback of the output. Gain is needed in the feedback, which can be implemented with two cascaded inverters.

A flip-flop is obtained by connecting a master and a slave latch working on opposite clock phases in series. To make it positive edge-triggered, the clock should be connected such that the master latch goes into its memory state when the clock goes high.

a) A schematic of static positive edge-triggered D flip-flop is drawn below. The output of a latch is taken after one of the inverters in the feedback to obtain some gain between latch input and output.



b) During rise and fall times, all transmission gates in the flip-flop will conduct (weaker than normal). If the rise or fall time are longer than the propagation time of the weakly conducting path, the flip-flop becomes transparent and will fail to store the signal properly.