Lesson 4 & 5

Chapter 6
PROBLEMS

1. [E, None, 4.2] Implement the equation $X = ((\overline{A} + \overline{B})\,(\overline{C} + \overline{D} + \overline{E}) + \overline{F})\,\overline{G}$ using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 2$ and PMOS $W/L = 6$. Which input pattern(s) would give the worst and best equivalent pull-up or pull-down resistance?
2. Implement the following expression in a full static CMOS logic fashion using no more than 10 transistors:

$$\overline{Y} = (A \cdot B) + (A \cdot C \cdot E) + (D \cdot E) + (D \cdot C \cdot B)$$

3. Consider the circuit of Figure 6.1.

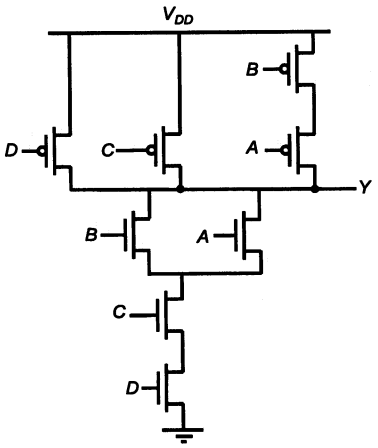


Figure 6.1 CMOS combinational logic gate.

   a. What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS $W/L = 4$ and PMOS $W/L = 8$.
   b. What are the input patterns that give the worst case t_{pHL} and t_{pLH}. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.
   c. Verify part (b) with SPICE. Assume all transistors have minimum gate length (0.25μm).
   d. If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=1, determine the power dissipation in the logic gate. Assume V_{DD}=2.5V, C_{out}=30fF and f_{clk}=250MHz.

4. [M, None, 4.2] CMOS Logic
   a. Do the following two circuits (Figure 6.2) implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.
   b. Will these two circuits' output resistances always be equal to each other?
   c. Will these two circuits' rise and fall times always be equal to each other? Why or why not?

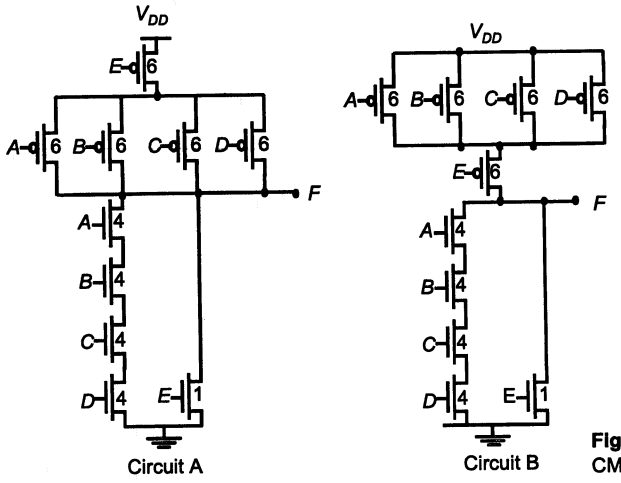


Figure 6.2 Two static CMOS gates.

5. [E, None, 4.2] The transistors in the circuits of the preceding problem have been sized to give an output resistance of 13 kΩ for the worst-case input pattern. This output resistance can vary, however, if other patterns are applied.
   a. What input patterns (*A–E*) give the lowest output resistance when the output is low? What is the value of that resistance?
   b. What input patterns (*A–E*) give the lowest output resistance when the output is high? What is the value of that resistance?
6. [E, None, 4.2] What is the logic function of circuits A and B in Figure 6.3? Which one is a dual network and which one is not? Is the nondual network still a valid static logic gate? Explain. List any advantages of one configuration over the other.

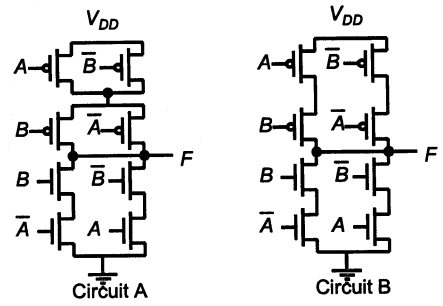


Figure 6.3 Two logic functions.

7. [E, None, 4.2] Compute the following for the pseudo-NMOS inverter shown in Figure 6.4:
   a. V_{OL} and V_{OH}
   b. NM_L and NM_H
   c. The power dissipation: (1) for V_{in} low, and (2) for V_{in} high
   d. For an output load of 1 pF, calculate t_{pLH}, t_{pHL}, and t_p. Are the rising and falling delays equal? Why or why not?
8. [M, SPICE, 4.2] Consider the circuit of Figure 6.5.

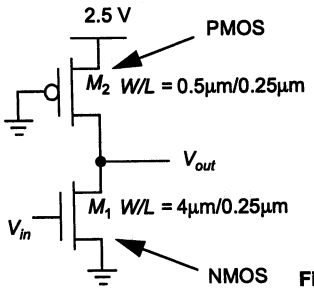


Figure 6.4 Pseudo-NMOS inverter.

a. What is the output voltage if only one input is high? If all four inputs are high?

b. What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0.5? 0.1?

c. Compare your analytically obtained results to a SPICE simulation.

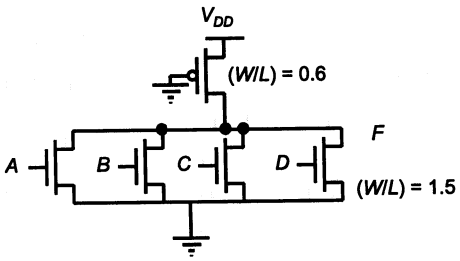


Figure 6.5 Pseudo-NMOS gate.

9. [M, None, 4.2] Implement $F = \overline{ABC} + \overline{A}CD$ (and $\overline{F}$) in DCVSL. Assume A, B, C, D, and their complements are available as inputs. Use the minimum number of transistors.

10. [E, Layout, 4.2] A complex logic gate is shown in Figure 6.6.

a. Write the Boolean equations for outputs F and G. What function does this circuit implement?

b. What logic family does this circuit belong to?

c. Assuming W/L = 0.5u/0.25u for *all nmos* transistors and W/L = 2u/0.25u for the *pmos* transistors, produce a layout of the gate using Magic. Your layout should conform to the following datapath style: (1) Inputs should enter the layout from the left in polysilicon; (2) The outputs should exit the layout at the right in polysilicon (since the outputs would probably be driving transistor gate inputs of the next cell to the right); (3) Power and ground lines should run vertically in metal 1.

d. Extract and netlist the layout. Load both outputs (F,G) with a 30fF capacitance and simulate the circuit. Does the gate function properly? If not, explain why and resize the transistors so that it does. Change the sizes (and areas and perimeters) in the HSPICE netlist.

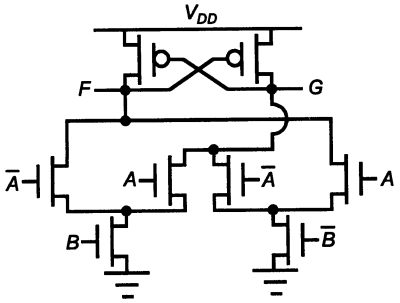


Figure 6.6 Two-input complex logic gate.

11. Design and simulate a circuit that generates an optimal differential signal as shown in Figure 6.7. Make sure the rise and fall times are equal.

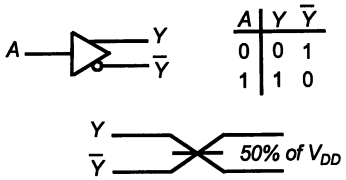


Figure 6.7 Differential Buffer.

12. What is the function of the circuit in Figure 6.8?

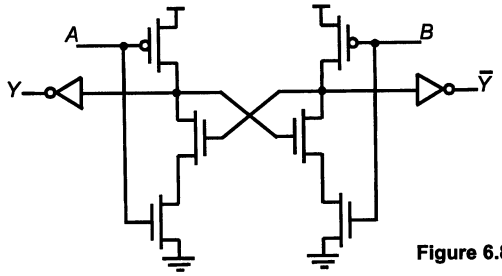


Figure 6.8 Gate.

13. Implement the function $S = ABC + A\overline{BC} + \overline{A}B\overline{C} + \overline{AB}C$, which gives the sum of two inputs with a carry bit, using NMOS pass transistor logic. Design a DCVSL gate which implements the same function. Assume A, B, C, and their complements are available as inputs.
14. Describe the logic function computed by the circuit in Figure 6.9. Note that all transistors (except for the middle inverters) are NMOS. Size and simulate the circuit so that it achieves a

100 ps delay (50-50) using 0.25μm devices, while driving a 100 fF load on both differential outputs. (V_{DD} = 2.5V) Assume A, B and their complements are available as inputs.

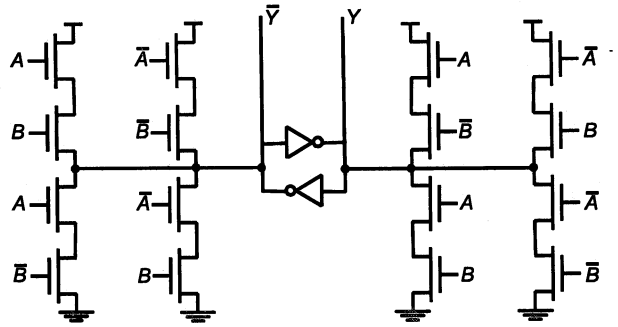


Figure 6.9 Cascoded Logic Styles.

For the drain and source perimeters and areas you can use the following approximations: AS=AD=W*0.625u and PS=PD=W+1.25u.

15. [M, None. 4.2] Figure 6.10 contains a pass-gate logic network.
    a. Determine the truth table for the circuit. What logic function does it implement?
    b. Assuming 0 and 2.5 V inputs, size the PMOS transistor to achieve a V_{OL} = 0.3 V.
    c. If the PMOS were removed, would the circuit still function correctly? Does the PMOS transistor serve any useful purpose?

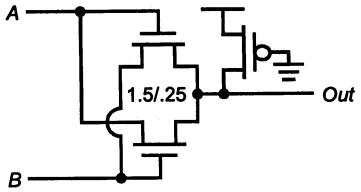


Figure 6.10 Pass-gate network.

16. [M, None, 4.2] This problem considers the effects of process scaling on pass-gate logic.
    a. If a process has a t_{buf} of 0.4 ns, R_{eq} of 8 kΩ, and C of 12 fF, what is the optimal number of stages between buffers in a pass-gate chain?
    b. Suppose that, if the dimension of this process are shrunk by a factor S, R_{eq} scales as $1/S^2$, C scales as $1/S$, and t_{buf} scales as $1/S^2$. What is the expression for the optimal number of buffers as a function of S? What is this value if S = 2?
17. [C, None, 4.2] Consider the circuit of Figure 6.11. Let C_x = 50 fF, M_r has W/L = 0.375/0.375, M_n has W/L_{eff} = 0.375/0.25. Assume the output inverter doesn't switch until its input equals $V_{DD}/2$.
    a. How long will it take M_n to pull down node x from 2.5 V to 1.25 V if In is at 0 V and B is at 2.5V?
    b. How long will it take M_n to pull up node x from 0 V to 1.25 V if V_{In} is 2.5 V and V_B is 2.5 V?
    c. What is the minimum value of V_B necessary to pull down V_x to 1.25 V when V_{In} = 0 V?

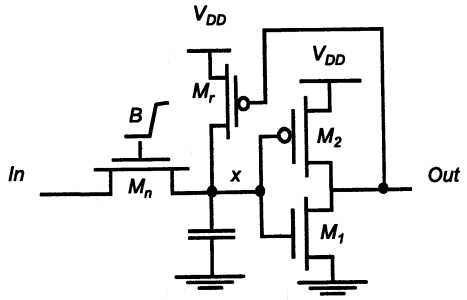
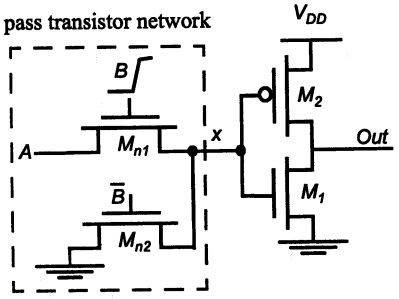


Figure 6.11 Level restorer.

18. Pass Transistor Logic



$V_{DD} = 2.5V$
$(W/L)_2 = 1.5um/0.25um$
$(W/L)_1 = 0.5um/0.25um$
$(W/L)_{ni} = 0.5um/0.25um$

$k_n' = 115uA/V^2$, $kp' = -30uA/V^2$
$V_{tN} = 0.43V$, $V_{tP} = -0.4V$

Figure 6.12 Level restoring circuit.

Consider the circuit of Figure 6.12. Assume the inverter switches ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.

a. What is the logic function performed by this circuit?

b. Explain why this circuit has non-zero static dissipation.

c. Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

d. Implement the same circuit using transmission gates.

e. Replace the pass-transistor network in Figure 6.12 with a pass transistor network that computes the following function: $x = ABC$ at the node x. Assume you have the true and complementary versions of the three inputs A,B and C.

19. [M, None, 4.3] Sketch the waveforms at *x*, *y*, and *z* for the given inputs (Figure 6.13). You may approximate the time scale, but be sure to compute the voltage levels. Assume that $V_T = 0.5$ V when body effect is a factor.

20. [E, None, 4.3] Consider the circuit of Figure 6.14.

a. Give the logic function of *x* and *y* in terms of *A*, *B*, and *C*. Sketch the waveforms at *x* and *y* for the given inputs. Do *x* and *y* evaluate to the values you expected from their logic functions? Explain.

b. Redesign the gates using *np*-CMOS to eliminate any race conditions. Sketch the waveforms at *x* and *y* for your new circuit.

21. [M, None, 4.3] Suppose we wish to implement the two logic functions given by $F = A + B + C$ and $G = A + B + C + D$. Assume both true and complementary signals are available.

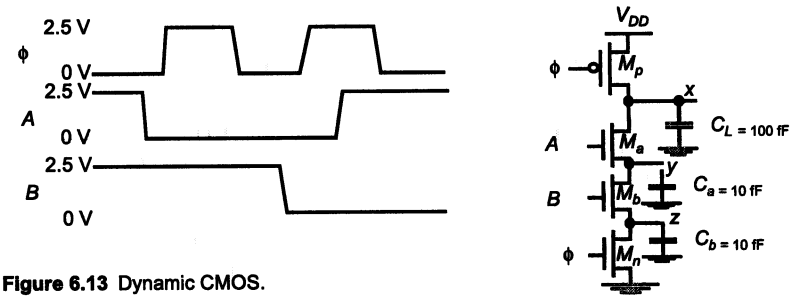


Figure 6.13 Dynamic CMOS.

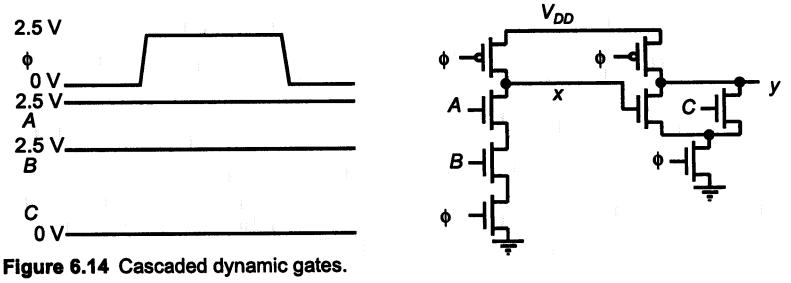


Figure 6.14 Cascaded dynamic gates.

a. Implement these functions in dynamic CMOS as cascaded ϕ stages so as to minimize the total transistor count.

b. Design an *np*-CMOS implementation of the same logic functions. Does this design display any of the difficulties of part (a)?

22. Consider a conventional 4-stage Domino logic circuit as shown in Figure 6.15 in which all precharge and evaluate devices are clocked using a common clock ϕ. For this entire problem, assume that the pulldown network is simply a single NMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge time, evaluate time, and propagation delay of the static inverter are all *T*/2. Assume that the transitions are ideal (zero rise/fall times).

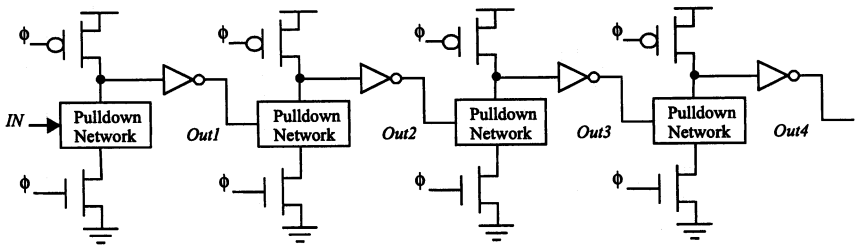


Figure 6.15 Conventional DOMINO Dynamic Logic.

a. Complete the timing diagram for signals Out_1, Out_2, Out_3 and Out_4, when the *IN* signal goes high before the rising edge of the clock ϕ. Assume that the clock period is 10 T time units.

b. Suppose that there are no evaluate switches at the 3 latter stages. Assume that the clock ϕ is initially in the precharge state (ϕ=0 with all nodes settled to the correct precharge states), and the block enters the evaluate period (ϕ=1). Is there a problem during the evaluate period, or is there a benefit? Explain.

c. Assume that the clock ϕ is initially in the evaluate state (ϕ=1), and the block enters the precharge state (ϕ = 0). Is there a problem, or is there any benefit, if the last three evaluate switches are removed? Explain.

23. [C, Spice, 4.3] Figure 6.16 shows a dynamic CMOS circuit in Domino logic. In determining source and drain areas and perimeters, you may use the following approximations: $AD = AS = W \times 0.625\mu m$ and $PD = PS = W + 1.25\mu m$. Assume 0.1 ns rise/fall times for all inputs, including the clock. Furthermore, you may assume that all the inputs and their complements are available, and that all inputs change during the precharge phase of the clock cycle.

a. What Boolean functions are implemented at outputs *F* and *G*? If *A* and *B* are interpreted as two-bit binary words, $A = A_1A_0$ and $B = B_1B_0$, then what interpretation can be applied to output *G*?

b. Which gate (1 or 2) has the highest potential for harmful charge sharing and why? What sequence of inputs (spanning two clock cycles) results in the worst-case charge-sharing scenario? Using SPICE, determine the extent to which charge sharing affects the circuit for this worst case..

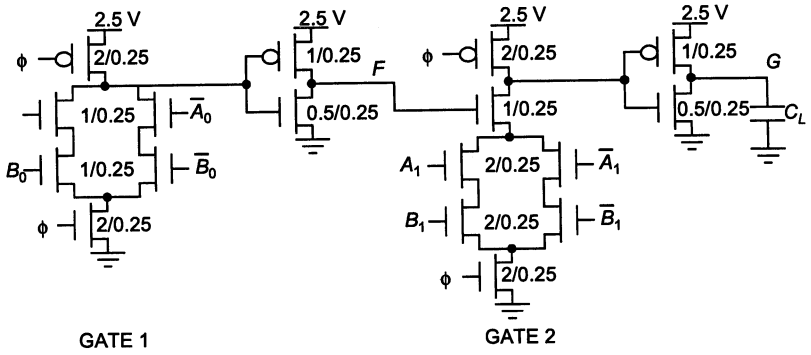


Figure 6.16 DOMINO logic circuit.

24. [M, Spice, 4.3] In this problem you will consider methods for eliminating charge sharing in the circuit of Figure 6.16. You will then determine the performance of the resulting circuit.

a. In problem 24 you determined which gate (1 or 2) suffers the most from charge sharing. Add a single 2/0.25 PMOS precharge transistor (with its gate driven by the clock ϕ and its source connected to V_{DD}) to one of the nodes in that gate to maximally reduce the charge-sharing effect. What effect (if any) will this addition have on the gate delay? Use SPICE to demonstrate that the additional transistor has eliminated charge sharing for the previously determined worst-case sequence of inputs.

b. For the new circuit (including additional precharge transistor), find the sequence of inputs (spanning two clock cycles) that results in the worst-case delay through the circuit.

Remember that precharging is another factor that limits the maximum clocking frequency of the circuit, so your input sequence should address the worst-case precharging delay.

c. Using SPICE on the new circuit and applying the sequence of inputs found in part (b), find the maximum clock frequency for correct operation of the circuit. Remember that the precharge cycle must be long enough to allow all precharged nodes to reach ~90% of their final values before evaluation begins. Also, recall that the inputs (A, B and their complements) should not begin changing until the clock signal has reached 0 V (precharge phase), and they should reach their final values before the circuit enters the evaluation phase.

25. [C, None, 4.2–3] For this problem, refer to the layout of Figure 6.17.

a. Draw the schematic corresponding to the layout. Include transistor sizes.

b. What logic function does the circuit implement? To which logic family does the circuit belong?

c. Does the circuit have any advantages over fully complementary CMOS?

d. Calculate the worst-case V_{OL} and V_{OH}.

e. Write the expresions for the area and perimeter of the drain and source for all of the FETs in terms of λ. Assume that the capacitance of shared diffuusions divides evenly between the sharing devices. Copy the layout into Magic, extract and simulate to find the worst-case t_{pHL} time. For what input transition(s) does this occur? Name all of the parasitic capacitances that you would need to know to calculate this delay by hand (you do not need to perform the calculation).

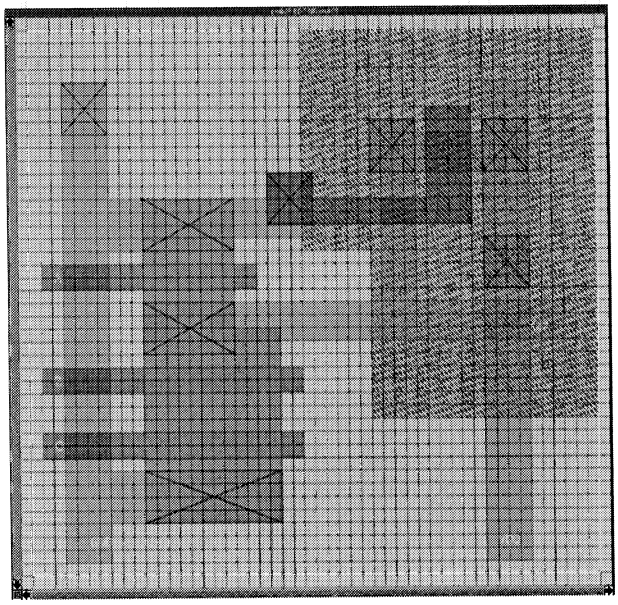


Figure 6.17 Layout of complex gate.

26. [E, None, 4.4] Derive the truth table, state transition graph, and output transition probabilities for a three-input XOR gate with independent, identically distributed, uniform white-noise inputs.

27. [C, None, 4.4] Figure 6.18 shows a two-input multiplexer. For this problem, assume independent, identically-distributed uniform white noise inputs.

a. Does this schematic contain reconvergent fan-out? Explain your answer.

b. Find the exact signal (P_1) and transition ($P_{0\rightarrow 1}$) formulas for nodes *X*, *Y*, and *Z* for: (1) a static, fully complementary CMOS implementation, and (2) a dynamic CMOS implementation.

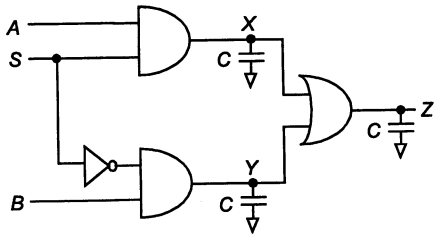


Figure 6.18 Two-input multiplexer

28. [M, None, 4.4] Compute the switching power consumed by the multiplexer of Figure 6.18, assuming that all significant capacitances have been lumped into the three capacitors shown in the figure, where $C = 0.3$ pF. Assume that $V_{DD} = 2.5$ V and independent, identically-distributed uniform white noise inputs, with events occuring at a frequency of 100 MHz. Perform this calculation for the following:

a. A static, fully-complementary CMOS implementation

b. A dynamic CMOS implementation

29. Consider the circuit shown Figure 6.19.

a. What is the logic function implemented by this circuit? Assume that all devices (M1-M6) are 0.5μm/0.25μm.

b. Let the drain current for each device (NMOS and PMOS) be 1μA for NMOS at $V_{GS} = V_T$ and PMOS at $V_{SG} = V_T$. What input vectors cause the worst case leakage power for each output value? Explain (state all the vectors, but do not evaluate the leakage). Ignore DIBL.

c. Suppose the circuit is active for a fraction of time *d* and idle for *(1-d)*. When the circuit is active, the inputs arrive at 100 MHz and are uniformly distributed ($Pr_{(A=1)} = 0.5$, $Pr_{(B=1)} = 0.5$, $Pr_{(C=1)} = 0.5$) and independent. When the circuit is in the idle mode, the inputs are fixed to one you chose in part (b). What is the duty cycle *d* for which the active power is equal to the leakage power?

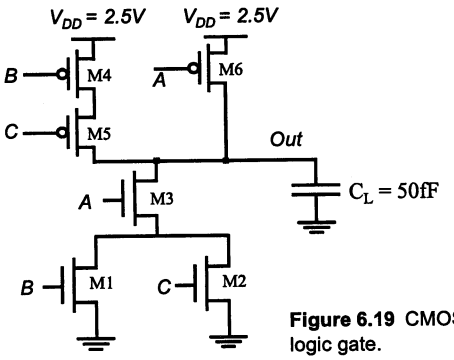


Figure 6.19 CMOS logic gate.

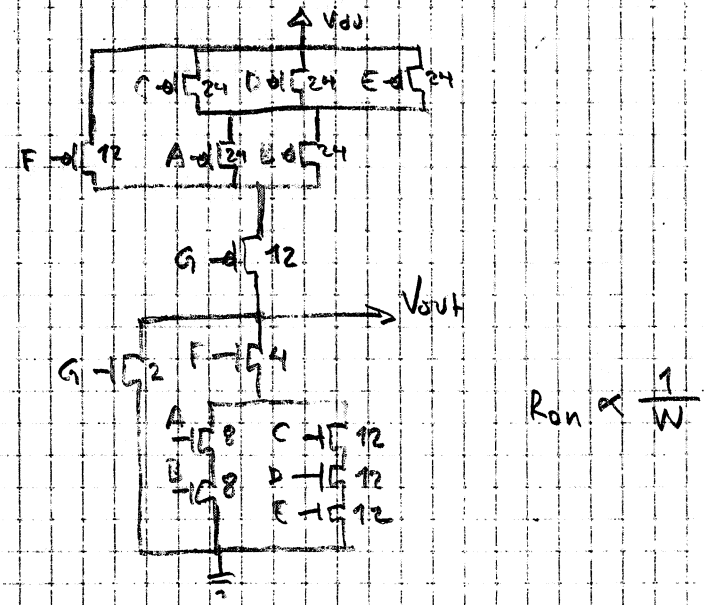
6.1 Implement the equation $X = \left[(\bar{A}+\bar{B})(\bar{C}+\bar{D}+\bar{E})+\bar{F}\right]\bar{G}$ using complementary CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 2 and PMOS W/L = 6. Which input pattern(s) would give the worst and best pull-up or pull-down resistance?

$$PUN = S_p = F(\bar{A},\bar{B},\ldots) = \left[(A+B)(C+D+E)+F\right]G$$

$$PDN = S_n = \overline{F(A,B\ldots)} = \left[(\bar{A}+\bar{B})(\bar{C}+\bar{D}+\bar{E})+\bar{F}\right]\bar{G}$$

$$= G + \left[(\bar{A}+\bar{B})(\bar{C}+\bar{D}+\bar{E})+\bar{F}\right] = G + F\left[\overline{(\bar{A}+\bar{B})(\bar{C}+\bar{D}+\bar{E})}\right]$$

$$= G + F\left[AB + CDE\right]$$



$R_{on} \propto \frac{1}{W}$

$$\frac{1}{W_{p,eq}} = \frac{1}{W_{p,G}} + \frac{1}{W_{p,F}} \qquad \text{set } W_{p,F} = W_{p,G} \text{ and } W_{p,eq} = 6$$

$$\frac{1}{6} = \frac{2}{W_{p,G}}$$

$$W_{p,G} = 12 = W_{p,F}$$

Also set

$$\frac{1}{W_{p,F}} = \frac{1}{W_{p,A}} + \frac{1}{W_{p,C}} \qquad \text{set } W_{p,A} = W_{p,C}$$

$$\frac{1}{12} = \frac{2}{W_{p,A}}$$

$$W_{p,A} = 24 = W_{p,C}$$

Also set $W_{p,C} = W_{p,B} = W_{p,E} = 24$

$W_{p,A} = W_{p,B} = 24$

Use the same idea for PDN

6.1 continued...

Worst Pull-Up resistance : ABCDEFG = 1111100, 0101110, etc
(only <u>one</u> path to Vdd)

Best Pull-Up resistance : ABCDEFG = 0000000

Worst Pull-Down resistance : ABCDEFG = 0000001, etc
(only <u>one</u> path to gnd)

Best Pull-Down resistance : ABCDEFG = 1111111

(6.2) Implement the following expression in a full static CMOS logic fashion using no more than 10 transistors. (The output should be $\bar{Y}$)

$$\bar{Y} = AB + ACE + DE + DCB = A(B+CE) + D(E+CB)$$

PDN = $S_n = \bar{Y} = A(B+CE) + D(E+CB)$

PUN = $S_p = Y(\bar{A}, \bar{B}, \bar{C}, \bar{D}, \bar{E})$

$$Y = \overline{A(B+CE) + D(E+CB)} = \overline{A(B+CE)} \cdot \overline{D(E+CB)} =$$

$$= \left[\bar{A} + (\bar{B}+\bar{C}\bar{E})\right]\left[\bar{D} + (\bar{E}+\bar{C}\bar{B})\right] = \left[\bar{A} + \bar{B}\,\overline{CE}\right]\left[\bar{D} + \bar{E}\,\overline{CB}\right] =$$

$$= \left[\bar{A} + \bar{B}(\bar{C}+\bar{E})\right]\left\{\bar{D} + \bar{E}(\bar{C}+\bar{B})\right\} =$$

$$= \bar{A}\bar{D} + \bar{A}\bar{E}(\bar{C}+\bar{B}) + \bar{B}\bar{D}(\bar{C}+\bar{E}) + \bar{B}\bar{E}(\bar{C}+\bar{E})(\bar{C}+\bar{B}) =$$

$$= \bar{A}\bar{D} + \bar{A}\bar{E}(\bar{C}+\bar{B}) + (\bar{C}+\bar{E})\underbrace{\left[\bar{B}\bar{D} + \bar{B}\bar{E}(\bar{C}+\bar{B})\right]}_{X_1}$$

$$X_1 = \bar{B}\bar{D} + \bar{B}\bar{C}\bar{E} + \bar{B}\bar{E} = \bar{B}\bar{D} + \bar{B}\bar{E}(\bar{C}+1) = \bar{B}(\bar{D}+\bar{E})$$

$$\Rightarrow Y = \bar{A}\bar{D} + \bar{A}\bar{E}(\bar{C}+\bar{B}) + \bar{B}\underbrace{(\bar{C}+\bar{E})(\bar{D}+\bar{E})}_{X_2}$$

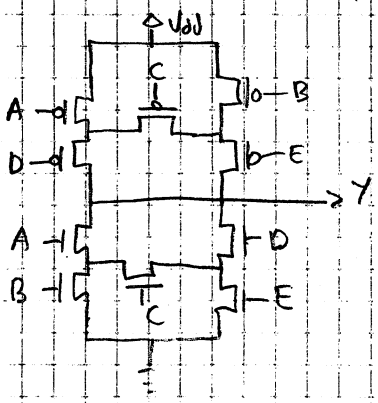
$$X_2 = \bar{C}\bar{D} + \bar{C}\bar{E} + \bar{D}\bar{E} + \bar{E} = \bar{C}\bar{D} + \bar{C}\bar{E} + \bar{E}(\bar{D}+1) = \bar{C}\bar{D} + \bar{C}\bar{E} + \bar{E} =$$

$$= \bar{C}\bar{D} + \bar{E}(\bar{C}+1) = \bar{C}\bar{D} + \bar{E}$$

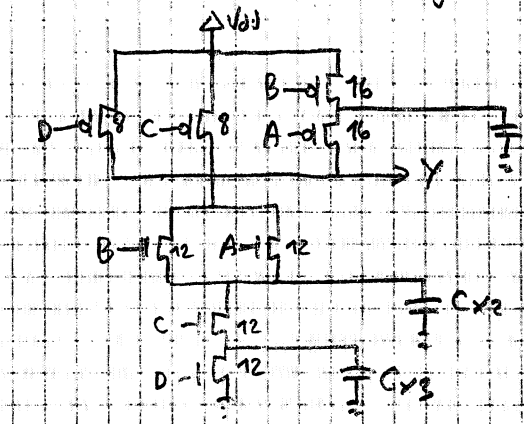
$$\Rightarrow Y = \bar{A}\bar{D} + \bar{A}\bar{E}(\bar{C}+\bar{B}) + \bar{B}(\bar{C}\bar{D}+\bar{E}) = \bar{A}\bar{D} + \bar{A}\bar{E}\bar{C} + \bar{A}\bar{E}\bar{B} + \bar{B}\bar{C}\bar{D} + \bar{B}\bar{E} =$$

$$= \bar{A}\bar{D} + \bar{A}\bar{E}\bar{C} + \bar{B}\bar{E}(\bar{A}+1) + \bar{B}\bar{C}\bar{D} = \bar{A}\bar{D} + \bar{A}\bar{E}\bar{C} + \bar{B}\bar{E} + \bar{B}\bar{C}\bar{D}$$

$$\Rightarrow \text{PUN} = Y(\bar{A}, \bar{B}, \bar{C}, \bar{D}, \bar{E}) = AD + ACE + BE + BCD = A(D+CE) + B(E+CD)$$



(6.3) Consider the circuit of figure 6.1



a) What is the logic function implemented by the cmos transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 4 and PMOS W/L = 8

$PDN = S_n = (A+B)CD = \overline{Y}$

$Y = \overline{CD(A+B)} = \overline{CD} + \overline{(A+B)} = \overline{C} + \overline{D} + \overline{A}\,\overline{B}$

The on-resistance of a transistor is proportional to $1/W$

In worst case, only one path in each network is conducting.

$\frac{1}{W_{n,eq}} = \frac{1}{W_{n,B}} + \frac{1}{W_{n,C}} + \frac{1}{W_{n,D}}$; set $W_{n,eq} = 4$ and $W_{n,B} = W_{n,C} = W_{n,D}$

$\frac{1}{4} = \frac{3}{W_{n,B}} \Leftrightarrow W_{n,B} = \underline{12} = W_{n,C} = W_{n,D} = W_{n,A}$

The path including the NMOS-A transistor is equivalent to the path containing the B-transistor

$\frac{1}{W_{p,eq}} = \frac{1}{W_{p,A}} + \frac{1}{W_{p,B}}$; set $W_{p,eq} = 8$ and $W_{p,A} = W_{p,B}$

$\frac{1}{8} = \frac{2}{W_{p,A}} \Leftrightarrow W_{p,A} = \underline{16} = W_{p,B}$

Trivial that $W_{p,D} = W_{p,C} = 8$

b) What are the input patterns that give the worst case t_{PHL} and t_{PLH}? State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effects of capacitances at the internal nodes.

6.3

continued…

b) The worst case t_{pHL} occurs when the internal node capaitances C_{x2}, C_{x3} are charged before the H→L transition. The initial states that can cause this are:

ABCD = {1010,1110,0110}

The final state is one of:

ABCD = {1011, 0111}

Note that the case of 0110→0111 is slightly worse than the other cases due to the impact of capacitance C_{x1}. However, considering the intermediate nodes, the capacitance in the nodes that belongs to the main path of the charging (or discharging) current are the most critical.

The worst case t_{pLH} happens when C_{x1} is discharged before the L→H transition. The input pattern that can cause this is:

ABCD = 0111 → 0011

c) If $P_{A=1}$=0.5, $P_{B=1}$=0.2, $P_{C=1}$=0.3 and $P_{D=1}$=1, determine the power dissipation in the logic gate. Assume V_{dd} = 2.5V, C_{out} = 30fF and f_{clk} = 250MHz.

Since D is always 1, the circuit implements the following function

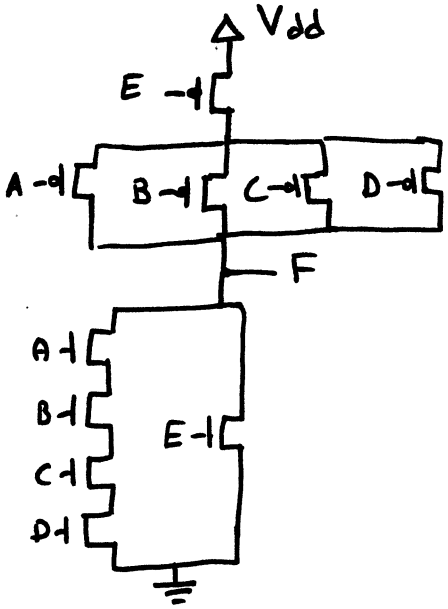
$Y = \overline{(A+B)C}$

$P_{(A+B)=1} = 1 - (P_{A=0} * P_{B=0}) = 1 – (0.5*(1-0.2)) = 0.6$
$P_{(A+B)=0} = 1 – 0.6 = 0.4$
$P_{Y=0} = P_{(A+B)=1} * P_{C=1} = 0.6*0.3=0.18$
$P_{Y=1} = 1 – 0.18 = 0.82$
$P_{Y:0→1} = 0.18*0.82 = 0.1476 = \alpha$

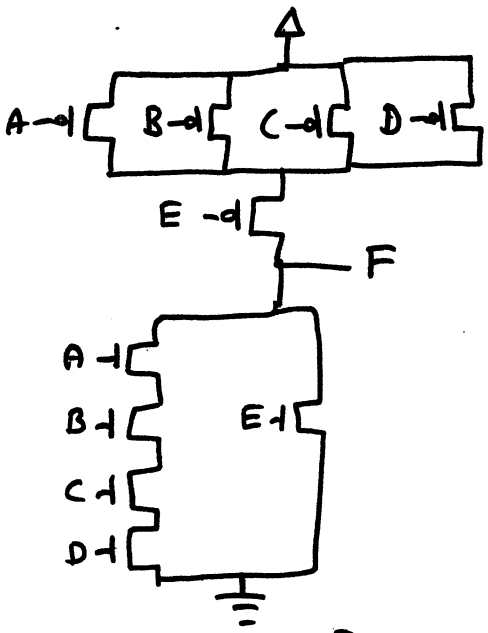
$$P_{dyn} = \alpha f_{clk} C_{out} V_{dd}^{\ 2} = 0.1476 \cdot 250 \cdot 10^{6} \cdot 30 \cdot 10^{-15} \cdot 2.5^{2} = 6.92 \mu W$$

6.4 CMOS Logic

a) Do the following two circuits (figure 6.2) implement the same logic function? If yes, what is the logic function? If no, give the boolean expressions for both circuits



Circuit A



Circuit B

Yes the PDN:s are equal and thus implement the same logic function

$F = ABCD + E$, $\overline{F} = \overline{ABCD + E}$

b) Will these two circuits' output resistances always be equal to each other?

No! In circuit A, four devices suffer from body effects compared to only one in circuit B

c) Will these two circuits' rise and fall times always be equal to each other? Why or why not?

6.4
continued

The deciding factor on the rise and fall times will be the parasitic capacitances of the pn-junctions. Looking at the PUN which is the only difference between the circuits we see 9 pn-junctions (from drain and source of the transistors) in active nodes in circuit A (2 from each A,B,C,D and 1 from E). Circuit B has 6 pn-junctions (1 from each A,B,C,D and 2 from E) and hence circuit B will be faster than circuit A.

6.5

The transistors in the circuits of the preceding problem have been sized to give an output resistance of 13kΩ for the worst-case input pattern. The output resistance can vary however, if other patterns are applied.

a) What input patterns (A-E) give the lowest output resistance when the output is low? What is the

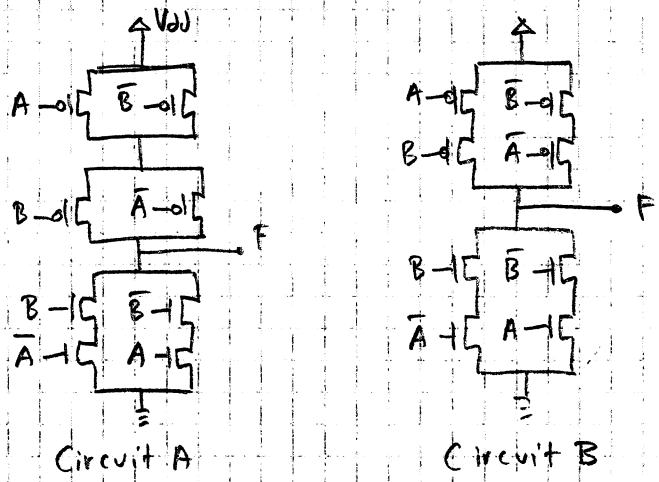
The lowest output resistance is obtained when all inputs are equal to 1. In that case, the output resistance is the parallel of the resistance of a NMOS of width 1, with a series of four equal NMOS of width 4. Both combinations have the same resistance, equal to the worst-case output resistance, 13kΩ. Then the output resistance, in this case, is half this value → 6,5kΩ

b) What input patterns (A-E) give the lowest output resistance when the output is high? What is the value of that resistance?

The lowest output resistance is obtained when all inputs are equal to zero. Each of the PMOS have the same width, so all of them have the same resistance. The worst case resistance occurs when only one of the inputs (A,B,C,D) is equal to 0 while all the rest are equal to 1. The output resistance in that case is the series of the resistance of two of the PMOS and is equal to 13kΩ. Then, each of the PMOS has an output resistance equal to 6,5kΩ. The output resistance is equal to the series of one of these resistances with the parallel of four of the same resistances. Then the minimum output resistance is

6,5kΩ + 6,5kΩ/4 = 8,125kΩ

6.6 What is the logic function of circuits A and B in figure 6.3? Which one is a dual network and which one is not? Is the non-dual network still a valid static logic gate? Explain. List any advantages of one configuration over the other.



CIRCUIT A & B :

$$\bar{F} = \bar{A}B + A\bar{B} = A \oplus B = A\ (EXOR)\ B$$

$$F = \overline{A\ (EXOR)\ B}$$

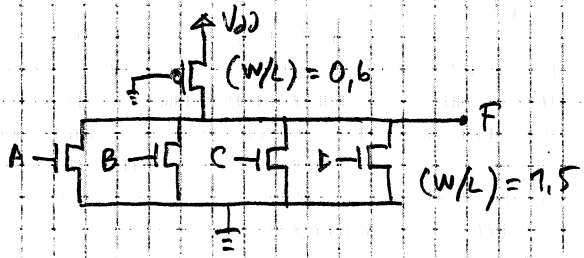
Circuit A is a dual network because the pull-up network is dual (series ↔ parallel) with the pull-down network. However, circuit B is still a valid static logic gate, since for any combination of the inputs, there is either a low resistance path from VDD or ground to the output. Circuit B has an extra advantage. The internal node capacitances are less compared to circuit A, which makes it faster than circuit A.

DUAL NETWORK :

PUN	PDN
Parallel	serial
Serial	parallel

6.8

Consider the circuit of figure 6.5



a) What is the output voltage if only one input is high? If all four inputs are high?

$$I_d = k'\left(\frac{W}{L}\right)\left[(V_{gs}-V_T)V_{min} - \frac{V_{min}^2}{2}\right](1+\lambda V_{ds})$$

$$V_{min} = \min\{V_{gs}-V_T\ ;\ V_{dsat}\ ;\ V_{ds}\}$$

Consider a case when only one input is high. Assume that V_{out} is small enough that $V_{min} = V_{dsat}$ for the PMOS device, and $V_{min} = V_{ds} = V_{out}$ for the NMOS devices. Solve for V_{out}:

$$|I_{dp}| = |I_{dn}|$$

$$k_p'\left(\frac{W}{L}\right)_p\left[(V_{DD}-|V_{TP}|)V_{dsat} - \frac{V_{dsat}^2}{2}\right](1+\lambda(V_{DD}-V_{out})) =$$

$$k_n'\left(\frac{W}{L}\right)_n\left[(V_{DD}-V_{Tn})V_{out} - \frac{V_{out}^2}{2}\right](1+\lambda V_{out})$$

$$30\cdot10^{-6}\cdot0,6\left[(2,5-0,4)\cdot1 - \frac{1^2}{2}\right](1+0,1(2,5-V_{out})) =$$

$$115\cdot10^{-6}\cdot7,5\left[(2,5-0,43)V_{out} - \frac{V_{out}^2}{2}\right](1+0,06\,V_{out})$$

Graphical solution on HP48:

$V_{out} \approx 102\,mV$; Assumption for V_{min} is ok

$\hookrightarrow I_d = 35,7\,\mu A$

When all inputs are high

$$|I_{dp}| = 4|I_{dn}|$$

Graphical solution on HP48:

25,869999

$V_{out} = 25,3\,mV$; Assumptions for V_{min} are still ok.

$\hookrightarrow I_d = 35,9\,\mu A$

(6.8) b) continued...

What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0,5 ? 0,1 ?

Notice in part a) that the drain current in the PMOS is 35,7 μA with one NMOS on and 35,9 μA with four NMOS devices on. The current in the PMOS can be approximated as 35,8 μA when any number of NMOS devices are on and 0 μA when all four are off. The probability that all four devices are off is $(1-s)^4$, where s is the probability an input is high. Therefore:

$P_{avg} = P_{off}(1-s)^4 + P_{on}\left[1-(1-s)^4\right]$ where

$P_{off} = 0W$ and $P_{on} = 35,8 \cdot 10^{-6} \cdot 2,5 = 89,5\,\mu W$

(i) $P_{avg} = 0(1-0,1)^4 + 89,5\left[1-(1-0,1)^4\right]\mu W = 30,8\,\mu W$ when $s=0,1$

(ii) $P_{avg} = 0(1-0,5)^4 + 89,5\left[1-(1-0,5)^4\right]\mu W = 83,9\,\mu W$ when $s=0,5$

(6.9) Implement $F = A\bar{B}\bar{C} + \bar{A}CD$ (and $\bar{F}$) in DCVSL

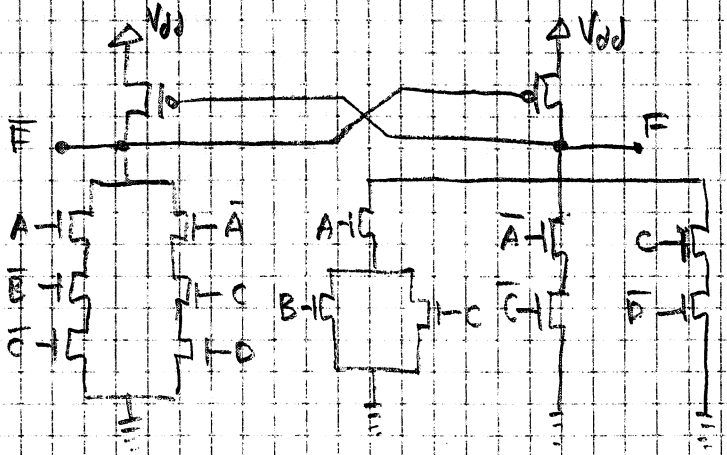
Assume A, B, C, D and their complements are available as inputs.

Use minimum number of transistors.

$S_n = \bar{F}$; Find $\bar{F}$ through a Karnaugh diagram.

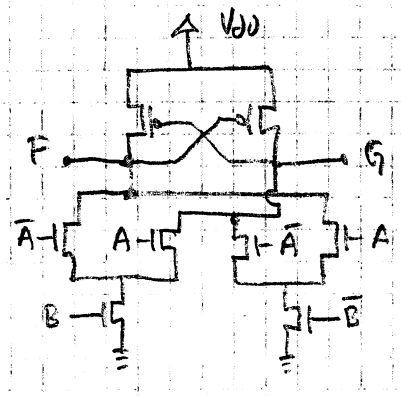
AB \ CD	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	0	0	0
10	1	1	0	0

$\bar{F} = \bar{A}\bar{C} + A\bar{B} + A\bar{C} + C\bar{D} = A(\bar{B}+\bar{C}) + \bar{A}\bar{C} + C\bar{D}$



DCVSL implementation

(6.10) A complex logic gate shown in Figure 6.6



a) Write the Boolean equations for outputs F and G. What function does the circuit implement?

$\bar{F} = \bar{A}B + A\bar{B}$; $F = \overline{\bar{A}B + A\bar{B}} = (\overline{\bar{A}B})(\overline{A\bar{B}}) = (A+\bar{B})(\bar{A}+B) =$

$= A\bar{A} + AB + \bar{A}\bar{B} + B\bar{B} = AB + \bar{A}\bar{B}$ (NXOR)

$\bar{G} = AB + \bar{A}\bar{B}$; $G = \overline{AB + \bar{A}\bar{B}} = (\overline{AB})(\overline{\bar{A}\bar{B}}) = (\bar{A}+\bar{B})(A+B) =$

$= \bar{A}A + \bar{A}B + A\bar{B} + B\bar{B} = \bar{A}B + A\bar{B}$ (XOR)

b) What logic family does this circuit belong to?

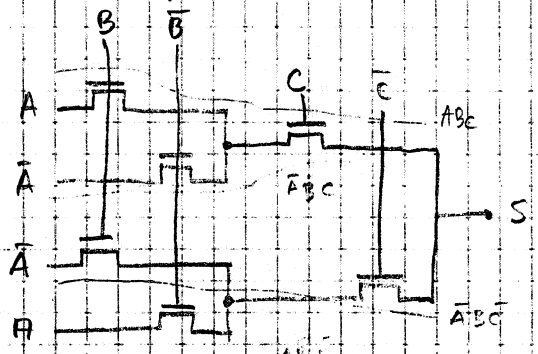
DCVSL (Differential Cascode Voltage Switch Logic)

6.13

Implement the function

$S = ABC + A\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}\bar{C}$

which gives the sum of two inputs with a carry bit, using NMOS pass transistor logic. Design a DCVSL gate which implements the same function. Assume A, B, C and their complements



$$\bar{S} = \overline{ABC + A\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}\bar{C}} =$$

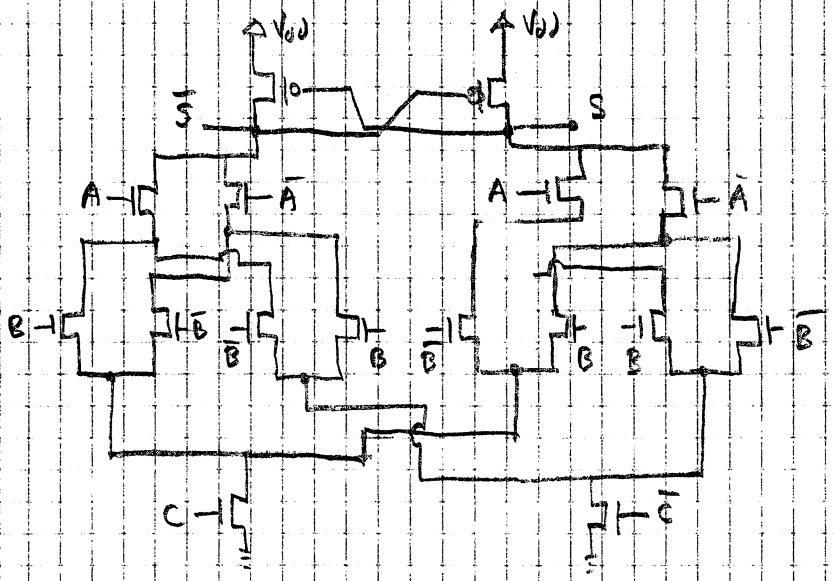
$$= \overline{(ABC)}\,\overline{(A\bar{B}\bar{C})}\,\overline{(\bar{A}BC)}\,\overline{(\bar{A}\bar{B}\bar{C})} = (\bar{A}+\bar{B}+\bar{C})(\bar{A}+B+C)(A+\bar{B}+C)(A+B+\bar{C})$$

$$= (\bar{A}+\bar{A}B+\bar{A}C+\bar{A}\bar{B}+B\bar{B}+\bar{B}C+\bar{A}\bar{C}+B\bar{C}+C\bar{C}) \cdot$$

$$\cdot (A+A\bar{B}+AC+AB+B\bar{B}+BC+A\bar{C}+\bar{B}\bar{C}+C\bar{C}) =$$

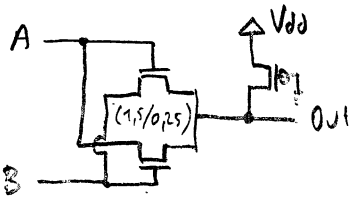
$$= \bar{A}BC + \bar{A}B\bar{C} + \bar{A}BC + \bar{A}BC + \bar{A}\bar{B}\bar{C} + ABC + A\bar{B}\bar{C} + AB\bar{C} + ABC =$$

$$= \bar{A}BC + \bar{A}B\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$$



(6.15) Figure 6.10 shows a pass-gate logic network.

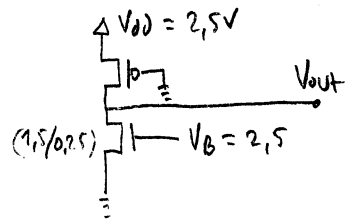
a) Determine the truth table for the circuit. What logic function does it implement?



A B	Out
0 0	1
0 1	0
1 0	0
1 1	1

The circuit implements the XNOR function

b) Assuming 0 and 2,5 V inputs, size the PMOS transistor to achieve a $V_{OL} = 0,3\,V$



For the PMOS we have:

$V_{min,p} = \min\{V_{sd,i} - V_T;\ V_{sd};\ |V_{dsat}|\} = \min\{(2,5-0,4);(0,3-0);1\}$

$\Rightarrow$ so the PMOS is VELOCITY SATURATED

For the NMOS we have:

$V_{min,n} = \min\{V_{gs} - V_T;\ V_{ds};\ V_{dsat}\} = \min\{2,5-0,43;\ 0,3;\ 0,63\} = 0,3$

so the NMOS in the LINEAR REGION

$I_{dp} = I_{dn}$

$$k_p'\left(\frac{W}{L}\right)_p\left[V_{gt,p}V_{min,p} - \frac{V_{min,p}^2}{2}\right](1+\lambda V_{sd,p}) = k_n'\left(\frac{W}{L}\right)_n\left[V_{gt}V_{min,n} - \frac{V_{min,n}^2}{2}\right](1+\lambda V_{ds,n})$$

$$30\cdot 10^{-6}\left(\frac{W}{L}\right)_p\left[(2,5-0,4)\cdot 1 - \frac{1^2}{2}\right](1+0,1(2,5-0,3)) = 115\cdot 10^{-6}\left(\frac{1,5}{0,25}\right)\left[(2,5-0,43)0,3 - \frac{0,3^2}{2}\right](1+0,06\cdot 0,3)$$

$$\left(\frac{W}{L}\right)_p = 6,91$$

$$\left(\frac{W}{L}\right)_p = \frac{1,73}{0,25}$$

(6.15) c) If the PMOS was removed, would the circuit still function
continued correctly? Does the PMOS transistor serve any useful purpose?

No, the circuit would fail if the PMOS was removed. The output node would then remain low when AB=00 since it would be floating. The PMOS device pulls the output node high when it would otherwise be in a high impedance state.

(6.16) This problem considers the effects of process scaling on pass-gate logic.

a) If a process has a t_{buf} of 0,4ns, R_{eq} of 8kΩ and C of 12fF, what is the optimal number of stages between buffers in a pass-gate chain?

(See textbook pp. 281-284)

The optimal number of switches (m_{opt}) between buffers is given by:

$$m_{opt} = 1{,}7\sqrt{\frac{t_{buf}}{CR_{eq}}} \quad (6.39)$$

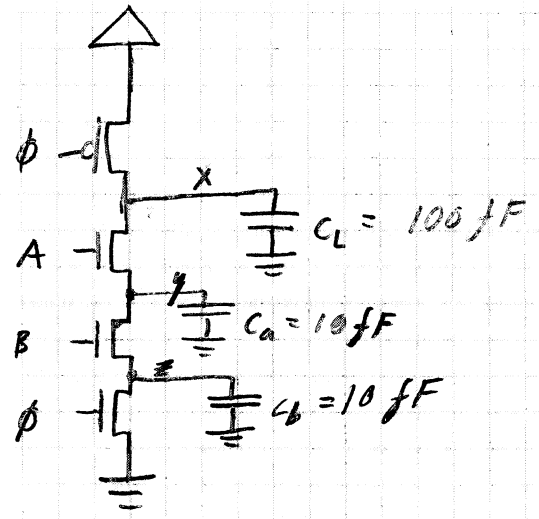
$$m_{opt} = 1{,}7\sqrt{\frac{0{,}4\cdot 10^{-9}}{12\cdot 10^{-15}\cdot 8\cdot 10^{3}}} = 3{,}47 \simeq \underline{3 \text{ gates between buffers}}$$

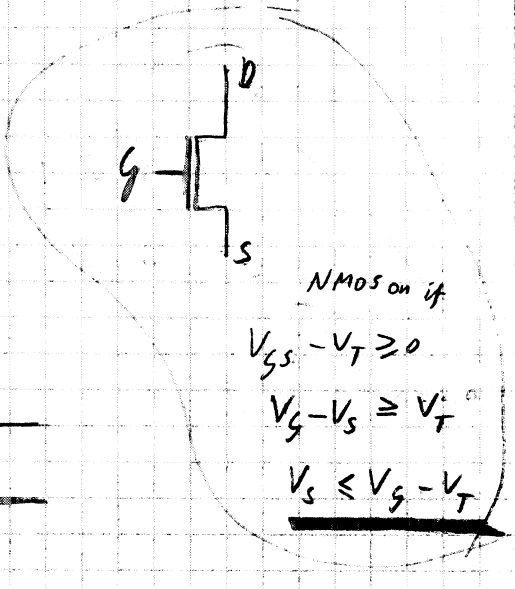
b) Suppose that, if the dimension of this process are shrunk by a factor S, R_{eq} scales as $1/S^2$, C scales as $1/S$, and t_{buf} scales as $1/S^2$. What is the expression for the optimal number of buffers as a function of S? What is the value if S = 2?

$$m_{opt,new} = 1{,}7\sqrt{\frac{t_{buf}\cdot\frac{1}{S^2}}{C\frac{1}{S}\cdot R_{eq}\frac{1}{S^2}}} = \underline{1{,}7\sqrt{\frac{t_{buf}}{CR_{eq}}}\sqrt{S}}$$

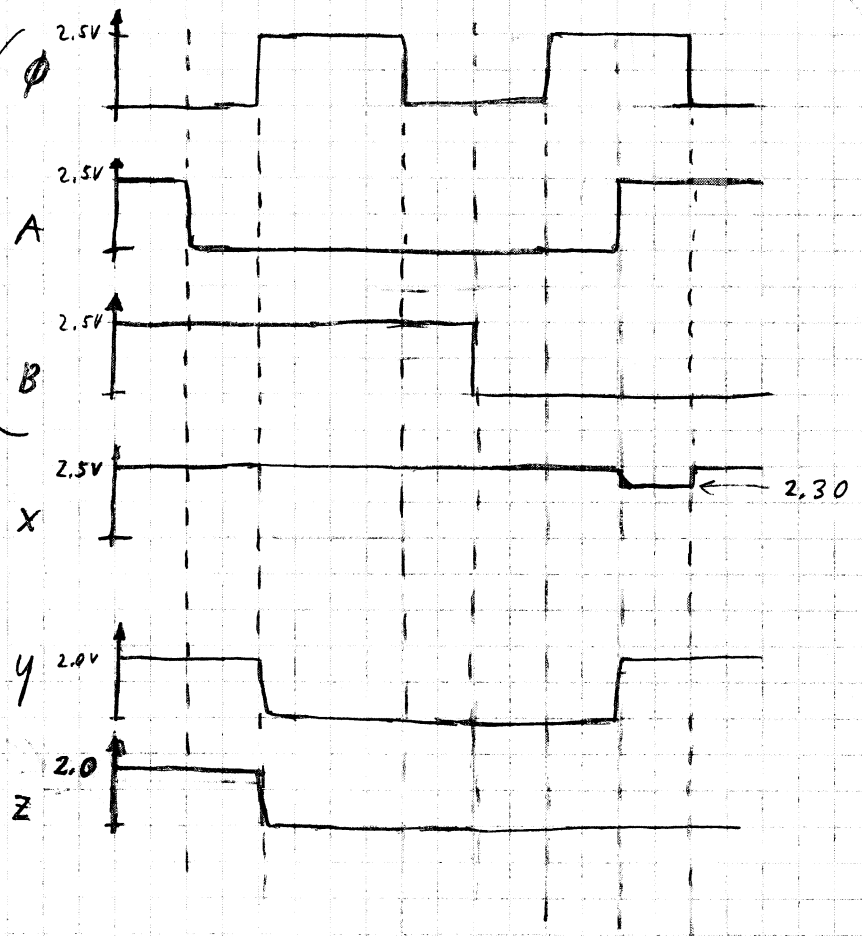
$$m_{opt,new(S=2)} = 1{,}7\sqrt{\frac{0{,}4\cdot 10^{-9}}{12\cdot 10^{-15}\cdot 8\cdot 10^{3}}}\sqrt{2} = 4{,}9074\ldots \simeq \underline{5 \text{ gates between buffers}}$$

6.19





given in circuit



$C = \frac{Q}{V}$

$Q_{tot_0} = Q_{tot_1}$

$Q_{X_0} = C_L V_{dd}$

$Q_{y_0} = 0$

$V_{y_0} = 0$

$V_{X_0} = V_{dd}$

$Q_{tot_0} = Q_{X_0} + Q_{y_0} = Q_{X_0}$

$Q_{tot_1} = Q_{X_1} + Q_{y_1}$

$= V_{X_1} C_L + V_{y_1} C_a$

(Assume $V_{X_1} \geq 2.0$ (check later) $\Rightarrow V_{y_1} = 2.0$ V)

$\Rightarrow$

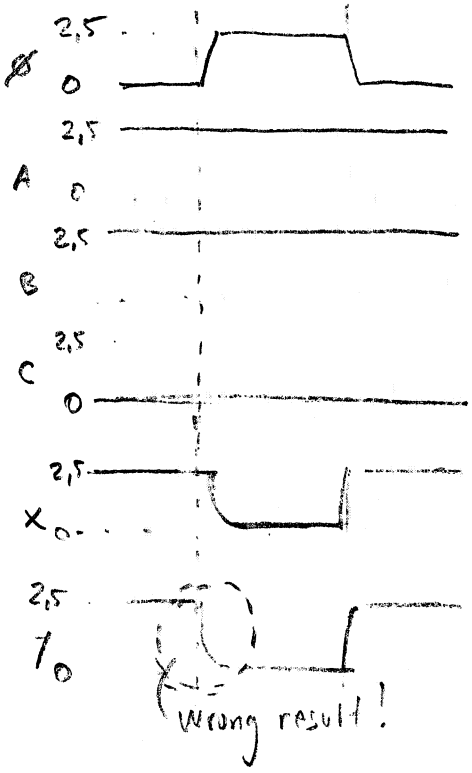
$C_L V_{dd} = V_{X_1} C_L + V_{y_1} C_a$

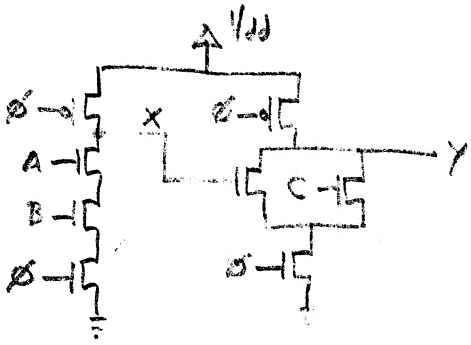
$V_{X_1} = \frac{100 \cdot 2.5 - 2.0 \cdot 10}{100}$

$V_{X_1} = 2.30$ V (Assumption $V_{X_1} \geq 2.0$ OK!)

6.20 Consider the circuit of figure 6.114

a) Give the logic function of x and y in terms of A, B, and C. Sketch the waveforms at x and y for the given inputs. Do x and y evaluate to the values you expected from their logic functions? Explain.





Cascaded dynamic gates

Logic function of x and y

$\bar{x} = AB$

$x = \overline{AB} = \bar{A} + \bar{B}$

$\bar{y} = x + C = \bar{A} + \bar{B} + C$

$y = \overline{\bar{A} + \bar{B} + C} = ABC$

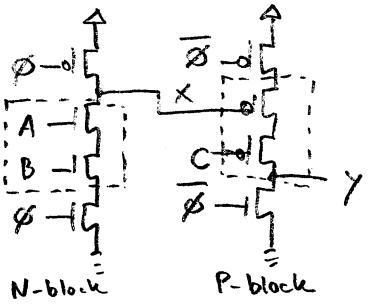
the circuit doesn't correctly implement the desired logic function. This stems from the fact that x is precharged high, and thus y is discharged as soon as the evaluation phase starts. Although x is eventually discharged by the first stage, y cannot be charged high again since it is a dynamic node with no low-impedance path to V_{dd} (during evaluate). Common solutions to this problem are to either place an inverter between the two stages (thus allowing only 0->1 transitions on the inputs to each stage during evaluate) as in domino logic or employing np-cmos. The latter is presented in b).

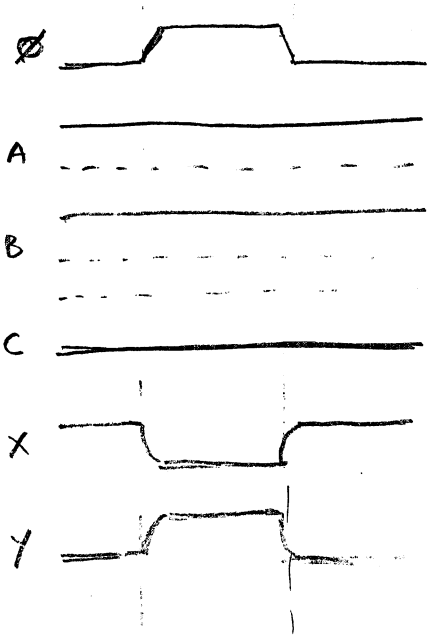
(6.20) b) Redesign the gates using np-CMOS to eliminate any race conditions. Sketch the waveforms at x and y for your new circuit.

$x = \overline{AB}$

$y = \overline{x+c} = \bar{x} \cdot \bar{c}$

$S_p = Y(\bar{x}, \bar{c}) = x \cdot c$ Pull-up network





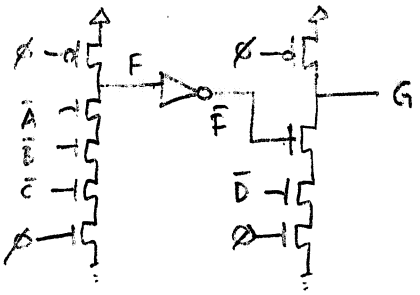
6.21) Suppose we wish to implement the two logic functions given by $F = A+B+C$ and $G = A+B+C+D$. Assume both true and complementary signals are available.

a) Implement these functions in dynamic CMOS as cascaded ϕ stages so as to minimize the total transistor count.

Using PDN-networks:

Second stage: $S_n = \bar{G} = \overline{F+D} = \bar{F}\cdot\bar{D}$

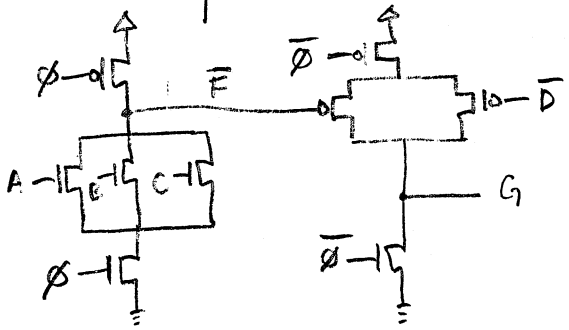
First stage: $S_n = \bar{F} = \overline{A+B+C} = \bar{A}\cdot\bar{B}\cdot\bar{C}$



b) Design an np-CMOS implementation of the same logic functions. Does this design display any of the difficulties of part a)?

Second stage: $S_p = G(\bar{F},\bar{D}) = \bar{F}+\bar{D}$

First stage: $S_n = F = (\text{no inverter on output}) = A+B+C$

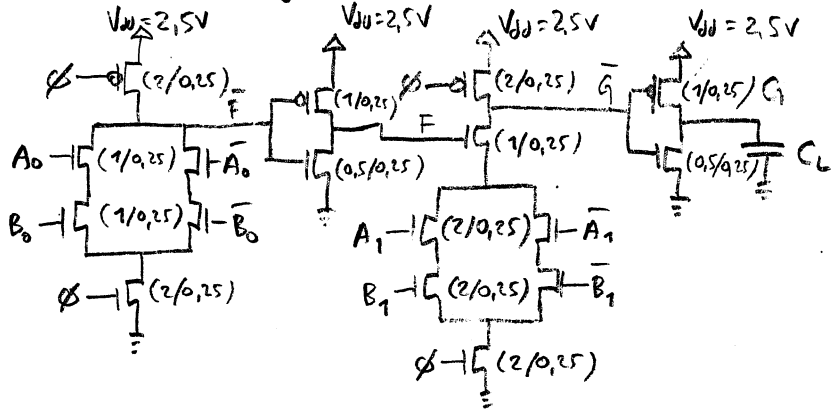


6.23 Figure 6.16 shows a dynamic CMOS circuit in Domino logic. In determining source and drain areas and perimeters, you may use the following approximations:

$AD = AS = W \cdot 0{,}625\,\mu m$

$PD = PS = W + 1{,}25\,\mu m$

Assume 0,1ns rise/fall times for all inputs, including the clock. Furthermore, you may assume that all the inputs and their complements are available, and that all inputs change during the precharge phase of the clock cycle.



a) What Boolean functions are implemented at outputs F and G? If A and B are interpreted as two-bit binary words, $A = A_1A_0$ and $B = B_1B_0$, then what interpretation can be applied to output G?

First stage: $S_n = A_0B_0 + \bar{A}_0\bar{B}_0 = \bar{\bar{F}}$

$F = A_0B_0 + \bar{A}_0\bar{B}_0$ (A_0 XNOR B_0)

Second stage: $S_n = F \cdot (A_1B_1 + \bar{A}_1\bar{B}_1) = \bar{\bar{G}}$

$G = (A_0B_0 + \bar{A}_0\bar{B}_0)(A_1B_1 + \bar{A}_1\bar{B}_1)$

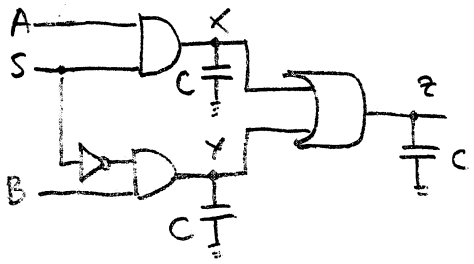
If A and B are interpred as two-bit binary words, output G is high if $A = B \Leftrightarrow$ COMPARATOR!

6.23 b) Which gate (1 or 2) has the highest potential for harmful charge sharing and why? What sequence of inputs (spanning two clock cycles) results in the worst-case charge-sharing scenario?

Gate 2 has the higher potential for harmful charge sharing since the capacitance that contributes to charge sharing is larger than in gate 1. The sequence of inputs resulting in the worst-case charge sharing is $A_0 = B_0$ and $A_1 = B_1$ for the first cycle. Then $A_0 = B_0$ and $A_1 \neq B_1$ for the second cycle such that $A_1/\overline{A_1}$ that is on during the second cycle is the same as in the first cycle. For example,

$A_0 = B_0 = A_1 = B_1 = V_{DD}$ in cycle 1 and $A_0 = B_0 = A_1 = V_{DD}$, $B_1 = 0V$ in cycle 2. This will cause the charge at the output of gate 2 to be shared with the total parasitic capacitance at the drains of the A_1, $\overline{A_1}$, and B_1 transistors.

(6.27) Figure 6.18 shows a two-input multiplexer. For this problem, assume independent, identically-distributed uniform white noise inputs.



a) Does this schematic contain reconvergent fan-out? Explain your answer.

This schematic has reconvergent fan-out because both inputs of the or-gate depend on the value of S.

b) Find the exact signal (P_1) and transition ($P_{0\to1}$) formulas for nodes X, Y, and Z for:

(1) A static, fully complementary CMOS implementation

(2) A dynamic CMOS implementation.

(1) Assuming a fully complementary CMOS implementation:

X is the output of an AND-gate with independent, identically-distributed uniform white noise inputs. Since the output is 1 only when both inputs are 1, $P_1 = 0{,}25$. On the other hand $P_{0\to1} = P_0 P_1 = 0{,}25(1-0{,}25) = 0{,}1875$. Y is also the output of an AND-gate with independent, identically-distributed uniform white noise inputs. The analysis is the same as with X.

If we represent the truth table of the schematic we will see that $P_1 = 0{,}5$ for Z. P_1 for X and P_1 for Y is 0,25 but they are never 1 at the same time

$\Rightarrow P_1 = 0{,}5$ for Z since $P_1(\text{out}) = P_1(\text{in})$ for or-gates.

6.27 b) Assuming a dynamic CMOS implementation:

continued…

The results depends on the chosen implementation. For example, two n-blocks followed by a p-block, where all blocks are NAND-gates can result in the following solution. Use

$$Z = AS + B\overline{S} = \overline{AS \cdot B\overline{S}}$$

Let the intermediate dynamic nodes be denoted as X' and Y' respectively.
For n-type blocks we have $P_{0\to1} = P_0$ while for p-type blocks we have $P_{0\to1} = P_1$
As previously $P_{X':0} = ¼$ during evaluation. In each precharge phase X' = 1 hence, $P_{X':0\to1} = ¼$ and therefore $P_{Y':0\to1} = ¼$. As for the static case we have $P_{Z':0} = ½$ so then $P_{Z':0\to1} = ½$