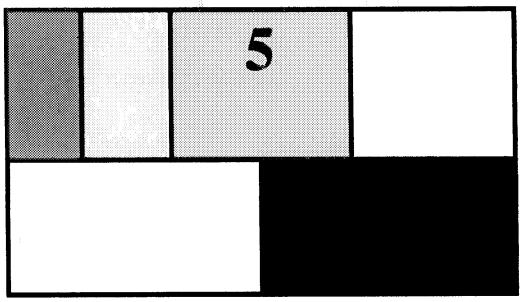
Lesson 2 & 3

CHAPTER



THE CMOS INVERTER

Quantification of integrity, performance, and energy metrics of an inverter
Optimization of an inverter design

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5.1 Exercises and Design Problems

1. [M, SPICE, 3.3.2] The layout of a static CMOS inverter is given in Figure 5.1. (λ = 0.125 μm).
   a. Determine the sizes of the NMOS and PMOS transistors.
   b. Plot the VTC (using HSPICE) and derive its parameters (V_{OH}, V_{OL}, V_M, V_{IH}, and V_{IL}).
   c. Is the VTC affected when the output of the gates is connected to the inputs of 4 similar gates?.

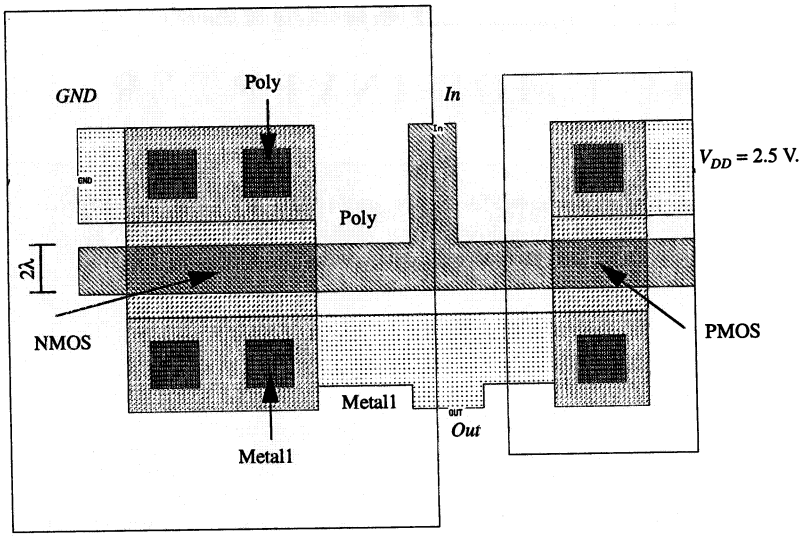


Figure 5.1 CMOS inverter layout.

   d. Resize the inverter to achieve a switching threshold of approximately 0.75 V. Do not layout the new inverter, use HSPICE for your simulations. How are the noise margins affected by this modification?

2. Figure 5.2 shows a piecewise linear approximation for the VTC. The transition region is approximated by a straight line with a slope equal to the inverter gain at V_M. The intersection of this line with the V_{OH} and the V_{OL} lines defines V_{IH} and V_{IL}.
   a. The noise margins of a CMOS inverter are highly dependent on the sizing ratio, $r = k_p/k_n$, of the NMOS and PMOS transistors. Use HSPICE with $V_{Tn} = |V_{Tp}|$ to determine the value of r that results in equal noise margins? Give a qualitative explanation.
   b. Section 5.3.2 of the text uses this piecewise linear approximation to derive simplified expressions for NM_H and NM_L in terms of the inverter gain. The derivation of the gain is based on the assumption that both the NMOS and the PMOS devices are velocity saturated at V_M. For what range of r is this assumption valid? What is the resulting range of V_M?
   c. Derive expressions for the inverter gain at V_M for the cases when the sizing ratio is just above and just below the limits of the range where both devices are velocity saturated. What are the operating regions of the NMOS and the PMOS for each case? Consider the effect of channel-length modulation by using the following expression for the small-signal resistance in the saturation region: $r_{o,sat} = 1/(\lambda I_D)$.

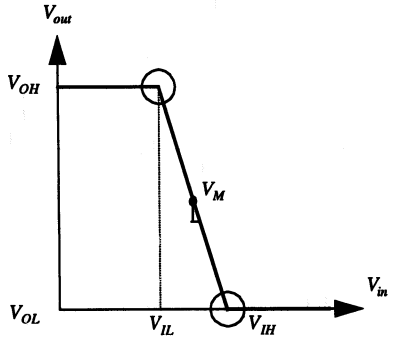


Figure 5.2 A different approach to derive V_{IL} and V_{IH}.

3. [M, SPICE, 3.3.2] Figure 5.3 shows an NMOS inverter with resistive load.
   a. Qualitatively discuss why this circuit behaves as an inverter.
   b. Find V_{OH} and V_{OL} calculate V_{IH} and V_{IL}.
   c. Find NM_L and NM_H, and plot the VTC using HSPICE.
   d. Compute the average power dissipation for: (i) $V_{in} = 0$ V and (ii) $V_{in} = 2.5$ V

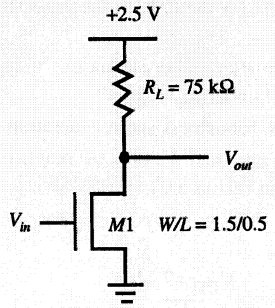


Figure 5.3 Resistive-load inverter

   e. Use HSPICE to sketch the VTCs for R_L = 37k, 75k, and 150k on a single graph.
   f. Comment on the relationship between the critical VTC voltages (i.e., V_{OL}, V_{OH}, V_{IL}, V_{IH}) and the load resistance, R_L.
   g. Do high or low impedance loads seem to produce more ideal inverter characteristics?
4. [E, None, 3.3.3] For the inverter of Figure 5.3 and an output load of 3 pF:
   a. Calculate t_{plh}, t_{phl}, and t_p.
   b. Are the rising and falling delays equal? Why or why not?
   c. Compute the static and dynamic power dissipation assuming the gate is clocked as fast as possible.
5. The next figure shows two implementations of MOS inverters. The first inverter uses only NMOS transistors.

a. Calculate V_{OH}, V_{OL}, V_M for each case.

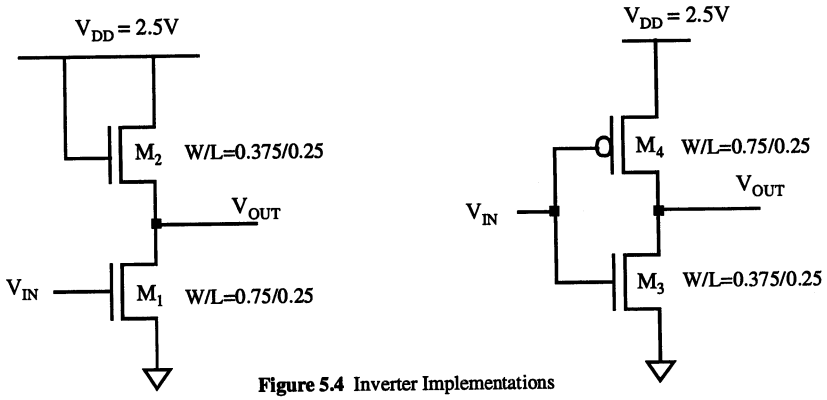


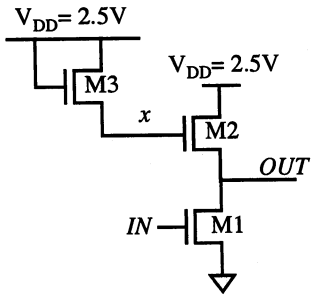
Figure 5.4 Inverter Implementations

b. Use HSPICE to obtain the two VTCs. You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, $\lambda = 0.125$ μm, and the source/drain extensions are 5λ for the PMOS; for the NMOS the source/drain contact regions are 5λx5λ.

c. Find V_{IH}, V_{IL}, NM_L and NM_H for each inverter and comment on the results. How can you increase the noise margins and reduce the undefined region?

d. Comment on the differences in the VTCs, robustness and regeneration of each inverter.

6. Consider the following NMOS inverter. Assume that the bulk terminals of all NMOS device are connected to GND. Assume that the input IN has a 0V to 2.5V swing.



a. Set up the equation(s) to compute the voltage on node *x*. Assume γ=0.5.

b. What are the modes of operation of device M2? Assume γ=0.

c. What is the value on the output node *OUT* for the case when *IN* =0V?Assume γ=0.

d. Assuming γ=0, derive an expression for the switching threshold (V_M) of the inverter. Recall that the switching threshold is the point where V_{IN}= V_{OUT}. Assume that the device sizes for M1, M2 and M3 are $(W/L)_1$, $(W/L)_2$, and $(W/L)_3$ respectively. What are the limits on the switching threshold?

For this, consider two cases:

i) $(W/L)_1 >> (W/L)_2$

ii) $(W/L)_2 >> (W/L)_1$

7. Consider the circuit in Figure 5.5. Device M1 is a standard NMOS device. Device M2 has all the same properties as M1, except that its device threshold voltage is *negative* and has a value of -0.4V. Assume that all the current equations and inequality equations (to determine the mode of operation) for the depletion device M2 are the same as a regular NMOS. Assume that the input *IN* has a 0V to 2.5V swing.

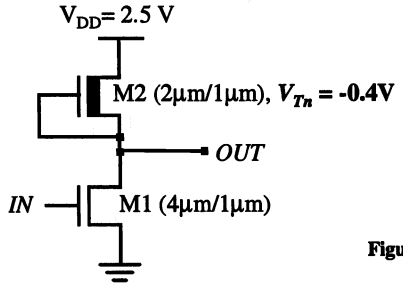


Figure 5.5 A depletion load NMOS inverter

   a. Device M2 has its gate terminal connected to its source terminal. If V_{IN} = 0V, what is the output voltage? In steady state, what is the mode of operation of device M2 for this input?
   b. Compute the output voltage for V_{IN} = 2.5V. You may assume that V_{OUT} is small to simplify your calculation. In steady state, what is the mode of operation of device M2 for this input?
   c. Assuming $Pr_{(IN=0)}$= 0.3, what is the static power dissipation of this circuit?

8. [M, None, 3.3.3] An NMOS transistor is used to charge a large capacitor, as shown in Figure 5.6.
   a. Determine the t_{pLH} of this circuit, assuming an ideal step from 0 to 2.5V at the input node.
   b. Assume that a resistor R_S of 5 kΩ is used to discharge the capacitance to ground. Determine t_{pHL}.
   c. Determine how much energy is taken from the supply during the charging of the capacitor. How much of this is dissipated in M1. How much is dissipated in the pull-down resistance during discharge? How does this change when R_S is reduced to 1 kΩ.
   d. The NMOS transistor is replaced by a PMOS device, sized so that k_p is equal to the k_n of the original NMOS. Will the resulting structure be faster? Explain why or why not.

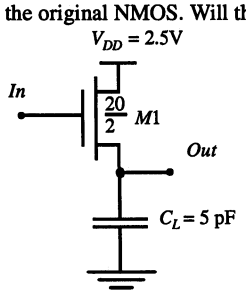


Figure 5.6 Circuit diagram with annotated *W/L* ratios

9. The circuit in Figure 5.7 is known as the *source follower* configuration. It achieves a DC level shift between the input and the output. The value of this shift is determined by the current I_0. Assume x_d=0, γ=0.4, $2|\phi_f|$=0.6V, V_{T0}=0.43V, k_n'=115μA/V^2 and λ=0.

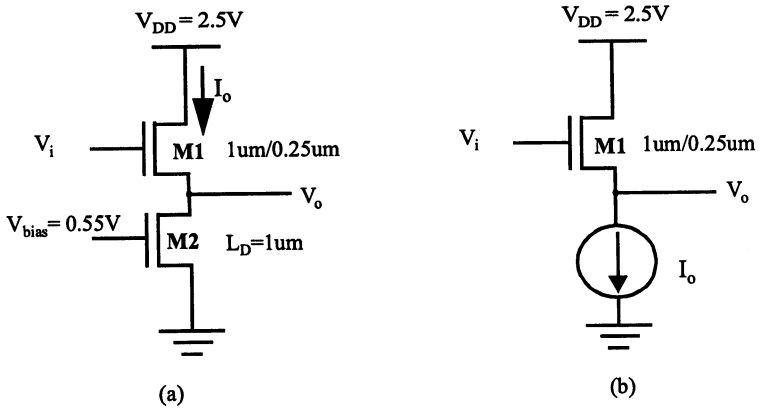


Figure 5.7 NMOS source follower configuration

a. Suppose we want the nominal level shift between V_i and V_o to be 0.6V in the circuit in Figure 5.7 (a). Neglecting the backgate effect, calculate the width of M2 to provide this level shift (Hint: first relate V_i to V_o in terms of I_o).

b. Now assume that an ideal current source replaces M2 (Figure 5.7 (b)). The NMOS transistor M1 experiences a shift in V_T due to the backgate effect. Find V_T as a function of V_o for V_o ranging from 0 to 2.5V with 0.5V intervals. Plot V_T vs. V_o

c. Plot V_o vs. V_i as V_o varies from 0 to 2.5V with 0.5 V intervals. Plot two curves: one neglecting the body effect and one accounting for it. How does the body effect influence the operation of the level converter?

d. At V_o(with body effect) = 2.5V, find V_o(ideal) and thus determine the maximum error introduced by the body effect.

10. For this problem assume:

V_{DD} = 2.5V, W_P/L = 1.25/0.25, W_N/L = 0.375/0.25, $L=L_{eff}$=0.25μm , $C_L=C_{inv\text{-}gate}$, k_n' = 115μA/V^2, k_p'= -30μA/V^2, V_{tn0} = | V_{tp0} | = 0.4V, λ = 0V^{-1}, γ = 0.4, 2|ϕ_f|=0.6V, and t_{ox} = 58A. Use the HSPICE model parameters for parasitic capacitance given below (i.e. C_{gd0}, C_j, C_{jsw}), and assume that V_{SB}=0V for all problems except part **(e)**.

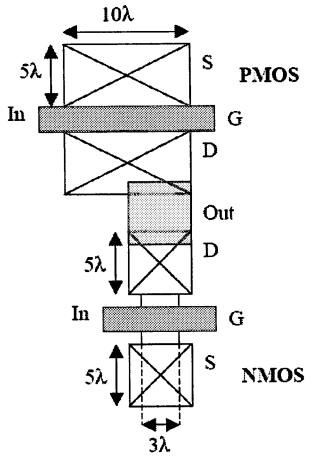


Figure for problem 5.10b

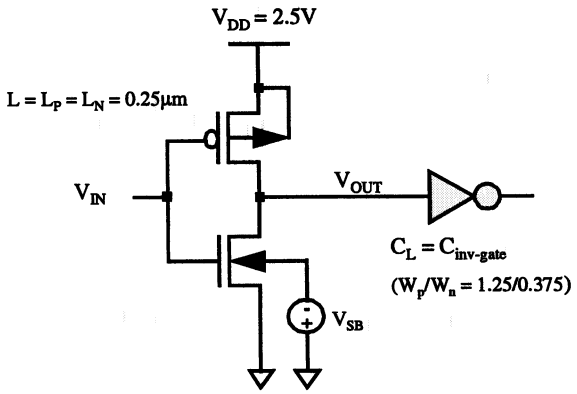


Figure 5.8 CMOS inverter with capacitive

Parasitic Capacitance Parameters (F/m)##
NMOS: CGDO=3.11x10^{-10}, CGSO=3.11x10^{-10}, CJ=2.02x10^{-3}, CJSW=2.75x10^{-10}
PMOS: CGDO=2.68x10^{-10}, CGSO=2.68x10^{-10}, CJ=1.93x10^{-3}, CJSW=2.23x10^{-10}

a. What is the V_m for this inverter?

b. What is the effective load capacitance C_{Leff} of this inverter? (include parasitic capacitance, refer to the text for K_{eq} and m.) **Hint:** You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, λ = 0.125 μm, and the source/drain extensions are 5λ for the PMOS; for the NMOS the source/drain contact regions are 5λx5λ.

c. Calculate t_{PHL}, t_{PLH} assuming the result of (b) is 'C_{Leff} = 6.5fF'. (Assume an ideal step input, i.e. t_{rise}=t_{fall}=0. Do this part by computing the average current used to charge/discharge C_{Leff})

d. Find (W_p/W_n) such that $t_{PHL} = t_{PLH}$.

e. Suppose we increase the width of the transistors to reduce the t_{PHL}, t_{PLH}. Do we get a proportional decrease in the delay times? Justify your answer.

f. Suppose V_{SB} = 1V, what is the value of V_{tn}, V_{tp}, V_m? How does this qualitatively affect C_{Leff}?

11. Using Hspice answer the following questions.

a. Simulate the circuit in Problem 10 and measure t_P and the average power for input V_{in}: pulse(0 V_{DD} 5n 0.1n 0.1n 9n 20n), as V_{DD} varies from 1V - 2.5V with a 0.25V interval. [t_P = (t_{PHL} + t_{PLH}) / 2]. Using this data, plot 't_P vs. V_{DD}', and 'Power vs. V_{DD}'.
Specify AS, AD, PS, PD in your spice deck, and manually add C_L = 6.5fF. Set V_{SB} = 0V for this problem.

b. For Vdd equal to 2.5V determine the maximum fan-out of identical inverters this gate can drive before its delay becomes larger than 2 ns.

c. Simulate the same circuit for a set of 'pulse' inputs with rise and fall times of $t_{in\_rise,fall}$ =1ns, 2ns, 5ns, 10ns, 20ns. For each input, measure (1) the rise and fall times t_{out_rise} and

t_{out_fall} of the inverter output, (2) the total energy lost E_{total}, and (3) the energy lost due to short circuit current E_{short}.

Using this data, prepare a plot of (1) $(t_{out\_rise}+t_{out\_fall})/2$ vs. $t_{in\_rise,fall}$, (2) E_{total} vs. $t_{in\_rise,fall}$, (3) E_{short} vs. $t_{in\_rise,fall}$ and (4) E_{short}/E_{total} vs. $t_{in\_rise,fall}$.

d. Provide simple explanations for:

(i) Why the slope for (1) is less than 1?

(ii) Why E_{short} increases with $t_{in\_rise,fall}$?

(iii) Why E_{total} increases with $t_{in\_rise,fall}$?

12. Consider the low swing driver of Figure 5.9:

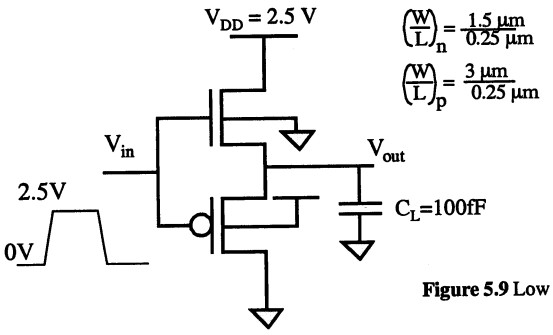


Figure 5.9 Low Swing Driver

a. What is the voltage swing on the output node (V_{out})? Assume γ=0.

b. Estimate (i) the energy drawn from the supply and (ii) energy dissipated for a 0V to 2.5V transition at the input. Assume that the rise and fall times at the input are 0. Repeat the analysis for a 2.5V to 0V transition at the input.

c. Compute t_{pLH} (i.e. the time to transition from V_{OL} to $(V_{OH} + V_{OL})/2$). Assume the input rise time to be 0. V_{OL} is the output voltage with the input at 0V and V_{OH} is the output voltage with the input at 2.5V.

d. Compute V_{OH} taking into account body effect. Assume $\gamma = 0.5V^{1/2}$ for both NMOS and PMOS.

13. Consider the following low swing driver consisting of NMOS devices M1 and M2. Assume an NWELL implementation. Assume that the inputs IN and $\overline{IN}$ have a 0V to 2.5V swing and that V_{IN} = 0V when $V_{\overline{IN}}$ = 2.5V and vice-versa. Also assume that there is no skew between IN and $\overline{IN}$ (i.e., the inverter delay to derive $\overline{IN}$ from IN is zero).

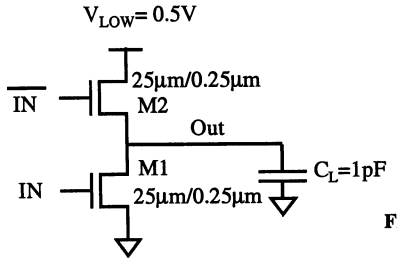


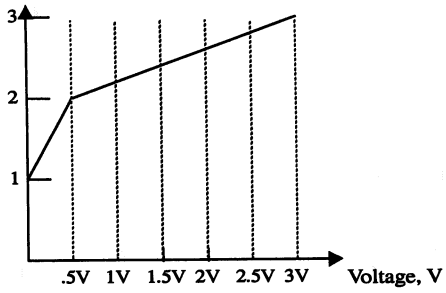
Figure 5.10 Low Swing Driver

a. What voltage is the bulk terminal of M2 connected to?

b. What is the voltage swing on the output node as the inputs swing from 0V to 2.5V. Show the low value and the high value.

c. Assume that the inputs IN and $\overline{IN}$ have zero rise and fall times. Assume a zero skew between IN and $\overline{IN}$. Determine the low to high propagation delay for charging the output node measured from the the 50% point of the input to the 50% point of the output. Assume that the total load capacitance is 1pF, including the transistor parasitics.

d. Assume that, instead of the 1pF load, the low swing driver drives a non-linear capacitor, whose capacitance vs. voltage is plotted below. Compute the energy drawn from the low supply for charging up the load capacitor. Ignore the parasitic capacitance of the driver circuit itself.



14. The inverter below operates with V_{DD}=0.4V and is composed of |Vt| = 0.5V devices. The devices have identical I_0 and n.

a. Calculate the switching threshold (V_M) of this inverter.

b. Calculate V_{IL} and V_{IH} of the inverter.

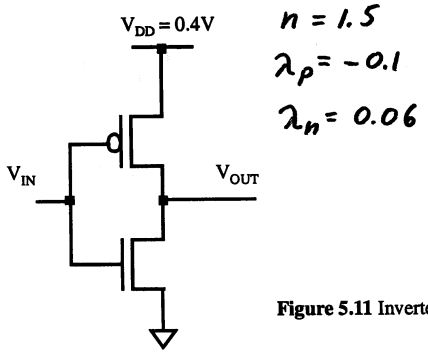


Figure 5.11 Inverter in Weak Inversion Regime

15. Sizing a chain of inverters.

a. In order to drive a large capacitance (C_L = 20 pF) from a minimum size gate (with input capacitance C_i = 10fF), you decide to introduce a two-staged buffer as shown in Figure 5.12. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume

The relation between the internal output capacitance and the input capacitance of an inverter is assumed to be γ=1.

that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.

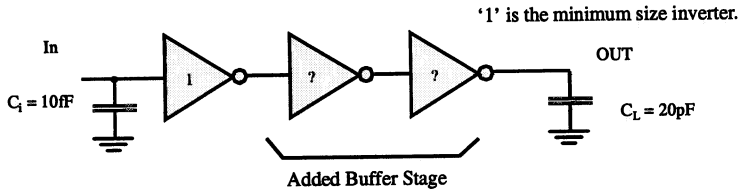


Figure 5.12 Buffer insertion for driving large loads.

b. If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

c. Describe the advantages and disadvantages of the methods shown in (a) and (b).

d. Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V and an activity factor of 1?

16. [M, None, 3.3.5] Consider scaling a CMOS technology by $S > 1$. In order to maintain compatibility with existing system components, you decide to use constant voltage scaling.

a. In traditional constant voltage scaling, transistor widths scale inversely with S, $W \propto 1/S$. To avoid the power increases associated with constant voltage scaling, however, you decide to change the scaling factor for *W*. What should this new scaling factor be to maintain approximately constant power. Assume long-channel devices (i.e., neglect velocity saturation).

b. How does delay scale under this new methodology?

c. Assuming short-channel devices (i.e., velocity saturation), how would transistor widths have to scale to maintain the constant power requirement?

(5.1) The layout of a static CMOS inverter is given in figure 5.1 ($\lambda = 0,125\mu m$)

a) Determine the sizes of the NMOS and PMOS transistors
$1\lambda = 3mm$ in picture

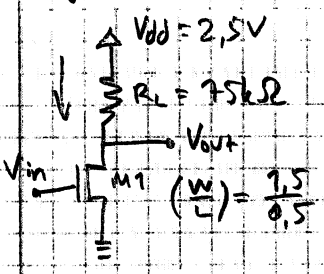
NMOS : $W_n = 8,3\lambda = 8,3 \cdot 0,125\mu m = 1,04\mu m$
$L_n = 2\lambda = 2 \cdot 0,125\mu m = 0,25\mu m$

PMOS : $W_p = 4\lambda = 4 \cdot 0,125\mu m = 0,5\mu m$
$L_p = 2\lambda = 2 \cdot 0,125\mu m = 0,25\mu m$

c) Is the VTC affected when the output of the gates is connected to the inputs of 4 similar gates?

No, the only thing that changes then is the rise and fall times. CMOS gates are purely capacitive load.

5.3 Figure 5.3 shows an NMOS inverter with resistive load.



a) Qualitatively discuss why this circuit behaves as an inverter.

$V_{in} = 0 < V_T$: M1 is off and no current flows through the transistor. V_{out} is equal to 2,5V

$V_{in} = 2,5 > V_T$: M1 is on and current flows through the transistor. There is a voltage drop over R_L and V_{out} reaches a value equal to $V_{DD} - R_L I$, which is a low value and the input is thus inverted.

b) Find V_{OH}, V_{OL} and calculate V_{IH}, V_{IL}

For $V_{in} < V_T$, Transistor M1 is off and $\underline{\underline{V_{OH} = 2,5V}}$

For $V_{in} = 2,5V$, assume M1 is in the LINEAR REGION and check later if that is so. Since V_{ds} is negligible in the linear region, channel length modulation (λ) can be ignored.

$$I_R = I_d$$

$$\frac{V_{DD} - V_{OL}}{R_L} = k'\left(\frac{W}{L}\right)\left[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}\right]$$

$$\frac{2,5 - V_{OL}}{75 \cdot 10^3} = 115 \cdot 10^{-6}\left(\frac{1,5}{0,5}\right)\left\{(2,5 - 0,43)V_{OL} - \frac{V_{OL}^2}{2}\right\}$$

$$2,5 - V_{OL} = 75 \cdot 10^3 \cdot 115 \cdot 10^{-6}\left(\frac{1,5}{0,5}\right)\left[2,07 V_{OL} - \frac{V_{OL}^2}{2}\right]$$

$$2,5 - V_{OL} = 53,56125 V_{OL} - 12,9375 V_{OL}^2$$

$$V_{OL}^2 - \frac{54,56125}{12,9375} V_{OL} + \frac{2,5}{12,9375} = 0$$

$$V_{OL}^2 - 4,2173 V_{OL} + 0,1932 = 0$$

$$V_{OL} = 2,1086 \pm \sqrt{2,1086^2 - 0,1932}$$

$$V_{OL} = 2,1086 \pm 2,0623 \;;\; V_{OL} \approx \underline{\underline{46,3\,mV}}$$

5.3 continued...

b) To find V_M, set the resistor current equal to the NMOS current, with an input voltage equal to V_M. Assume saturation, check later if that assumption is true.

$$I_{R_L} = I_{D,sat}$$

$$\frac{V_{DD} - V_M}{R_L} = \frac{k'}{2}\left(\frac{W}{L}\right)(V_M - V_T)^2(1 + \lambda V_M)$$

$$\frac{2,5 - V_M}{75 \cdot 10^3} = \frac{115 \cdot 10^{-6}}{2}\left(\frac{1,5}{0,5}\right)(V_M - 0,43)^2(1 + 0,06 V_M)$$

Using HP calculator:

$$V_M = 0,786\,V$$

~~$V_M = +0,09\,V$~~
~~$V_M = -76,6\,V$~~

To find V_{IL} and V_{IH}, the slope of the VTC, at V_M, is derived and the line is extrapolated out to V_{OH} and V_{OL} respectively. Ignoring effects of channel length modulation:

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k'}{2}\frac{W}{L}(V_{in} - V_T)^2$$

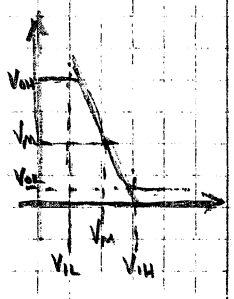
$$V_{out} = V_{DD} - R_L\frac{k'}{2}\frac{W}{L}(V_{in} - V_T)^2$$

The slope is given by:

$$\frac{dV_{out}}{dV_{in}} = -\cancel{2}R_L\frac{k'}{\cancel{2}}\frac{W}{L}(V_{in} - V_T)$$

Insert $V_M = 0,786\,V$:

$$\left.\frac{dV_{out}}{dV_{in}}\right|_{V_M} = -75 \cdot 10^3 \cdot 115 \cdot 10^{-6}\left(\frac{1,5}{0,5}\right)(0,786 - 0,43) = -9,21$$



$$V_{IH} = V_M - \frac{V_M - V_{OL}}{\left.\frac{dV_{out}}{dV_{in}}\right|_{V_M}} = 0,786 - \frac{0,786 - 46,3 \cdot 10^{-3}}{-9,21} = 0,8663... \approx \underline{0,87\,V}$$

$$V_{IL} = V_M + \frac{V_{OH} - V_M}{\left.\frac{dV_{out}}{dV_{in}}\right|_{V_M}} = 0,786 + \frac{2,5 - 0,786}{-9,21} = 0,59989... \approx \underline{0,60\,V}$$

$$S = \frac{V_{OL} - V_M}{V_{IH} - V_{in}}$$

$$S(V_{in} - V_M) = V_{OL} - V_M$$

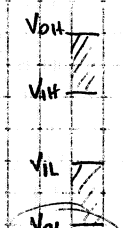
$$V_{in} = V_M$$

5.3

c) Find NM_L and NM_H

$NM_L = V_{IL} - V_{OL} = 0,60 - 46,3 \cdot 10^{-3} = 0,5537 \approx \underline{\underline{0,55V}}$

$NM_H = V_{OH} - V_{IH} = 2,5 - 0,87 = \underline{\underline{1,63V}}$



I boken är denna satt till NOLL (för CMOS).

d) Compute the average power dissipation for

(i) $V_{in} = 0V$

No power dissipation since M1 is cut off ($I_{VDD} = 0$)

(ii) $V_{in} = 2,5V$

$I_{VDD} = \dfrac{V_{DD} - V_{OL}}{R_L}$

$P_{VDD} = I_{VDD} \cdot V_{DD} = 2,5 \cdot \dfrac{2,5 - 46,3 \cdot 10^{-3}}{75 \cdot 10^3} = \underline{\underline{87,75 \mu W}}$

(5.4)

For the inverter of figure 5.3 and an output load of 3 pF:

a) Calculate t_{plh}, t_{phl}, and t_p.

t_{plh} is equivalent to charging the output capacitance through a resistance.

$$t_{plh} = 0,69 R_L C_L = 0{,}69 \cdot 75 \cdot 10^3 \cdot 3 \cdot 10^{-12} = 155.25 \text{ ns}$$

$t_{phl} = 0.69 R_{avg} C_L$, where $R_{avg} = \frac{R_{on}(V_{dd}) + R_{on}(V_{dd}/2)}{2}$

$$R_{on}(Vdd) = \frac{V_{dd}}{I_d(V_{dd})} = \left/ \begin{array}{c} V_{ds} > V_{gs} - V_T \\ V_d > V_g - V_T \\ 2.5 > 2.5\text{-}V_T \\ \text{OK! SAT!} \end{array} \right/ = \frac{V_{dd}}{k'\left(\frac{W}{L}\right)\left[(V_{gs} - V_T)V_{min} - \frac{V_{min}^2}{2}\right](1 + \lambda V_{ds})}$$

$$= \left/ \begin{array}{c} V_{min} = \min\{(V_{gs} - V_T); V_{ds}; V_{dsat}\} = \\ = \min\{2.01;\ 2.5;\ 1.26\} = 1.26 \text{ V} \end{array} \right/ = \frac{2.5}{115 \cdot 10^{-6}\left(\frac{1.5}{0.5}\right)\left[(2.5\text{-}0.43)1.26 - \frac{1.26^2}{2}\right](1 + 0.06 \cdot 2.5)} = 3473\Omega$$

$$R_{on}(Vdd/2) = \frac{Vdd/2}{I_d(Vdd/2)} = \left/ \begin{array}{c} V_{min} = \min\{(V_{gs} - V_T); V_{ds}; V_{dsat}\} = \\ = \min\{2.07;\ 1.25;\ 1.26\} = 1.25 \text{ V} \end{array} \right/ =$$

$$= \frac{1.25}{115 \cdot 10^{-6}\left(\frac{1.5}{0.5}\right)\left[(2.5\text{-}0.43) \cdot 1.25 - \frac{1.25^2}{2}\right](1 + 0.06 \cdot 1.25)} = 1866\Omega$$

$$R_{avg} = \frac{3473 + 1866}{2} = 2670\Omega$$

$$\Rightarrow t_{phl} = 0.69 \cdot \left[\frac{3473 + 1866}{2}\right] \cdot 3 \cdot 10^{-12} = 5.53 \text{ ns}$$

$$\Rightarrow t_p = \frac{t_{plh} + t_{phl}}{2} = \frac{155.25 + 5.53}{2} = 80.39 \text{ ns}$$

b) Are the rising and falling delays equal? Why or why not?

No, they are different. $t_{plh} \gg t_{phl}$ since $R_L = 75 \text{ k}\Omega$ is much larger than the effective on-resistance of transistor M1.

5.4 continued...

c) Compute the STATIC and DYNAMIC power dissipation assuming the gate is clocked as fast as possible.

* STATIC POWER (see 5.3b):

$V_{in} = V_{OL}$ gives $V_{out} = V_{DD}$, thus $I_{VDD} = 0$ so $P_{VDD} = 0\,W$

$V_{in} = V_{OH}$ gives $V_{out} = V_{OL} = 46{,}3\,mV$; M1 is in the linear region

which gives $I_{VDD} = 32{,}4\,\mu A \Rightarrow P_{VDD} = V_{DD} \cdot I_{VDD} = 81{,}75\,\mu W$

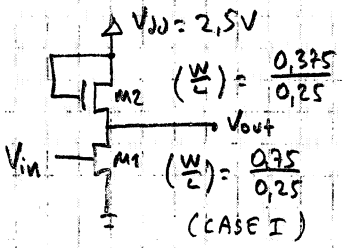
* DYNAMIC POWER:

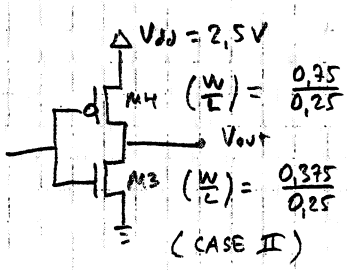
$$P_{dyn} = I_{avg} \cdot V_{DD} = f_{max} \cdot C_L \cdot \Delta V \cdot V_{DD} = \left(\frac{1}{t_p}\right) \cdot C_L \cdot (V_{OH} - V_{OL}) \cdot V_{DD} =$$

$$= \frac{1}{82{,}15 \cdot 10^{-9}} \cdot 3 \cdot 10^{-12} \cdot (2{,}5 - 46{,}3 \cdot 10^{-3}) \cdot 2{,}5 = 0{,}224\,mW$$

Comment: The maximal data input rate (frequency) of this gate can in reality not be 1/tp, since the charging takes much longer time compared with the discharging. (The output will only reach about 0.8 V (2.5 V power supply) in this case).

(5.5) Two implementations of MOS inverters are shown. The first uses only NMOS transistors.





a) Calculate V_{OH}, V_{OL}, V_M for each case

CASE I:

V_{OH} is calculated when $V_{in} = 0V$

The threshold voltage for M2 is then

$$V_T = V_{T0} + \gamma\left[\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}\right]$$

$V_{SB} = V_{out}$; $\gamma = 0,4\,V^{1/2}$; $|2\phi_F| = 0,6V$

M2 is off when $V_{gs} - V_T = V_{DD} - V_{out} - V_T = 0$

This gives:

$$V_{DD} - V_{out} - V_T = V_{DD} - V_{out} - V_{T0} - \gamma\left[\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}\right] = 0$$

$$0 = 2,5 - 0,43 - 0,4\left[\sqrt{V_{out} + 0,6} - \sqrt{0,6}\right] - V_{out}$$

Graphical solution on calculator gives one not in the region of interest:

$V_{out} = 1,7647... \approx 1,765\,V$

5.9 continued...

a) V_{OL}: To calculate V_{OL} we set $V_{in} = 2,5$ V.
We expect $V_{out} = V_{OL}$ to be low, so we can make the assumption that M2 will be velocity saturated and M1 will be in the linear region (check later)

For M2: $I_{d2} = k_n' \frac{W_2}{L_2}\left[(V_{gs}-V_T)V_{dsat} - \frac{V_{dsat}^2}{2}\right](1+\lambda V_{ds})$

For M1: $I_{d1} = k_n' \frac{W_1}{L_1}\left[(V_{gs}-V_{T0})V_{ds} - \frac{V_{ds}^2}{2}\right](1+\lambda V_{ds})$

Set $I_{d1} = I_{d2}$

$$k_n' \frac{W_2}{L_2}\left[(V_{DD}-V_{out}-V_{T0}-\gamma\left(\sqrt{V_{out}+|2\phi_F|}-\sqrt{|2\phi_F|}\right))V_{dsat} - \frac{V_{dsat}^2}{2}\right](1+\lambda(V_{DD}-V_{out})) =$$

$$k_n' \frac{W_1}{L_1}\left[(V_{in}-V_{T0})V_{out} - \frac{V_{out}^2}{2}\right](1+\lambda V_{out})$$

$$1,5\left[(2,5-V_{out}-0,43-0,4\left(\sqrt{V_{out}+0,6}-\sqrt{0,6}\right))0,63 + \frac{0,63^2}{2}\right](1+0,06(2,5+V_{out})) =$$

$$3\left[(2,5-0,43)V_{out} - \frac{V_{out}^2}{2}\right](1+0,06\cdot V_{out})$$

Graphical solution on HP48: (only two roots in region of interest)

$V_{out(1)} = 0,260048 \approx 0,26$ V

($V_{out(2)} = 4,46398$) unrealistic!

ASSUMPTION REGARDING REGION OF OPERATION HOLDS

V_M: To calculate V_M we set $V_M = V_{in} = V_{out}$.
Assuming that both transistors are velocity saturated, we get the next pair of equations:

$$I_{d1} = k_n' \frac{W_1}{L_1}\left[(V_M-V_{T0})V_{dsat} + \frac{V_{dsat}^2}{2}\right](1+\lambda V_M)$$

$$I_{d2} = k_n' \frac{W_2}{L_2}\left[(V_{DD}-V_M-V_{T0}-\gamma\left[\sqrt{V_M+|2\phi_F|}-\sqrt{|2\phi_F|}\right])V_{dsat} - \frac{V_{dsat}^2}{2}\right](1+\lambda(V_{DD}-V_M$$

Set $I_{d1} = I_{d2}$, and solve for V_M

$$3\left[(V_M-0,43)0,63 - \frac{0,63^2}{2}\right](1+0,06V_M) =$$

$$= 1,5\left[(2,5-V_M-0,43-0,4\left[\sqrt{V_M+0,6}-\sqrt{0,6}\right])0,63 - \frac{0,63^2}{2}\right](1+0,06(2,5-V_M))$$

5.5 continued...

Graphical solution on HP48GX gives only one root in region of interest:

$V_M = 1,01989 \approx \underline{\underline{1,02\ V}}$

CASE II: Static CMOS inverter

When $V_{in} = 0$, the NMOS transistor is off and the PMOS transistor is on which pulls V_{out} up to V_{DD}, so $\underline{\underline{V_{OH} = V_{DD}}}$.

Similarly, when $V_{in} = 2,5V$, the PMOS transistor is off and the NMOS transistor pulls V_{out} to ground, so $\underline{\underline{V_{OL} = 0V}}$.

To calculate V_M we set $V_M = V_{in} = V_{out}$.

We assume both transistors are velocity saturated.

We get the following pair of equations:

$$I_{d4} = K_p' \frac{W_4}{L_4}\left[(V_M - V_{DD} - V_{T0,p})V_{dsatp} - \frac{V_{dsatp}^2}{2}\right](1+\lambda_p(V_M - V_{DD}))$$

$$I_{d3} = k_n' \frac{W_3}{L_3}\left[(V_M - V_{T0,n})V_{dsatn} - \frac{V_{dsatn}^2}{2}\right](1+\lambda_n \cdot V_M)$$

$V_{T0,n} = 0,43V$; $V_{dsatn} = 0,63V$; $k_n' = 115\,\mu A/V^2$; $\lambda_n = 0,06\,V^{-1}$

$V_{T0,p} = -0,4V$; $V_{dsatp} = -1V$; $k_p' = 30\,\mu A/V^2$; $\lambda_p = -0,1\,V^{-1}$

Set $I_{d4} = I_{d3}$ and solve for V_M

$$30 \cdot 3\left[(2,5 - V_M - |-0,4|)|-1| - \frac{(-1)^2}{2}\right](1+|-0,1|(2,5-V_M)) =$$

$$115 \cdot 1,5\left[(V_M - 0,43)0,63 - \frac{0,63^2}{2}\right](1+0,06 \cdot V_M)$$

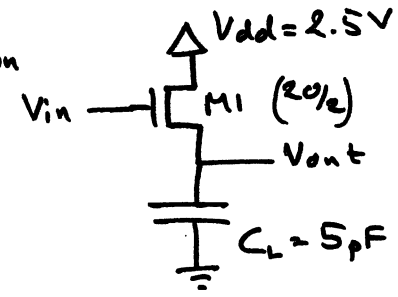
Graphical solution on calculator gives only one root in region of interest:

$V_M = 1,145188... \approx \underline{\underline{1,145\ V}}$

5.8

An NMOS transistor is used to charge a large capacitor, as shown in Figure 5.6

a) Determine the t_{pLH} of this circuit, assuming an ideal step from 0 to 2.5 V at the input node



t_{pLH}: To determine the propagation delay an average current has to be calculated between the start of the transition and the midpoint of the transition (50% of its final value).

At the start of the transition: $V_{out} = V_{OL} = 0V$, M1 is saturated, long channel device is NOT velocity saturated ($\lambda \approx 0$)

$$I_{dsat} = \frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{gs}-V_T)^2 = \frac{115\cdot10^{-6}}{2}\cdot\left(\frac{20}{2}\right)\cdot(2.5-0.43)^2 = 2.464\,mA$$

To find the voltage swing, V_{OH} must be calculated using the body effect:

$$V_{gs}-V_T = 0 \Rightarrow V_{in}-V_{OH}-V_{TO}-\gamma\left(\sqrt{V_{OH}+|2\phi_F|}-\sqrt{|2\phi_F|}\right)=0$$

$$2.5-V_{OH}-0.43-0.4\left(\sqrt{V_{OH}+0.6}-\sqrt{0.6}\right)=0$$

Solving, or graphical solution, gives $V_{OH} = 1.765\,V$

The midpoint is thus: $\frac{V_{OH}+V_{OL}}{2} = \frac{1.765+0}{2} \approx 0.88\,V$

and the threshold voltage at the midpoint is

$$V_T(V_{out}=0.88V) = V_{TO}+\gamma\left(\sqrt{V_{out}+|2\phi_F|}-\sqrt{|2\phi_F|}\right) =$$

$$0.43+0.4\left(\sqrt{0.88+0.6}-\sqrt{0.6}\right) = 0.607\,V$$

$$I(V_{out}=0.88V) = \frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{gs}-V_T)^2 = \frac{115\cdot10^{-6}}{2}\left(\frac{20}{2}\right)\cdot(2.5-0.88-0.607)^2 =$$

$$\approx 0.59\,mA$$

The average current between $V_{out}=0V$ and $V_{out}=0.88V$ is $\frac{2.464+0.59}{2}\,mA = 1.527\,mA$

5.8

continued

$$t_p = \frac{C_L \Delta V}{I_{avg}} = \frac{5 \cdot 10^{-12} \cdot 0.88}{1.527 \cdot 10^{-3}} = 2.88\,ns$$

b) Assume that a resistor R_s of 5kΩ is used to discharge the capacitance to ground. Determine t_{pHL}

$$t_{pHL} = 0.69 \cdot R_s \cdot C_L = 0.69 \cdot 5 \cdot 10^3 \cdot 5 \cdot 10^{-12} = 17.25\,ns$$

c) Determine how much energy is taken from the supply during the charging of the capacitor. How much of this is dissipated in M1? How much is dissipated in the pull-down resistance during discharge? How does this change when R_s is reduced to 1kΩ?

$$\Delta Q_{vdd} = C_L \Delta V = 5 \cdot 10^{-12} \cdot 1.765 = 8.8\,pC$$

$$\Delta E_{vdd} = \int_0^\infty i_{VDD}(t) V_{DD} \cdot dt = V_{DD} \cdot \int_0^\infty C_L \frac{dV_{out}}{dt} \cdot dt = C_L \cdot V_{DD} \cdot \int_0^{V_{OH}} dv_{out} = C_L V_{DD} V_{OH}$$

$$= C_L \cdot V_{DD} \cdot V_{OH} = 5 \cdot 10^{-12} \cdot 2.5 \cdot 1.765 = 22\,pJ$$

$$\Delta E_C = \int_0^\infty i_{VDD}(t) v_{out} dt = \int_0^\infty C_L \frac{dv_{out}}{dt} v_{out} dt = C_L \int_0^{V_{OH}} v_{out} dv_{out} = \frac{C_L V_{OH}^2}{2}$$

$$= \frac{5 \cdot 10^{-12} \cdot (1.765)^2}{2} = 7.8\,pJ$$

ΔE_C is dissipated in the resistor regardes of its size and $\Delta E_{vdd} - \Delta E_C = 14.2\,pJ$ is dissipated in transistor M1

d) The NMOS transistor is replaced by a PMOS device, sized so that k_p is equal to the k_n of the original NMOS. Will the resulting structure be faster? Explain why or why not.

The PMOS will have no body effect in this setup so that the structure will be faster.

5.10

For this problem, assume

$V_{DD} = 2,5V$ | $k_n' = 115 \mu A/V^2$
$W_p/L = 1,25/0,25$ | $k_p' = -30 \mu A/V^2$
$W_N/L = 0,375/0,25$ | $V_{tn0} = |V_{tp0}| = 0,4V$
$L = L_{eff} = 0,25 \mu m$ | $\lambda = 0V^{-1}$
(i.e. $X_d = 0 \mu m$) | $\gamma = 0,4$
$C_L = C_{inv-gate}$ | $2|\phi_F| = 0,6V$
| $t_{ox} = 58 Å$

Use the HSPICE model parameters for parasitic capacitance given below (i.e. C_{gdo}, C_j, C_{jsw}), and assume that $V_{SB} = 0V$ for all problems except part e.

PARASITIC CAPACITANCE PARAMETERS (F/m)

NMOS: $CGDO = 3,11 \cdot 10^{-10}$ / $CGSO = 3,11 \cdot 10^{-10}$ / $CJ = 2,02 \cdot 10^{-3}$ / $CJSW = 2,75 \cdot 10^{-10}$

PMOS: $CGDO = 2,68 \cdot 10^{-10}$ / $CGSO = 2,68 \cdot 10^{-10}$ / $CJ = 1,93 \cdot 10^{-3}$ / $CJSW = 2,23 \cdot 10^{-10}$

$V_{dsat} = \min\{V_{gt}; V_{dd}; V_{dsat}\}$

NMOS:
$V_{min} = \min\{V_M - V_t; V_M; V_{dsat}\} = \min\{0,82; 1,25; 0,63\}$

PMOS:
$V_{min} = \min\{0,85; 1,25; 1\}$

a) What is V_M for this inverter?

Assume that V_M is around 1,25V. This means the NMOS is velocity saturated and the PMOS is saturated (check later if this is correct)

At V_M: $I_{on} = I_{dp}$

$$k_n' \frac{W_n}{L_n}\left[(V_M - V_{Tn})V_{dsat} - \frac{V_{dsat}^2}{2}\right] = \frac{k_p'}{2}\frac{W_p}{L_p}(V_{dd} - V_M - |V_{tp}|)^2$$

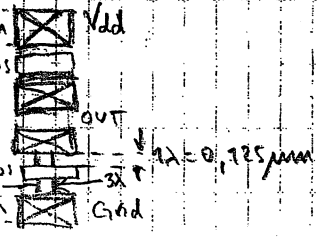
$$115 \cdot \frac{0,375}{0,25}\left[(V_M - 0,4)0,63 - \frac{0,63^2}{2}\right] = \frac{30}{2} \cdot \frac{1,25}{0,25}(2,5 - V_M - 0,4)^2$$

Graphical solution on HP48:

$\Rightarrow V_M \approx 1,233V$; Assumption OK!

b) What is the effective load capacitance C_{Leff} of this inverter? (include parasitic capacitance, refer to text for K_{eq} and m)

HINT: You must assume certain values for the source, drain areas and perimeters since there is no layout. For our scalable CMOS process, $\lambda = 0,125 \mu m$ and the source/drain extensions are 5λ for the PMOS. For the NMOS the source/drain contact regions are $5\lambda \times 5\lambda$



5.10 continued...

b) See Example 5.3 pp 195-199

$$C_{Leff} = C_L + C_{parasitic} = \underbrace{C_{g3} + C_{g4}}_{C_L = C_{inv-gate}} + \underbrace{C_{dbp} + C_{dbn} + C_{gdp} + C_{gdn}}_{C_{parasitic}}$$

$$C_L = C_{inv-gate} = (C_{gdo,n} + C_{gso,n}) W_n + \overbrace{C_{ox}}^{\text{tab. 3-5}} W_n L_n +$$
$$+ (C_{gdo,p} + C_{gso,p}) W_p + C_{ox} W_p L_p =$$
$$= 2(3{,}11 \cdot 10^{-10}) \cdot 0{,}375 \cdot 10^{-6} + 6 \cdot 10^{-15} \cdot 0{,}375 \cdot 0{,}25 +$$
$$+ 2(2{,}68 \cdot 10^{-10}) \cdot 1{,}25 \cdot 10^{-6} + 6 \cdot 10^{-15} \cdot 1{,}25 \cdot 0{,}25 =$$
$$= 0{,}79575\,fF + 2{,}545\,fF \approx 3{,}341\,fF$$

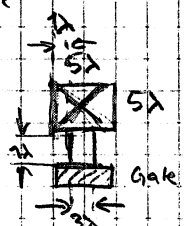
$$C_{dbn} = K_{eqn}(AD_n) C_j + K_{eqswn}(PD_n) C_{jsw}$$

Need to do this calculation for both transitions and average the result. The K_{eq}-values are already calculated in the text (p. 196)

$$AD_p = AS_p = \underset{(W_p)}{1{,}25} \cdot \underset{(L_D)}{0{,}625}\,\mu m^2 = 0{,}78125\,\mu m^2$$

Since NMOS is not as wide as PMOS.

$$\begin{cases} AD_n = AS_n = \underset{(W_n)}{0{,}375} \cdot \underset{(L_D)}{0{,}125} + \underset{(5\lambda)^2 = \text{contact}}{0{,}625^2}\,\mu m^2 = 0{,}4375\,\mu m^2 \\ PD_p = PS_p = \underset{(2 \cdot L_D)}{2 \cdot 0{,}625} + \underset{(W_p)}{1{,}25} = 2{,}5\,\mu m \\ PD_n = PS_n = \underset{(\text{contact})}{5 \cdot 0{,}125} \cdot 3 + (2+1+1)\,0{,}125 = 2{,}375\,\mu m \end{cases}$$



NMOS: H→L $K_{eq} = 0{,}57$; $K_{eqsw} = 0{,}61$
L→H $K_{eq} = 0{,}79$; $K_{eqsw} = 0{,}81$

↑ Multiplication factor

H→L: $C_{dbn} = 0{,}57 \cdot 0{,}4375 \cdot 2{,}02 + 0{,}61 \cdot 2{,}375 \cdot 0{,}275 = 0{,}902\,fF$

L→H: $C_{dbn} = 0{,}79 \cdot 0{,}4375 \cdot 2{,}02 + 0{,}81 \cdot 2{,}375 \cdot 0{,}275 = 1{,}227\,fF$

$C_{dbn,average} \approx 1{,}065\,fF$

$$C_{dbp} = K_{eqp}(AD_p) C_j + K_{eqswp}(PD_p) C_{jsw}$$

PMOS: H→L $K_{eq} = 0{,}79$; $K_{eqsw} = 0{,}86$
L→H $K_{eq} = 0{,}59$; $K_{eqsw} = 0{,}70$

H→L: $C_{dbp} = 0{,}79 \cdot 0{,}78125 \cdot 1{,}93 + 0{,}86 \cdot 2{,}5 \cdot 0{,}223 = 1{,}6706\,fF$

L→H: $C_{dbp} = 0{,}59 \cdot 0{,}78125 \cdot 1{,}93 + 0{,}7 \cdot 2{,}5 \cdot 0{,}223 = 1{,}2798\,fF$

$C_{dbp,average} \approx 1{,}475$

5.10 continued...

b)

Miller (gate and output node swing in opposite directions)

$C_{gdn} = (2) C_{GDOn} \cdot W_n = 2 \cdot 3{,}11 \cdot 10^{-10} \cdot 0{,}375 \cdot 10^{-6} = 0{,}233\,fF$

$C_{gdp} = 2 \cdot C_{GDOp} \cdot W_p = 2 \cdot 2{,}68 \cdot 10^{-10} \cdot 1{,}25 \cdot 10^{-6} = 0{,}67\,fF$

$C_{Leff} = C_{inv\text{-}gate} + C_{db_p,average} + C_{db_n,average} + C_{gdn} + C_{gdp} =$

$= 3{,}341 + 1{,}065 + 1{,}475 + 0{,}233 + 0{,}67 = \underline{\underline{6{,}784\,fF}}$

c) Calculate t_{PHL}, t_{PLH} assuming the result of (b) is $C_{Leff} = 6{,}5\,fF$ (assume an ideal step input, i.e. $t_{rise} = t_{fall} = 0$. Do this part by computing the average current used to charge/discharge C_{Leff})

We can approximate the propagation delay by using $\Delta t = \Delta Q / I$, where $\Delta Q = C_{Leff} \cdot V_{DD}$ and I is the average current used to charge/discharge C_{Leff}.

$t_{delay} \approx \dfrac{(V_{DD}/2) \cdot C_{Leff}}{I_{avg}}$ ($V_{DD}/2$ is ΔV defined for propagation delay)

* t_{PLH} (charge C_{Leff} through the PMOS)

$I_{avg} = \dfrac{I_d(V_{out}=0) + I_d(V_{out}=V_{DD}/2)}{2}$

$I_d(V_{out}=0) = \Big/ V_{min} = \min\{(V_{sg}-|V_{TP}|); V_{sd}; V_{sat}\} = \min\{2{,}1; 2{,}5; 1\} = 1 \Big/ = k_p'\left(\frac{W_p}{L_p}\right)\left[(V_{sg}-|V_{TP}|)V_{min} - \frac{V_{min}^2}{2}\right] =$

$= 30 \cdot 10^{-6}\left(\frac{1{,}25}{0{,}25}\right)\left[(2{,}5-0{,}4)1 - \frac{1^2}{2}\right] = 0{,}24\,mA$

$I_d(V_{out}=1{,}25) = \Big/ V_{min} = \min\{2{,}1; 1{,}25; 1\} = 1 \Big/ = 0{,}24\,mA$

$\Rightarrow t_{PLH} = \dfrac{1{,}25 \cdot 6{,}5 \cdot 10^{-15}}{0{,}24 \cdot 10^{-3}} \approx \underline{\underline{33{,}9\,ps}}$

* t_{PHL} (discharge C_{Leff} through the NMOS)

$I_{avg} = \dfrac{I_d(V_{out}=V_{DD}) + I_d(V_{out}=V_{DD}/2)}{2}$

$I_d(V_{out}=V_{DD}) = \Big/ V_{min} = \min\{(V_{gs}-V_T); V_{ds}; V_{sat}\} = \min\{2{,}1; 2{,}5; 0{,}63\} = 0{,}63 \Big/ = k_n'\left(\frac{W_n}{L_n}\right)\left\{(V_{gs}-V_{Tn})V_{min} - \frac{V_{min}^2}{2}\right\} =$

$= 115 \cdot 10^{-6}\,\frac{0{,}375}{0{,}25}\left[(2{,}5-0{,}4)0{,}63 - \frac{0{,}63^2}{2}\right] = 0{,}194\,mA$

$I_d(V_{out}=V_{DD}/2) = \Big/ V_{min} = \min\{2{,}1; 1{,}25; 0{,}63\} = 0{,}63 \Big/ = 0{,}194\,mA$

$\Rightarrow t_{PHL} = \dfrac{1{,}25 \cdot 6{,}5 \cdot 10^{-15}}{0{,}194 \cdot 10^{-3}} = \underline{\underline{41{,}9\,ps}}$

5.10 continued

d) Find (W_p/W_n) such that $t_{pHL} = t_{pLH}$

$t_{pHL} = t_{pLH} \iff I_{avg,charge} = I_{avg,discharge}$

$I_{d,vel.sat\,p} = I_{d,vel.sat\,n}$ (see equations from c))

$$k_p' \left(\frac{W_p}{L_p}\right)\left[(V_{sg}-|V_{tp}|)V_{dsat\,p} - \frac{V_{dsat\,p}^2}{2}\right] = k_n' \frac{W_n}{L_n}\left[(V_{gs}-V_{tn})V_{dsat\,n} - \frac{V_{dsat\,n}^2}{2}\right]$$

$$30 \frac{W_p}{0,25\mu m}\left[(2,5-0,4)\cdot 1 - \frac{1^2}{2}\right] = 115 \frac{W_n}{0,25\mu m}\left[(2,5-0,4)\cdot 0,63 - \frac{0,63^2}{2}\right]$$

$$\frac{W_p}{W_n} = \frac{115\left[(2,5-0,4)\cdot 0,63 - \frac{0,63^2}{2}\right]}{30\left[(2,5-0,4)\cdot 1 - \frac{1^2}{2}\right]} = 2,694\ldots \approx 2,7$$

e) Suppose we increase the width of the transistors to reduce the t_{pHL}, t_{pLH}. Do we get a proportional decrease in delay times? Justify your answer.

The propagation delays <u>Do NOT</u> decrease in proportion to the widths because of self loading effects. As the device size increases, its parasitic capacitances increase as well. In this problem, increasing device sizes increases both average current and C_{Leff}.

f) Suppose $V_{SB} = 1V$; what is the value of V_{tn}, V_{tp}, V_M? How does this qualitatively affect C_{Leff}?

$V_{tp} = V_{tp0} = -0,4V$ (No body effect according to the figure)

$V_{tn} = V_{tn0} + \gamma\left(\sqrt{V_{SB}+|2\phi_F|} - \sqrt{|2\phi_F|}\right) = 0,4 + 0,4\left(\sqrt{1+0,6} - \sqrt{0,6}\right) =$

$= 0,596V$

V_M: $I_{dn} = I_{dp}$

$$k_n' \frac{W_n}{L_n}\left[(V_M - V_{tn})V_{dsat} - \frac{V_{dsat}^2}{2}\right] = \frac{k_p'}{2}\frac{W_p}{L_p}\left(V_{dd} - V_M - |V_{tp}|\right)^2$$

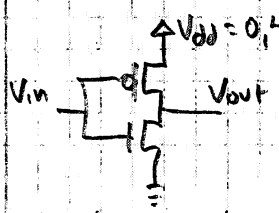
$$115 \frac{0,375}{0,25}\left[(V_M - 0,596)0,63 - \frac{0,63^2}{2}\right] = \frac{30}{2}\frac{1,25}{0,25}\left(2,5 - V_M - 0,4\right)^2$$

Graphical solution on HP48:

$\Rightarrow V_M = 1,325V$

5.14

The inverter below operates with $V_{DD} = 0,4V$ and is composed of $|V_t| = 0,5V$ devices. The devices have identical I_0 and n. ($n = 1,5$)



Inverter in weak inversion regime

a) Calculate the switching threshold (V_M) of this inverter

$$I_d = I_0 e^{\left(\frac{V_{gs}}{nkT/q}\right)}\left[1 - e^{\left(\frac{-V_{ds}}{kT/q}\right)}\right](1+\lambda V_{ds}) \qquad (p.99;\ Eq.\ 3.39)$$

$\frac{kT}{q} \approx 26mV$ @ room temperature

Assume $V_{ds} > 50mV \Rightarrow 1 - e^{-V_{ds}/(kT/q)} \approx 1$

$$\Rightarrow I_d \propto I_0 e^{\frac{V_{gs}}{nkT/q}}(1+\lambda V_{ds})$$

$V_{in} = V_{out} = V_M$ and $I_{dn} = I_{dp}$

$$\Rightarrow \cancel{I_0} e^{\left(\frac{V_M}{nkT/q}\right)}(1+\lambda_n V_M) = \cancel{I_0} e^{\left(\frac{V_{DD}-V_M}{nkT/q}\right)}(1+\lambda_p(V_{DD}-V_M))$$

$$\frac{1+\lambda_n V_M}{1+\lambda_p(V_{DD}-V_M)} = e^{\left(\frac{V_{DD}-2V_M}{nkT/q}\right)}$$

$$\ln\left\{\frac{1+\lambda_n V_M}{1+\lambda_p(V_{DD}-V_M)}\right\} = \frac{V_{DD}-2V_M}{nkT/q}$$

$\left[\begin{array}{l} V_{DD} = 0,4V \\ kT/q = 26mV \\ \lambda_n = 0,6V^{-1} \\ \lambda_p = 1V^{-1} \\ n = 1,5 \end{array}\right]$

$$\frac{0,4-2V_M}{0,026} - \ln\left\{\frac{1+0,6\cdot V_M}{1+0,4-V_M}\right\} = 0$$

Graphical solution on HP48 :

$$\Rightarrow V_M = 0,20088\ldots \approx \underline{\underline{0,2V}}$$

5.14 Continued...

b) Calculate V_{IL} and V_{IH} of the inverter

To calculate V_{IL} and V_{IH} we need to calculate the slope of the VTC at $V_M = V_{DD}/2$

Equating the currents we get:

$$I_0 e^{\left(\frac{V_{in}}{nkT/q}\right)}(1+\lambda_n V_{out}) = I_0 e^{\left(\frac{V_{DD}-V_{in}}{nkT/q}\right)}(1+\lambda_p(V_{DD}-V_{out}))$$

Differentiate both sides with respect to V_{in}:

$$\frac{\partial}{\partial V_{in}}\left[e^{\left(\frac{V_{in}}{nkT/q}\right)}(1+\lambda_n V_{out})\right] = \frac{\partial}{\partial V_{in}}\left[e^{\frac{V_{DD}-V_{in}}{nkT/q}}(1+(V_{DD}-V_{out})\lambda_p)\right]$$

$$\frac{1}{nkT/q} e^{\left(\frac{V_{in}}{nkT/q}\right)}(1+\lambda_n V_{out}) + e^{\frac{V_{in}}{nkT/q}}\cdot\lambda_n\cdot\frac{\partial V_{out}}{\partial V_{in}} =$$

$$= -\frac{e^{\left(\frac{V_{DD}-V_{in}}{nkT/q}\right)}(1+\lambda_p(V_{DD}-V_{out}))}{nkT/q} - e^{\left(\frac{V_{DD}-V_{in}}{nkT/q}\right)}\lambda_p\frac{\partial V_{out}}{\partial V_{in}}$$

e^{2x}

$2e^{2x}$

$$\left[\lambda_p e^{\left(\frac{V_{DD}-V_{in}}{nkT/q}\right)} + \lambda_n e^{\frac{V_{in}}{nkT/q}}\right]\frac{\partial V_{out}}{\partial V_{in}} = -\frac{e^{\left(\frac{V_{DD}-V_{in}}{nkT/q}\right)}(1+\lambda_p(V_{DD}-V_{out})) + e^{\left(\frac{V_{in}}{nkT/q}\right)}(1+\lambda_n V_{out})}{nkT/q}$$

Insert $V_{out} = V_{in} = V_{DD}/2$:

$$e^{\left(\frac{V_{DD}/2}{nkT/q}\right)}(\lambda_p+\lambda_n)\frac{\partial V_{out}}{\partial V_{in}} = -\frac{e^{\frac{V_{DD}/2}{nkT/q}}(1+\lambda_p V_{DD}/2) + e^{\frac{V_{DD}/2}{nkT/q}}(1+\lambda_n V_{DD}/2)}{nkT/q}$$

$$\left.\frac{\partial V_{out}}{\partial V_{in}}\right|_{V_{in}=V_{DD}/2} = -\frac{2+(V_{DD}/2)(\lambda_n+\lambda_p)}{\frac{nkT}{q}(\lambda_p+\lambda_n)}$$

$V_{DD} = 0{,}4\,V$
$kT/q = 26\,mV$
$\lambda_n = 0{,}06\,V^{-1}$
$\lambda_p = 0{,}1\,V^{-1}$
$n = 1{,}5$

$$g \equiv \frac{\partial V_{out}}{\partial V_{in}} = \frac{-(2+0{,}2\cdot 0{,}16)}{1{,}5\cdot 0{,}026\cdot 0{,}16} = -325{,}6$$

This value is much larger than we would expect from a CMOS inverter (which typically has $g \sim -30$). However, we should keep in mind that in the subthreshold regime MOS devices behave essentially as bipolar devices and can yield such values of gain

(5.14) continued

b) We know that $V_{IL} = V_M + \frac{V_{DD} - V_M}{9}$

$$V_{IH} = V_M - \frac{V_M}{9}$$

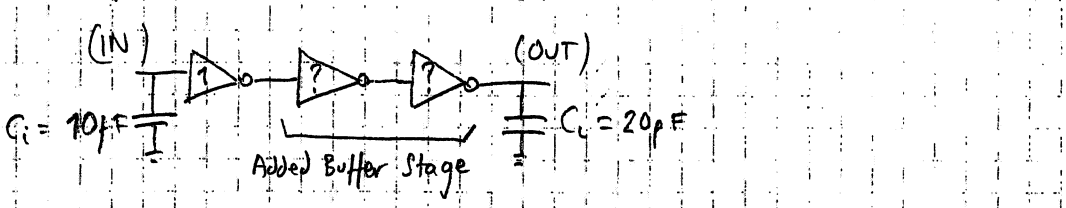
$$\Rightarrow V_{IL} = 0,2 + \frac{0,4 - 0,2}{-325,6} = \underline{\underline{0,1994\,V}}$$

$$V_{IH} = 0,2 - \frac{0,2}{-325,6} = \underline{\underline{0,2006\,V}}$$

(Also $NM_H = NM_L = 0,1994\,V$)

5.15 SIZING A CHAIN OF INVERTERS

a) In order to drive a large capacitance ($C_L = 20pF$) from a minimum size gate (with input capacitance $C_i = 10fF$), you decide to introduce a TWO-STAGED buffer as shown in Fig. 5.12. Assume that the propagation delay of a minimum size inverter is 70ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.



Size for minimum delay.

Minimum delay occurs when the delay through each buffer is the same. This can be achieved by sizing the buffer as f, f^2, respectively

where $f = \sqrt[N]{C_L/C_{in}} = \Big/$ N = Total inverters in the buffer $\Big/ = \sqrt[3]{\frac{20000}{10}} \simeq 12,6$

$t_p = N \cdot t_{p0}(1 + f/\gamma)$ where $t_{p0} = 70ps$; $\gamma = 1$ for most submicron processes

$t_p = 3 \cdot 70 \cdot 10^{-12}(1 + 12,6) = 2,18558\ldots ns \simeq \underline{\underline{2,86ns}}$

5.15 b) $t_p = N t_{p0} \cdot (1 + \sqrt[N]{F}/\gamma) = N \cdot t_{p0}(1 + f/\gamma)$

$f = \sqrt[N]{F}$

$\frac{\partial t_p}{\partial N} = 0 \Rightarrow \gamma + \sqrt[N]{F} - \frac{\sqrt[N]{F} \ln F}{N} = 0$

$\Rightarrow f = e^{(1+\gamma/f)}$

$\gamma = 1 \Rightarrow f_{opt} = 3,6$

$f_{opt} \approx 3,6 \Rightarrow N_{opt} = \frac{\ln F}{\ln f} = \frac{\ln 2000}{\ln 3,6} = 5,93\ldots \approx 6$

$\Rightarrow t_{pmin} = N_{opt} \cdot t_{p0} \cdot (1 + f_{opt}/\gamma) = \ldots$

$= 6 \cdot 270ps \cdot (1 + 3,6/1) = 1,932\,ns \approx \underline{1,93\,ns}$

PP. 207-209

5.15 continued...

c) Describe the advantages and disadvantages of the methods shown in a) and b).

Solution b) is faster but consumes much more area than solution a).

d) Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2,5V and an activity factor of 1?

The power consumption is determined as follows:

$$P = \frac{1}{T} C_{tot} \Delta V V_{DD} \alpha = \left| \begin{array}{l} \Delta V = \text{voltage swing} \\ = V_{DD} \end{array} \right| = \alpha \frac{1}{T} C_{tot} V_{DD}^2$$

$$V_{DD} = 2,5 \; ; \; \alpha = 1 \; , \; C_{tot} = C_{in} + C_{in} f + C_{in} f^2 + C_{in} f^3 =$$

$$= C_{in} \sum_{k=0}^{3} f^k = C_{in} \frac{f^4 - 1}{f - 1}$$

$$\Rightarrow P = 1 \cdot \frac{1}{T} \cdot C_{in} \left[\frac{f^4 - 1}{f - 1} \right] V_{DD}^2 = 1 \cdot \frac{1}{T} \cdot 10 \cdot 10^{-15} \left[\frac{12,6^4 - 1}{12,6 - 1} \right] 2,5^2 =$$

$$= \underline{\underline{135,8 \left(\frac{1}{T} \right) pW}}$$

5.16 Consider scaling a CMOS technology by $S > 1$. In order to maintain compatibility with existing system components, you decide to use constant voltage scaling.

a) In traditional constant voltage scaling, transistor widths scale inversely with S, $W \propto 1/S$. To avoid the power increase associated with constant voltage scaling, however, you decide to change the scaling factor for W. What should this new scaling factor be to maintain approximately constant power? Assume long-channel devices (i.e. neglect velocity saturation)

We know that $P \propto f C V_{DD}^2$ and $f \propto \frac{1}{t_p}$

$I = \frac{\Delta Q}{\Delta t}$, $C = \frac{\Delta Q}{\Delta V}$, $\Delta Q = C\Delta V$ $\Big\}$ $I = \frac{C\Delta V}{\Delta t} \Leftrightarrow \frac{1}{t_p} = \frac{I_{dsat}}{C V_{DD}}$

$\Rightarrow P \propto \frac{I_{dsat}}{C \cdot V_{DD}} \cdot C V_{DD} = I_{dsat} \cdot V_{DD} \propto k' \frac{W}{L} (V_{DD} - V_T)^2 V_{DD}$

textbook p. 124 $L \propto 1/S$; $k' \propto S$; $V_T \propto 1$ for constant voltage scale

$P \propto S \cdot \frac{W}{(\frac{1}{S})} = S^2 \cdot W$

To make $P \propto 1$, we must scale W by $\underline{\underline{1/S^2}}$

b) How does delay scale under this new methodology?

$t_p \propto \frac{C V_{DD}}{I_{dsat}} = \frac{C V_{DD}}{k'(\frac{W}{L}) V_{DD}} \propto \frac{W \cdot L \cdot \frac{\varepsilon}{t_{ox}}}{k'(\frac{W}{L}) V_{DD}} \propto \frac{\frac{1}{S^2} \cdot \frac{1}{S} \cdot \frac{1}{(1/S)}}{S \cdot \frac{1}{S^2} \cdot \frac{1}{(1/S)}} = \underline{\underline{\frac{1}{S^2}}}$

c) Assuming short-channel devices (i.e. velocity saturation), how would transistor widths have to scale to maintain the constant power requirement?

text book p. 124

$P \propto I_{dvelsat} V_{DD} \propto C_{ox} W (V_{gs} - V_T) V_{DD} \propto S \cdot W \cdot 1 \cdot 1$

So to maintain constant power, W has to scale as $1/S$ (same as standard constant voltage scaling)