

TSEI03 Homework 2: Solution

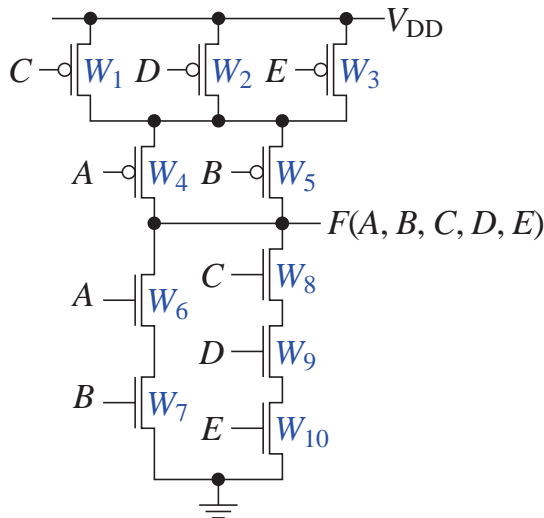
Identify logic function from gate schematic

$$F(A, B, C, D, E) = \overline{\overline{\overline{A \cdot B}} + \overline{\overline{\overline{C \cdot D}} + E}} = \overline{A \cdot B + C \cdot D \cdot E}$$

Switch nets

$$\begin{cases} S_p = F(\overline{A}, \overline{B}, \overline{C}, \overline{D}, \overline{E}) = \overline{\overline{\overline{A \cdot B + C \cdot D \cdot E}}} = (A + B)(C + D + E) \\ S_n = \overline{F(A, B, C, D, E)} = \overline{\overline{\overline{A \cdot B + C \cdot D \cdot E}}} = A \cdot B + C \cdot D \cdot E \end{cases}$$

Transistor schematic with annotated widths, W_k



Select all channel lengths to minimum, L_{\min} , and express the widths in units of L_{\min} . Worst case resistance occurs when a single path conducts. Design the widths of a single conduction path to be equal. Using $R \propto 1/W$, we should design the six pull-up paths to have an equivalent resistance of $W_p = 5L_{\min}$:

$$\begin{cases} W_1^{-1} + W_4^{-1} = (5L_{\min})^{-1} \\ W_1^{-1} + W_5^{-1} = (5L_{\min})^{-1} \\ W_2^{-1} + W_4^{-1} = (5L_{\min})^{-1} \\ W_2^{-1} + W_5^{-1} = (5L_{\min})^{-1} \\ W_3^{-1} + W_4^{-1} = (5L_{\min})^{-1} \\ W_3^{-1} + W_5^{-1} = (5L_{\min})^{-1} \end{cases} \xrightarrow{\text{equal widths in path}} \begin{cases} W_1 = W_4 = 10L_{\min} \\ W_1 = W_5 = 10L_{\min} \\ W_2 = W_4 = 10L_{\min} \\ W_2 = W_5 = 10L_{\min} \\ W_3 = W_4 = 10L_{\min} \\ W_3 = W_5 = 10L_{\min} \end{cases}$$

Design the two pull-down paths to have an equivalent resistance of $W_n = 1.5L_{\min}$:

$$\begin{cases} W_6^{-1} + W_7^{-1} = (1.5L_{\min})^{-1} \\ W_8^{-1} + W_9^{-1} + W_{10}^{-1} = (1.5L_{\min})^{-1} \end{cases} \xrightarrow{\text{equal widths in path}} \begin{cases} W_6 = W_7 = 3L_{\min} \\ W_8 = W_9 = W_{10} = 4.5L_{\min} \end{cases}$$

Hence $W_1 = W_2 = W_3 = W_4 = W_5 = 10L_{\min}$, $W_6 = W_7 = 3L_{\min}$, and $W_8 = W_9 = W_{10} = 4.5L_{\min}$.