TSEI03 Homework 3: Dynamic logic

A layout of a dynamic gate is shown in Figure 1. The spacing of the grid is 0.25 µm. For metal wires, area capacitance is 35 aF/µm^2 and fringing capacitance is 55 aF/µm. For polysilicon wires, area capacitance is 75 aF/µm^2 and fringing capacitance is 40 aF/µm. Use transistor parameters according to the formulas in the Problems & Solution manual. Neglect gate overlap and capacitance due to contacts in calculations.

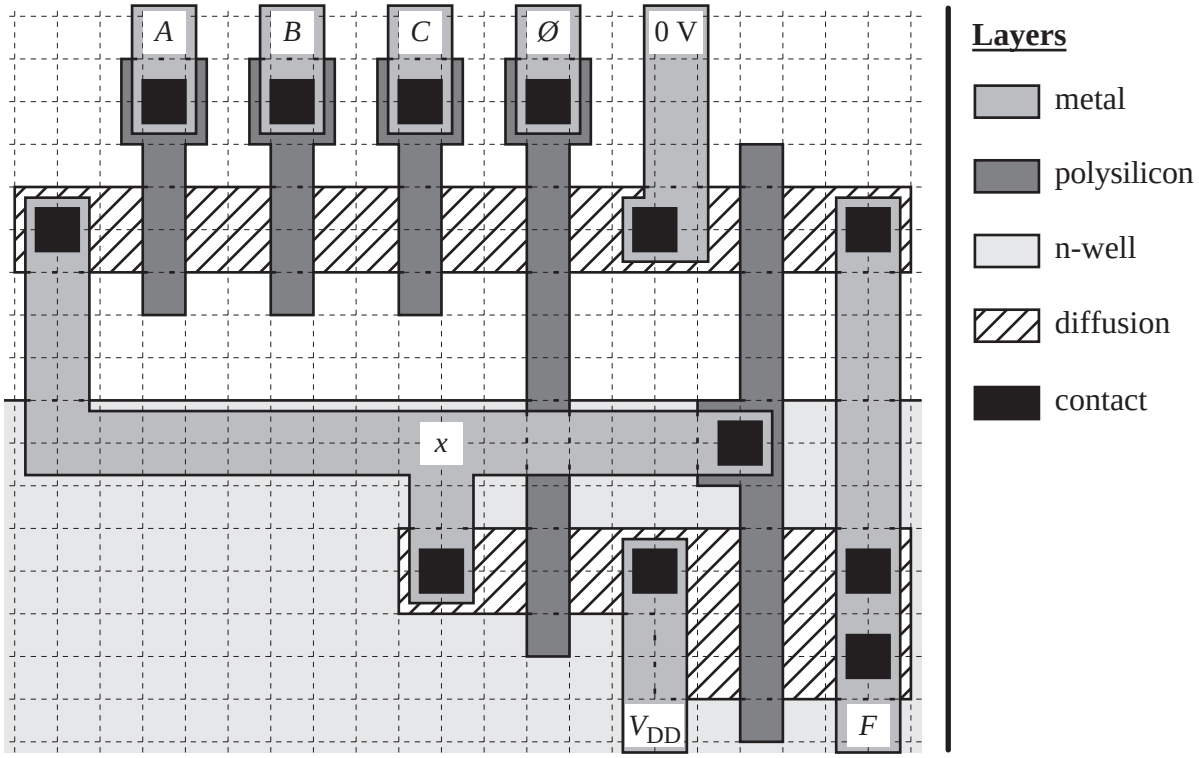

Figure 1. Dynamic gate layout.

a) What function $F(A, B, C)$ has been implemented?

b) Estimate the worst-case parasitic capacitance of the internal node x.

c) What input combination causes the largest problem with charge sharing?