TSEI03 Homework 2: Static CMOS design

A logic function is defined by the gate schematic shown in Figure 1.

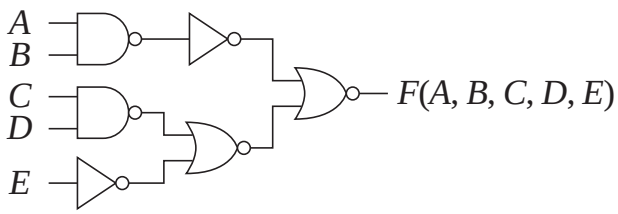

Figure 1. Logic design.

Implement the function $F(A, B, C, D, E)$ as one static CMOS gate. Assume that only non-inverted input signals are available and that maximum 10 transistors can be used. Size all the devices in your completed static CMOS gate so that the worst case output resistance is the same as that of an inverter with $W_n/L_n = 1.5$ and $W_p/L_p = 5$. Clearly explain and motivate your sizing strategy.