Digital ICs — Lectures

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2) **Devices** [Ch. 3, 4]	*TSEI03/TSTE86*
3) **Interconnect** [Ch. 4, 9]	*TSTE86*
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10) **Memory** [Ch. 12]	*TSEI03/TSTE86*
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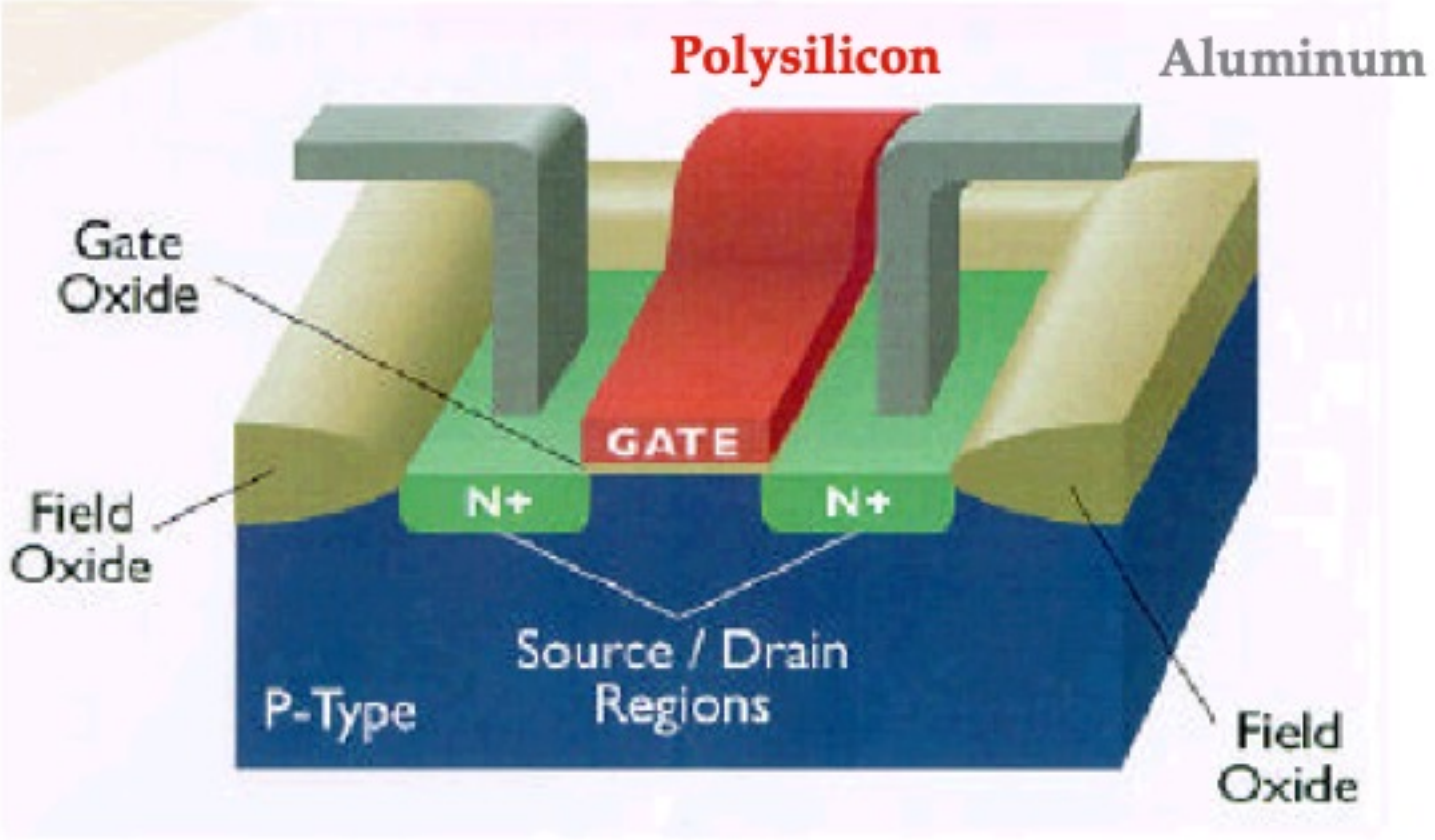
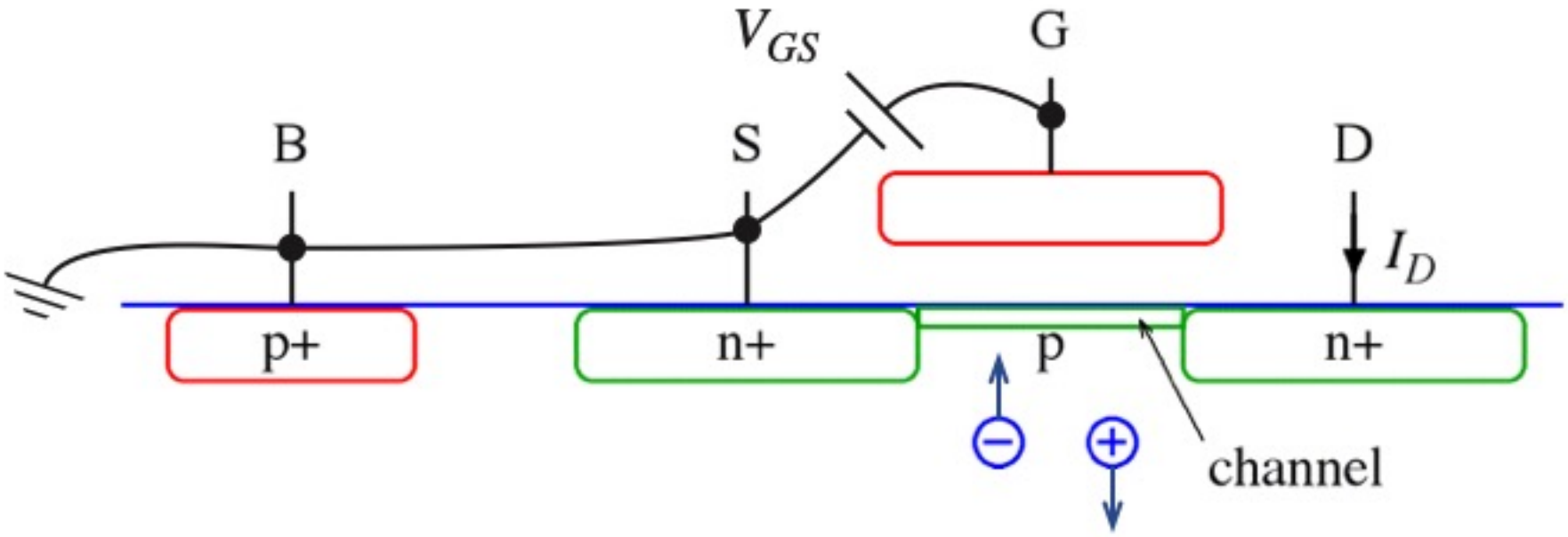
12) **System design** [Ch. 8]	*TSTE86*

MOSFET

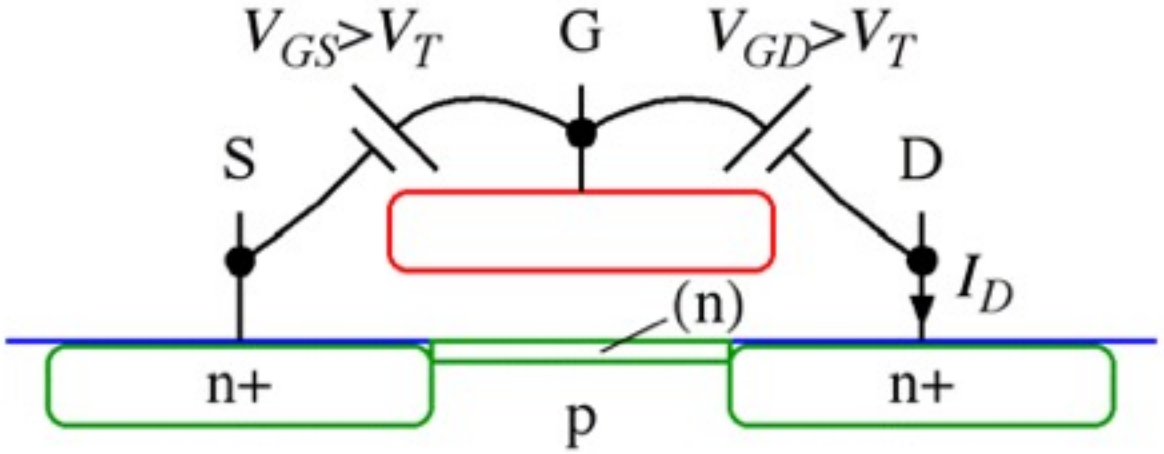

Polysilicon
Aluminum
Gate Oxide
GATE
N+
N+
Field Oxide
Source / Drain Regions
P-Type
Field Oxide

MOSFET Operation



Cut-off region: $V_{GS} \le V_T$ Current: $I_D = 0$

Resistive (or Linear) Region

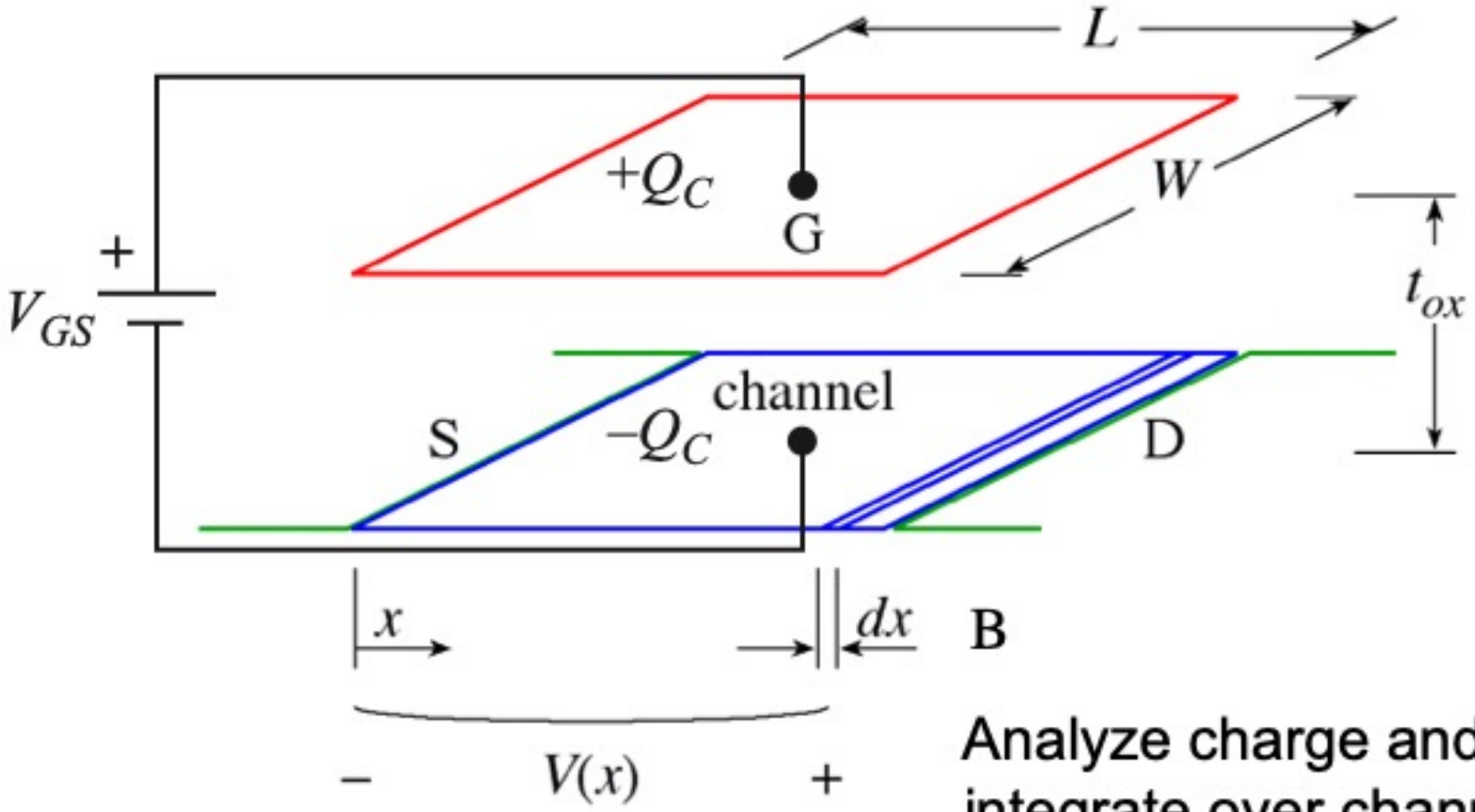


Conduction: $V_{GS} > V_T$

Resistive region: $V_{GD} > V_T \Rightarrow V_{GS} - V_{DS} > V_T$

$$\Rightarrow V_{DS} < V_{GS} - V_T = V_{GT}$$

Resistive Operation



Analyze charge and integrate over channel

Resistive Current

Current: $$I_D = k' \frac{W}{L}\left(V_{GT}V_{DS} - \frac{1}{2}V_{DS}^2\right)$$

where

k' is the process transconductance

Threshold Voltage

$$V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\phi_F|} - \sqrt{|2\phi_F|}\right)$$

where

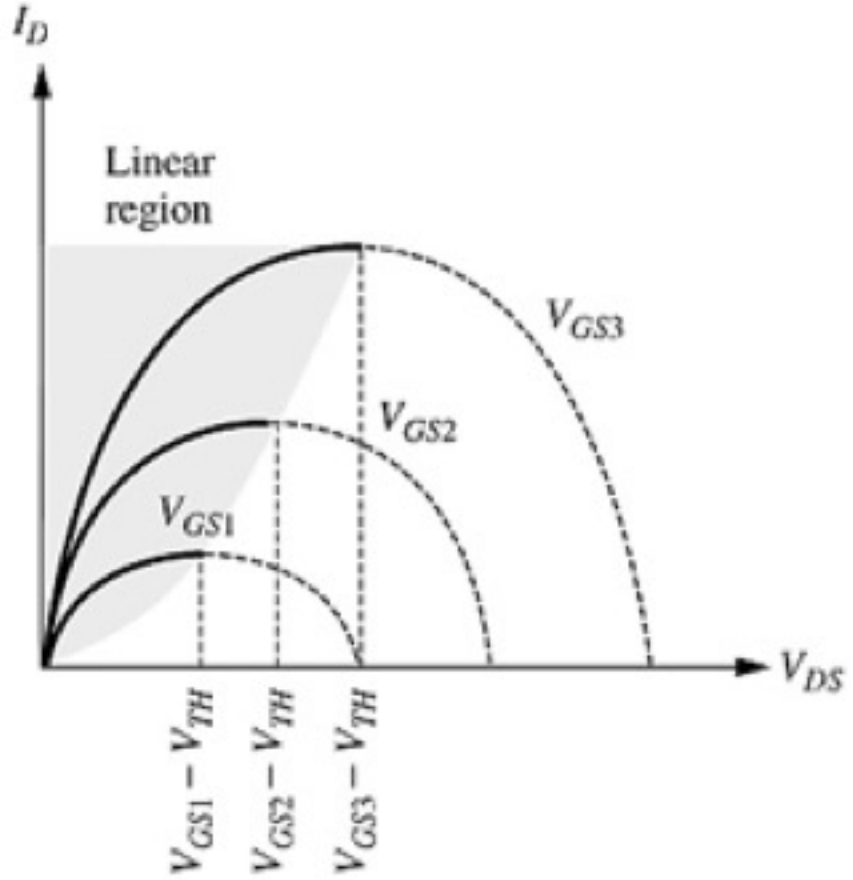
V_T is the threshold voltage

V_{T0} is V_T at $V_{SB} = 0$

γ is the body-effect coefficient

ϕ_F is the Fermi potential

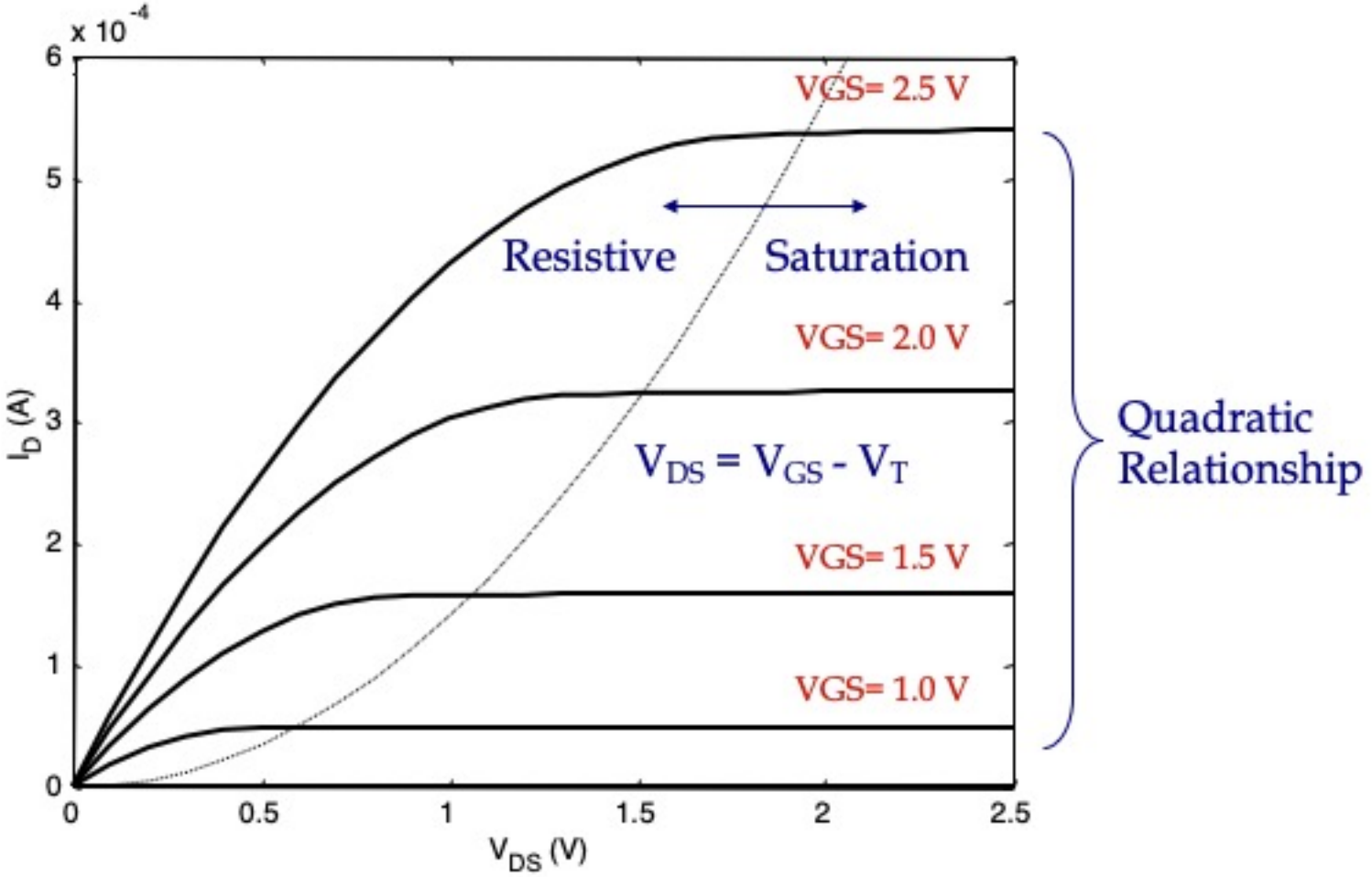
I(V) Plot of Resistive MOSFET



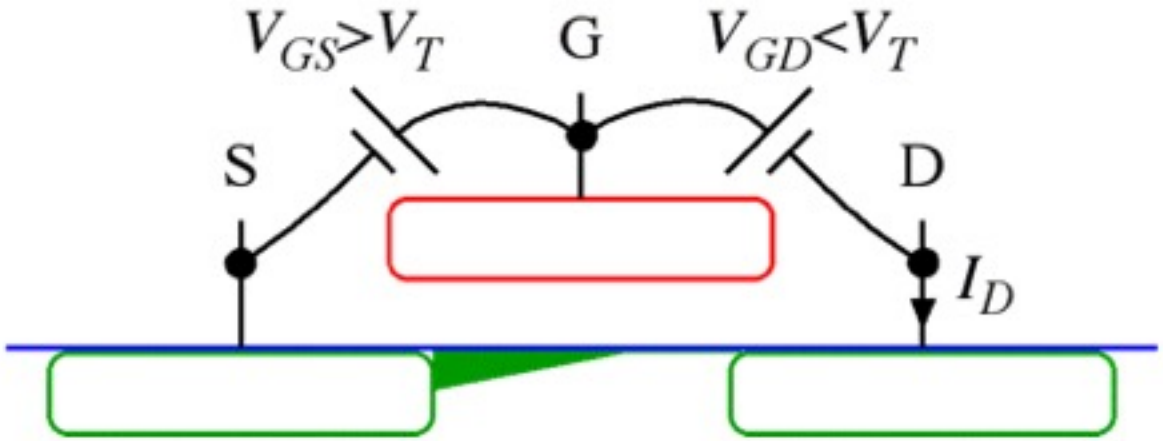
What happens to the right of the resistive region?

$$V_{GD} \leq V_T !$$

I(V) Relations

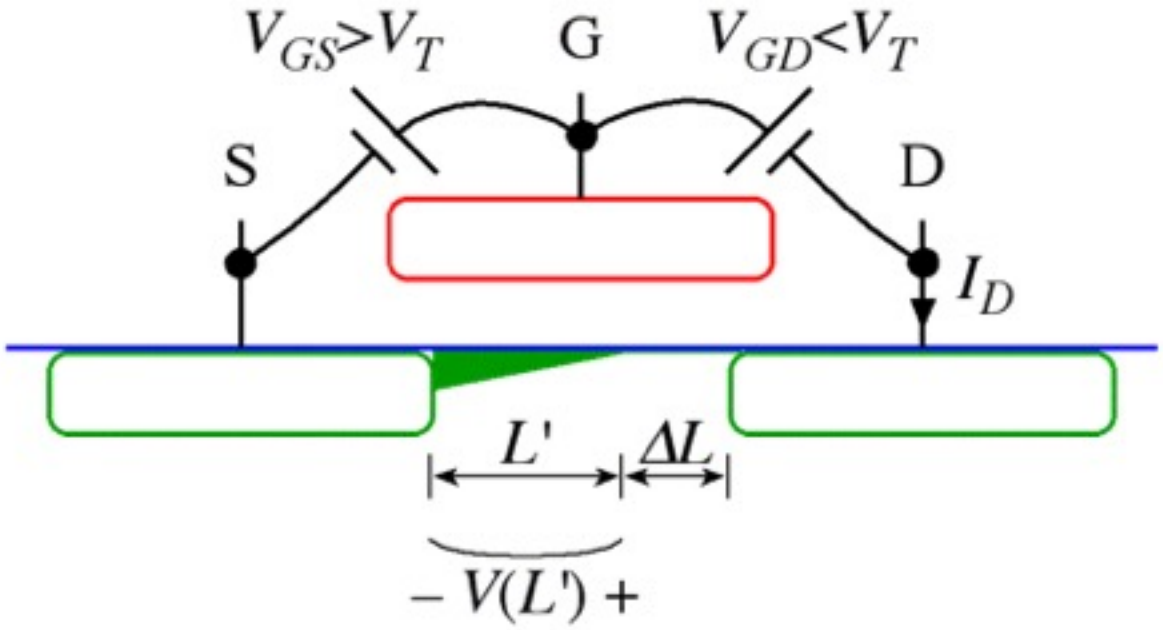


Saturation Condition



Saturation region: $V_{GS} > V_T, V_{DS} > V_{GS} - V_T = V_{GT}$

Saturation Operation



Channel is pinched off at $L' \Rightarrow V(L') = V_{GS} - V_T = V_{GT}$

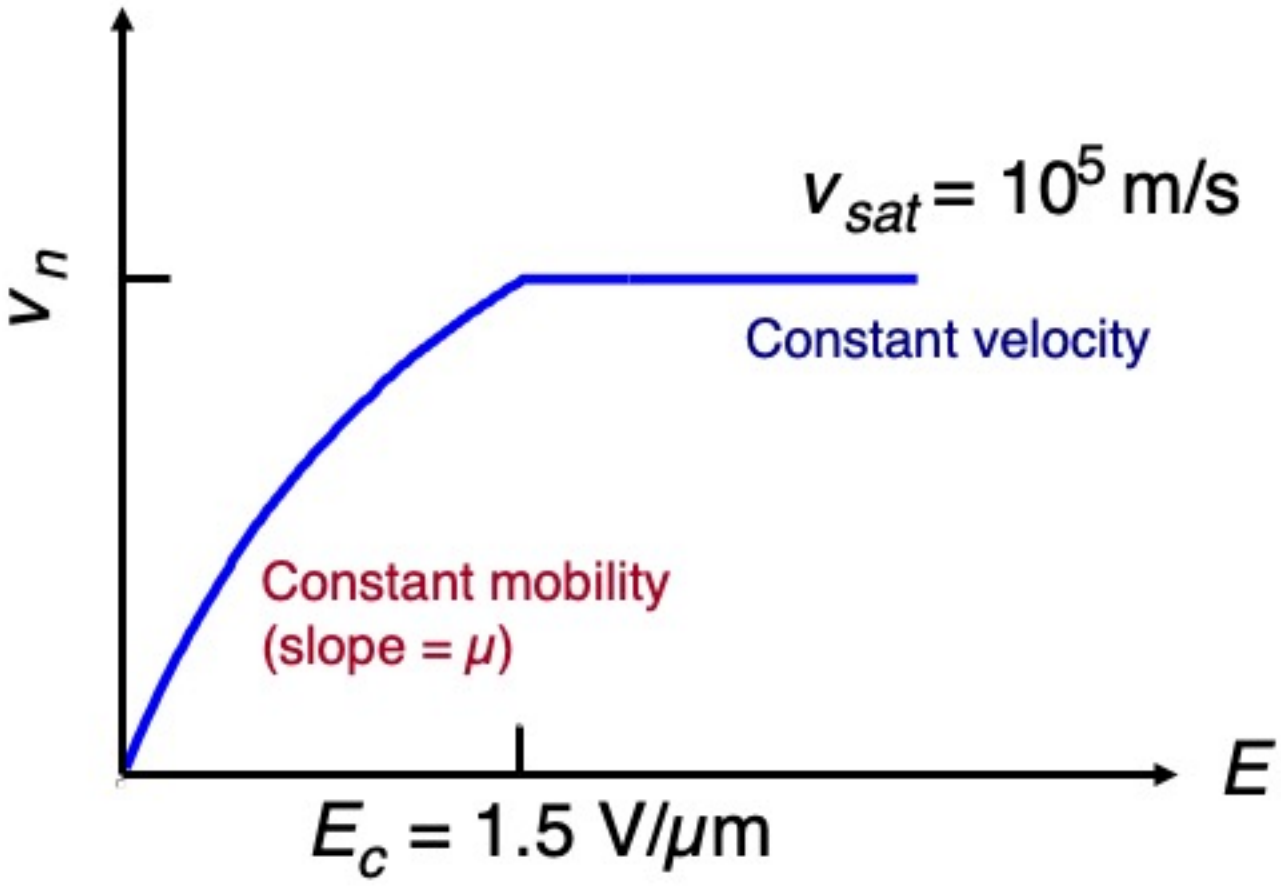
Saturation Current

Current: $$I_D = k' \frac{W}{L} \frac{V_{GT}^2}{2} (1 + \lambda V_{DS})$$

where

λ is the channel-length modulation

Velocity Saturation



Velocity Saturation Current

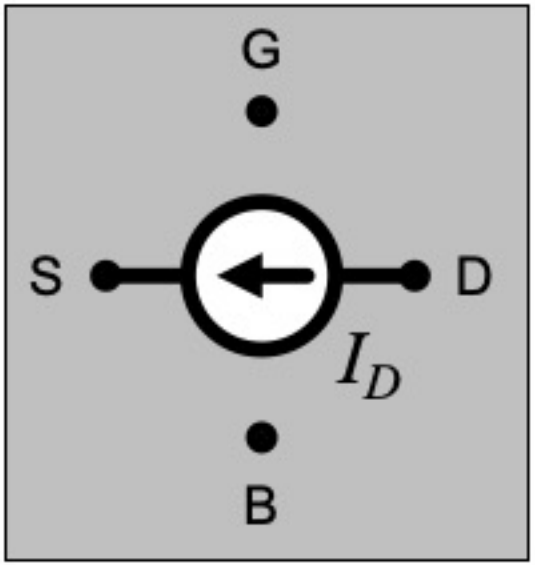
Velocity saturation region: $V_{GS} > V_T, V_{DS} > V_{DSAT}$

Current: $$I_D = k' \frac{W}{L}\left(V_{GT}V_{DSAT} - \frac{1}{2}V_{DSAT}^2\right)$$

where

V_{DSAT} is the V_{DS} at which velocity saturation occurs

Unified Model for Manual Analysis



$$I_D = 0 \text{ for } V_{GT} \le 0$$

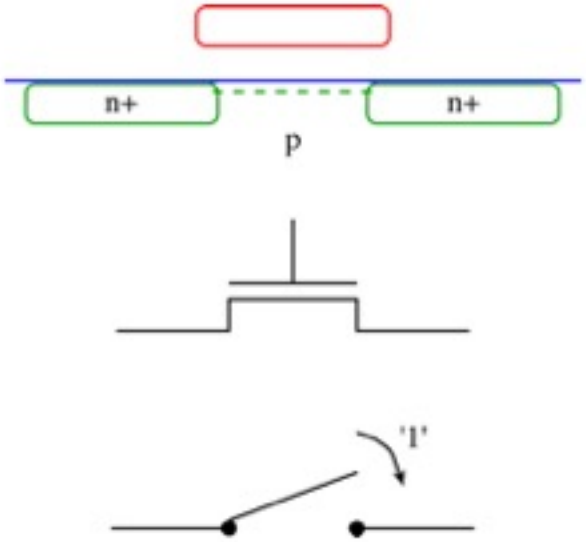
$$I_D = k' \frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{DS}) \text{ for } V_{GT} \ge 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

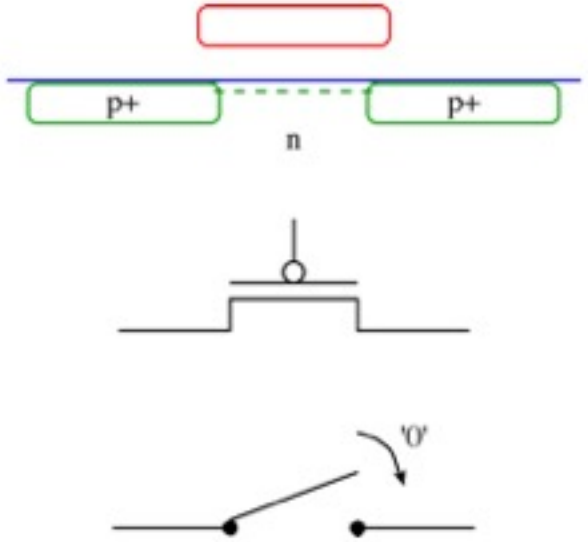
$V_{GT} = V_{GS} - V_T$,

and $V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$

Complementary MOS (CMOS)



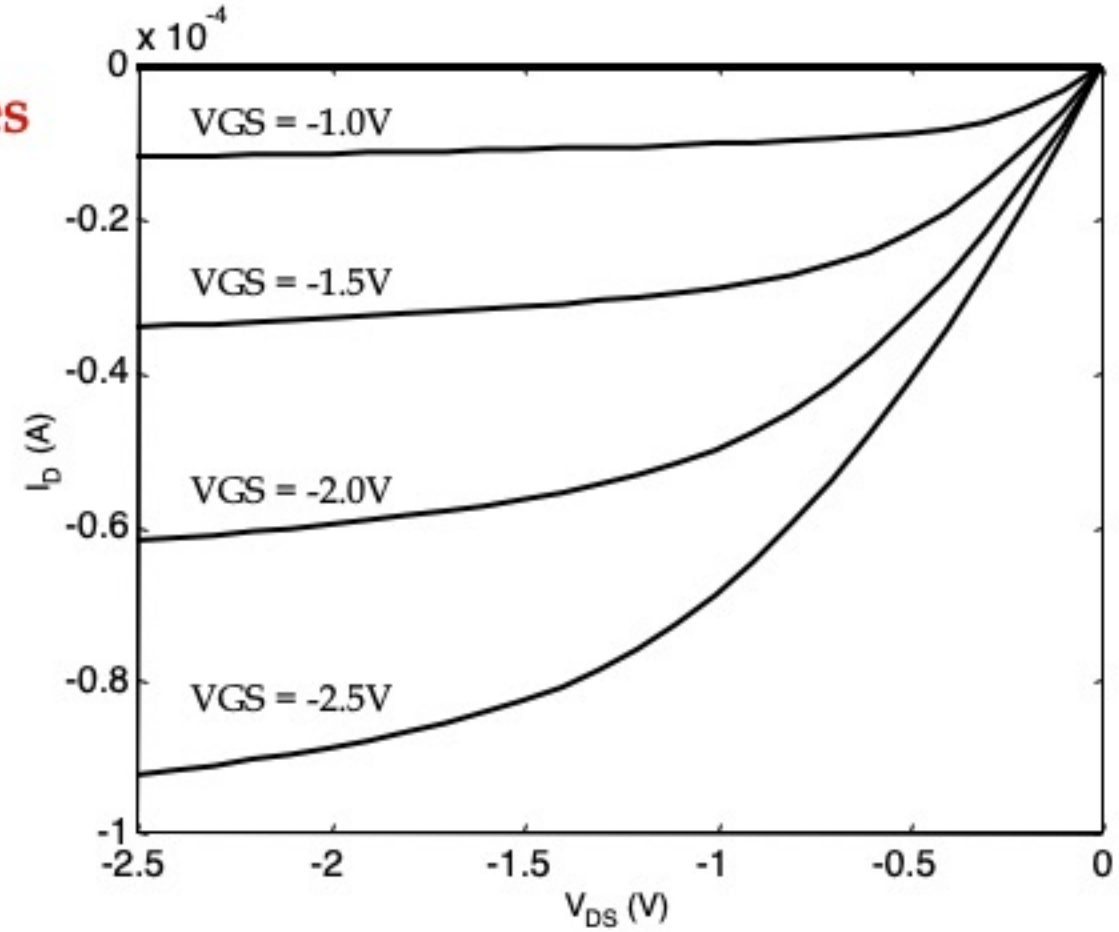
NMOSFET



PMOSFET

PMOSFET

Assume all variables negative



Process Parameters

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	K' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1