Master thesis - Timing Accuracy and Simulation Speed in a Manycore Processor Simulation

Background
Ericsson develops simulators, referred to as virtual platforms, for its many-core processor architecture. The virtual platforms are used for software development prior to the availability of hardware, for the purpose of gaining time-to-market, but also in software regression testing after hardware is available.

Thesis Description
The processor models used in the virtual platforms are instruction accurate, but they also model timing. We have seen that there is an interplay between enhancing the timing modeling in the processor models, and the resulting behavior of software that runs on the virtual platform. In most cases, an enhanced timing model enables more software test cases to pass. In other cases, it is difficult to find the proper amount of timing modeling.

When adding timing, there is also a penalty, in the form of increased execution time for the virtual platform. In this master thesis, the goal is to investigate and optimize the trade-off between timing modeling and execution time, for a selected set of software test cases. Based on a description of timing modeling techniques used in the virtual platform, the work shall explore how adding or removing timing modeling affects the software. As a secondary effect, we expect that this investigation will lead to new insights on how to modify the software itself, so that it is less sensitive to timing, and hence can take advantage of a less timing-accurate, but faster, virtual platform.

Qualifications
The candidate for this work should be interested in computer architecture and processor instruction sets. In addition, you should be familiar with embedded systems and low-level software development, such as assembly programming and C programming. Knowledge of concurrent programming and real-time operating systems is also important.

Extent
1-2 students, 30hp each

Location
Ericsson AB Kista, Stockholm

Preferred Starting Date
Spring 2019

Keywords
Computer architecture, processor models, simulation timing, simulation performance, low-level programming, concurrent programming, real-time operating systems

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