Master Thesis – Performance Investigation of Access Types to IQC Device

Background
Performance comparison between APB and AHB access to IQC Device Processor packet TX and RX memories including transmitting packets between those using the IQ Control, IQC, packet switch.

The thesis consists of two parts, a design part and a performance investigation part, which are dependent on each other.

Thesis Description
Design:
- Exchange the present APB/MIRI interface to IQC packet RX and TX memories to AHB interface.
- This would include prestudy of how the AHB shall connect to the IQC DP packet memories. And how to implement the AHB.

Performance tests:
- Develop performance tests for IQC packet transmission from one processor to another using the IQC DP packet memories.
- These performance test would include latency and throughput for different size packets.
- A comparison would then be made between the present APB/MIRI solution and the new AHB connection.
- This also would include a prestudy of how to implement and visualize the performance in a graphical quick and easy to understand way using the existing SystemVerilog UVM verification environment.
- To analyze how the performance scales with a greater number of device processors, DP, functions with same AHB interface connecting multiple DP RX ports (if it gets better or worsens or no change)
- This will help identify if single AHB port is enough or we need to add extra AHB port when we have more DP functions or more DPs.

Reliability:
- Packet loss and packet bit errors should be measured.

Implementation size and timing:
- Comparison between the APB MIRI and the AHB interface design.

Contact Persons
Contact Person
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Qualifications
This project aims at students in MSc, or WWW, TTT or similar.

Extent
1-2 students, 30hp each

Location
Ericsson AB, Kista

Preferred Starting Date
Spring 2021

Keywords
C/C++, SystemVerilog, ASIC, synthesis, Mobile Telecommunication, Optimization, Air Interfaces, Coding Schemes

Contact Persons
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