Master Thesis – PTP PHY Adaptation

Background
In 5G networks there will an even greater demand for fast and accurate synchronization compared to previous generations. This push for synchronization in both fronthaul and backhaul will be implemented using 1588, PTP, over Ethernet packet based synchronization. For short haul and moderate speed ethernet can operate over standard twisted copper cables. This calls for ASIC external Phy devices, these devices need to be PTP aware and perform high precision timestamping. These Phy devices usually implements custom synchronization schemes for synchronization of its timestamping engine in addition to device specific PTP timestamp handling. To allow Ericsson ASIC’s to leverage future standard updates and enhancements in newer Phy devices, a general Phy adaptation scheme is needed.

Thesis Description
This thesis is divided into several steps

The following steps are envisioned as part of the thesis work:

- Investigate current synchronization and PTP handling of market leading Phy devices
- Implement and general PTP interface block in FPGA
- Analyze cost benefits with a general-purpose implementation

The thesis will be concluded with a result presentation for the Ericsson Digital Asic team.

Qualifications
This project aims at students in electrical engineering, computer science, computer engineering or similar.

Extent
1-2 students, 30hp each

Location
Ericsson AB, Kista

Preferred Starting Date
Spring 2019

Keywords
High Speed Serial link, 5G, SGMII, UXGMII, PTP, Synchronization, SERDES

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