Master Thesis – Multithreaded Simulation of Manycore Systems

Background

Ericsson develops simulators, referred to as virtual platforms, for accelerating software development prior to availability of hardware. The virtual platforms contain models for processors, ASIC components, and board components, for digital parts of Ericsson Radio Systems. The simulation models, for baseband processing as well as for radio processing, are implemented in C and C++, using SystemC and TLM. The simulated system is highly parallel, with software executing concurrently on processors, and with communication between processors as well as with entities outside of the simulated system.

The SystemC simulation environment provides support for concurrent activities. However, the support for scheduling these activities on multiple cores is limited. As a result, the simulation speed is limited by the speed of the host system on which the simulator runs. If we could enable multithreading in the simulation, so that the concurrent activities are scheduled on multiple cores, a performance gain could be achieved. In addition, for such a multithreading to be successful, the communication between threads must not be a limiting factor.

Thesis Description

In this Master thesis work, we intend to develop a functional prototype for multithreading in a SystemC-based virtual platform. The work shall include design and implementation, using Linux threads, and mechanisms for thread communication and shared resource handling shall be selected and evaluated against each other. The resulting simulator shall be evaluated, using measurements from running Ericsson production software, and trade-offs for the parallelization, with respect to Linux thread partitioning and choice of concurrency mechanisms, shall be analyzed.

Qualifications

This project aims at students in electrical engineering, computer science, computer engineering or similar.

Extent

1-2 students, 30hp each

Location

Ericsson AB Kista, Stockholm

Preferred Starting Date

Spring 2020