Master Thesis – ASIC IO

Background
With the introduction of 5G the push for greater integration of functions into ASIC is accelerated, and the semiconductor industry push for smaller and smaller geometries. Has increased the relative cost of implementing a general-purpose Input Output pin. These pins are required to interface other components on a board, and often require much higher voltages then otherwise used with the ASIC.
This master thesis will investigate cost saving opportunities for ASIC IO.

Thesis Description
This thesis is divided into several steps

The following steps are envisioned as part of the thesis work:

- Investigate current usage of ASIC IO’s
- Investigate different cost savings, cots device, cPLD or other
- Analyze cost benefits with a cost saving opportunity

The thesis will be concluded with a result presentation for the Ericsson Digital Asic team.

Qualifications
This project aims at students in electrical engineering, computer science, computer engineering or similar.

Extent
1-2 students, 30hp each

Location
Ericsson AB, Kista

Preferred Starting Date
Spring 2019

Keywords
ASIC, IO, cPLD, cots

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