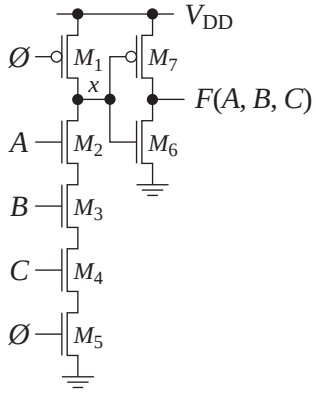
TSTE86 Homework 3: Solution

Inspect layout ⇒

Schematic



Function

$S_n = ABC \Rightarrow x = (ABC)' \Rightarrow \boxed{F = ABC}$

Gate, source, and drain widths

$W_1 = W_2 = W_3 = W_4 = W_5 = W_6 = 0.5$ µm, $W_7 = 1.0$ µm

Gate lengths

$L_1 = L_2 = L_3 = L_4 = L_5 = L_6 = L_7 = 0.25$ µm

Source lengths

$L_{s1} = L_{s5} = L_{s6} = L_{s7} = 0.5$ µm, $L_{s2} = L_{s3} = L_{s4} = 0.25$ µm

Drain lengths

$L_{d1} = L_{d2} = L_{d6} = L_{d7} = 0.75$ µm, $L_{d3} = L_{d4} = L_{d5} = 0.25$ µm

Metal wire dimensions of node x

$W_m = 0.375$ µm, $L_m \approx 7$ µm

Poly wire dimensions of node x

$W_p = 0.25$ µm, $L_p \approx 4$ µm

Worst-case PMOS drain capacitance of node x

$$C_{d1} \approx W_1 L_{d1} C_{j0p} + \left(W_1 + 2L_{d1}\right) C_{jsw0p} =$$

$$= 0.5\cdot 10^{-6} \cdot 0.75\cdot 10^{-6} \cdot 1.9\cdot 10^{-3} + \left(0.5\cdot 10^{-6} + 2\cdot 0.75\cdot 10^{-6}\right)\cdot 0.22\cdot 10^{-9} \text{ F} \approx 1.16 \text{ fF}$$

Worst-case NMOS drain capacitance of node x

$$C_{d2} \approx W_2 L_{d2} C_{j0n} + \left(W_2 + 2L_{d2}\right) C_{jsw0n} =$$

$$= 0.5\cdot 10^{-6} \cdot 0.75\cdot 10^{-6} \cdot 2.0\cdot 10^{-3} + \left(0.5\cdot 10^{-6} + 2\cdot 0.75\cdot 10^{-6}\right)\cdot 0.28\cdot 10^{-9} \text{ F} \approx 1.31 \text{ fF}$$

Worst-case gate capacitance of MOSFETs M_1 … M_6

$$C_{g1} = C_{g2} = C_{g3} = C_{g4} = C_{g5} = C_{g6} \approx W_i L_i C_{ox} = 0.5\cdot 10^{-6} \cdot 0.25\cdot 10^{-6} \cdot 6\cdot 10^{-3} \text{ F} = 0.75 \text{ fF}$$

Worst-case gate capacitance of MOSFET M_7

$$C_{g7} \approx W_7 L_7 C_{ox} = 1.0\cdot 10^{-6} \cdot 0.25\cdot 10^{-6} \cdot 6\cdot 10^{-3} \text{ F} = 1.5 \text{ fF}$$

Capacitance of metal wire of node x

$$C_m \approx W_m L_m C_{ma} + 2\left(W_m + L_m\right) C_{mf} =$$

$$= 0.375\cdot 10^{-6} \cdot 7\cdot 10^{-6} \cdot 35\cdot 10^{-6} + 2\left(0.375\cdot 10^{-6} + 7\cdot 10^{-6}\right)\cdot 55\cdot 10^{-12} \text{ F} \approx 0.91 \text{ fF}$$

Capacitance of poly wire of node x

$$C_p \approx W_p L_p C_{pa} + 2\left(W_p + L_p\right) C_{pf} =$$

$$= 0.25\cdot 10^{-6} \cdot 4\cdot 10^{-6} \cdot 75\cdot 10^{-6} + 2\left(0.25\cdot 10^{-6} + 4\cdot 10^{-6}\right)\cdot 40\cdot 10^{-12} \text{ F} \approx 0.42 \text{ fF}$$

Worst-case capacitance of node x

$C_x \approx C_{d1} + C_{d2} + C_{g1} + C_{g2} + C_{g6} + C_{g7} + C_m + C_p \approx \boxed{7.6 \text{ fF}}$

Initial state for worst case charge sharing is when all internal capacitances are discharged

- $A = 0$ turns off path to rest of the switch net
- $B = C = Ø = 1$ discharges the capacitances in the switch net

Output node x should then be precharged with no charging of internal capacitances

- $A = 0$ turns off path to rest of the switch net
- $Ø = 0$ precharges node x
- State of B and C does not matter since associated capacitances are already discharged

Worst case charge sharing occurs when the output node x shares its charge with internal ones

- $Ø = 1$ makes node x dynamic
- $A = B = 1$ connects node x to the switch net nodes and shares the charge
- $C = 0$ is needed for evaluating x to 1

Answers

a) Implemented funtion is $F = ABC$

b) Worst-case parasitic capacitance at node x is $C_x \approx 7.6$ fF

c) Largest charge sharing occurs for $\langle Ø,A,B,C \rangle = \langle 1,0,1,1 \rangle \rightarrow \langle 0,0,-,- \rangle \rightarrow \langle 1,1,1,0 \rangle$