

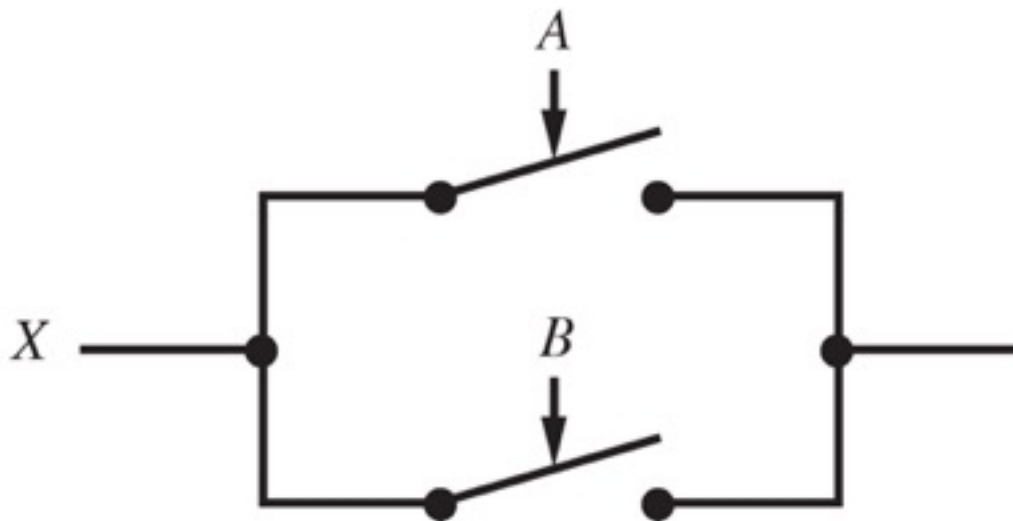
# Digital ICs — Lectures

1) <b>Introduction</b> [Ch. 1]	TSEI03/TSTE86
2) <b>Devices</b> [Ch. 3, 4]	TSEI03/TSTE86
3) <b>Interconnect</b> [Ch. 4, 9]	TSTE86
4) <b>Circuits</b> [Ch. 5]	TSEI03/TSTE86
5) <b>Combinational logic</b> [Ch. 6]	TSEI03/TSTE86
6) <b>Sequential circuits</b> [Ch. 7]	TSEI03/TSTE86
7) <b>Synchronization</b> [Ch. 10]	TSTE86
8) <b>Adders</b> [Ch. 11]	TSEI03/TSTE86
9) <b>Multipliers</b> [Ch. 11]	TSTE86
10) <b>Memory</b> [Ch. 12]	TSEI03/TSTE86
11) <b>Manufacturing</b> [Ch. 2]	TSTE86
12) <b>System design</b> [Ch. 8]	TSTE86

# Switch Nets

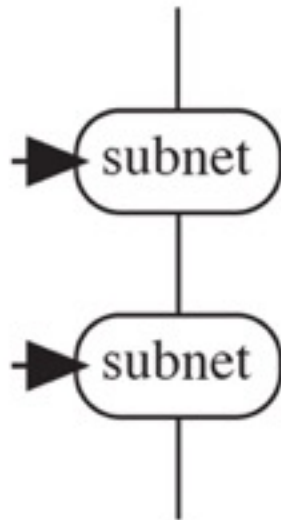


$X$  if  $A \cdot B$   
otherwise  $Z$



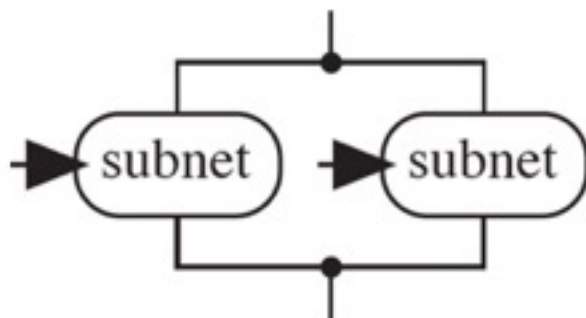
$X$  if  $A + B$   
otherwise  $Z$

# Subnets



## **AND net**

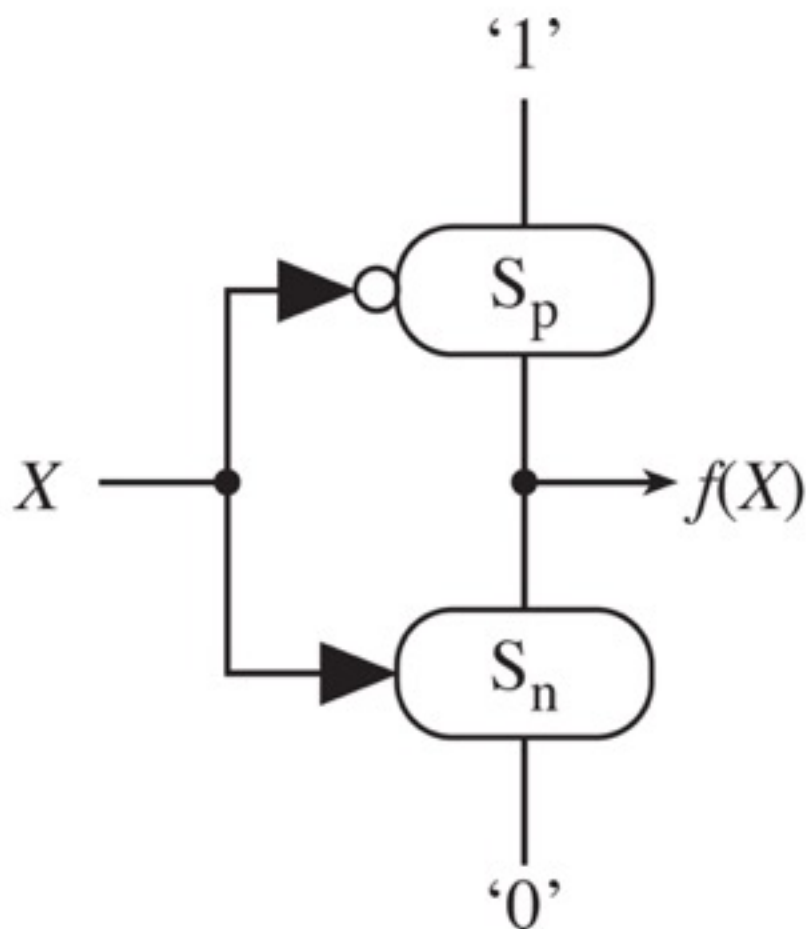
conducts when all subnets conduct



## **OR net**

conducts when any subnet conducts

# Static CMOS Switch Nets



Conducts when  $f(\bar{X}) = 1$

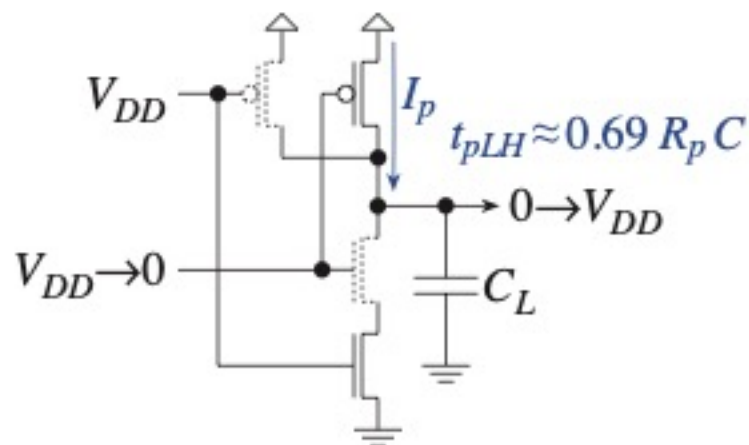
$$S_p = f(\bar{x}_1, \bar{x}_2, \dots, \bar{x}_m)$$

Conducts when  $f(X) = 0$

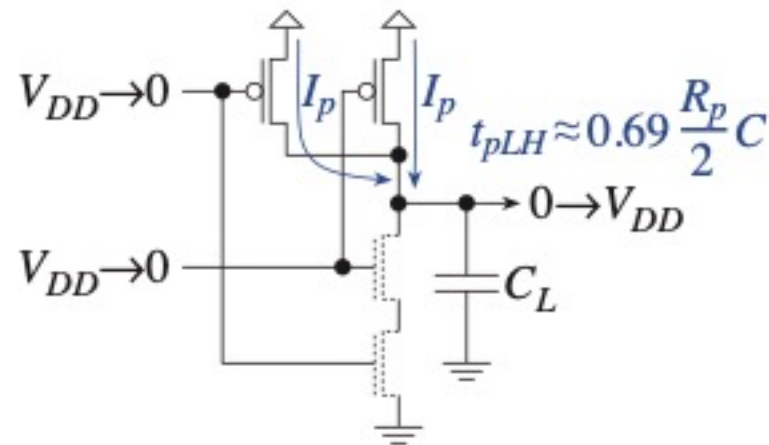
$$S_n = \overline{f(x_1, x_2, \dots, x_m)}$$

# Input Pattern Effects on Delay

Propagation delay of a NAND gate

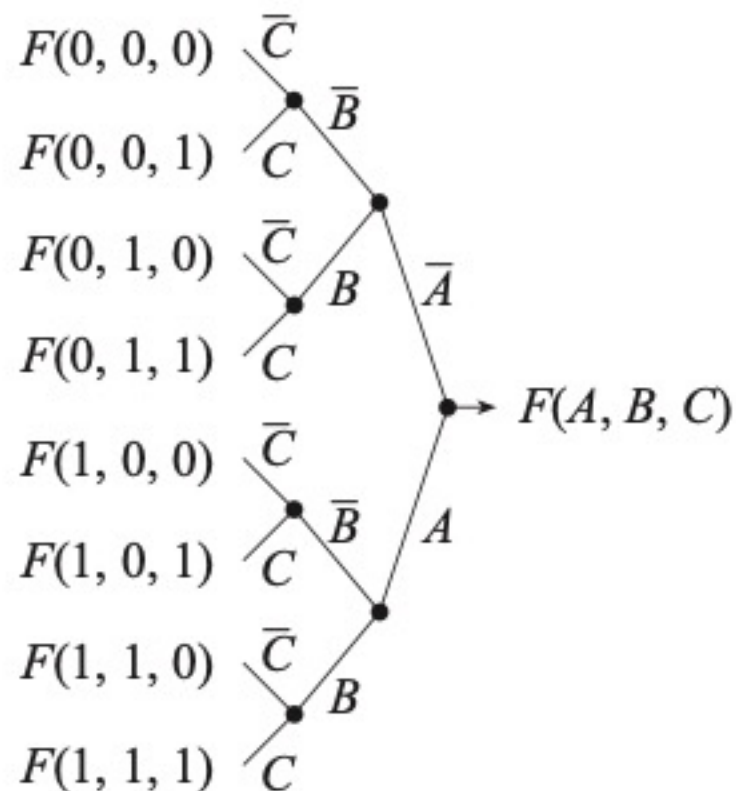


One input switches

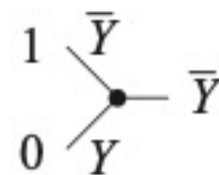
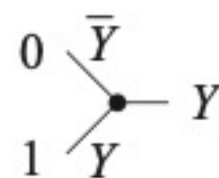
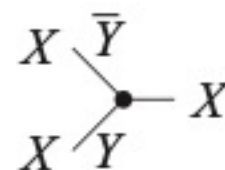


Two inputs switch

# Designing Pass Transistor Logic

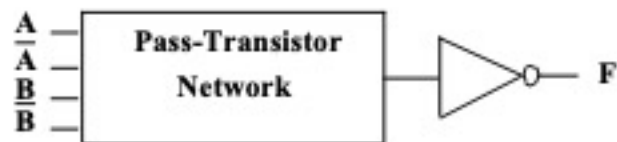


Start with binary tree

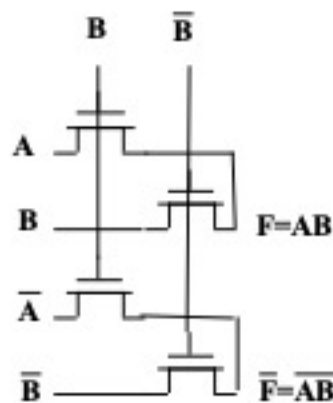
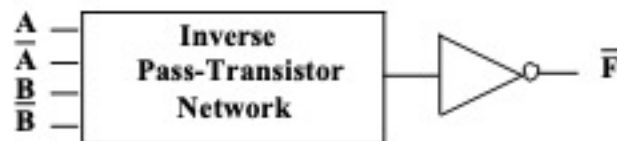


Simplify branches

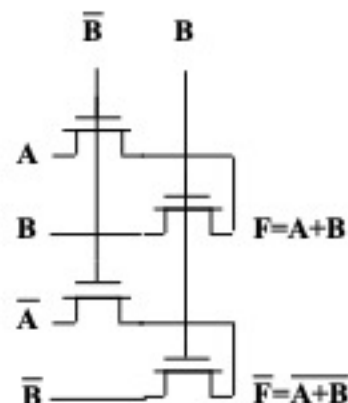
# Complementary Pass Transistor Logic



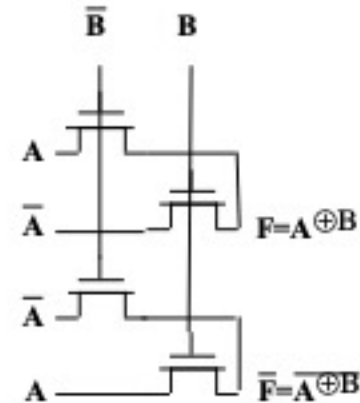
(a)



AND/NAND



OR/NOR

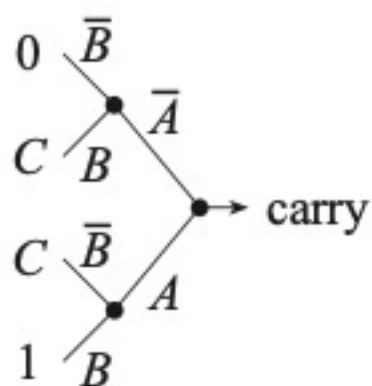


EXOR/NEXOR

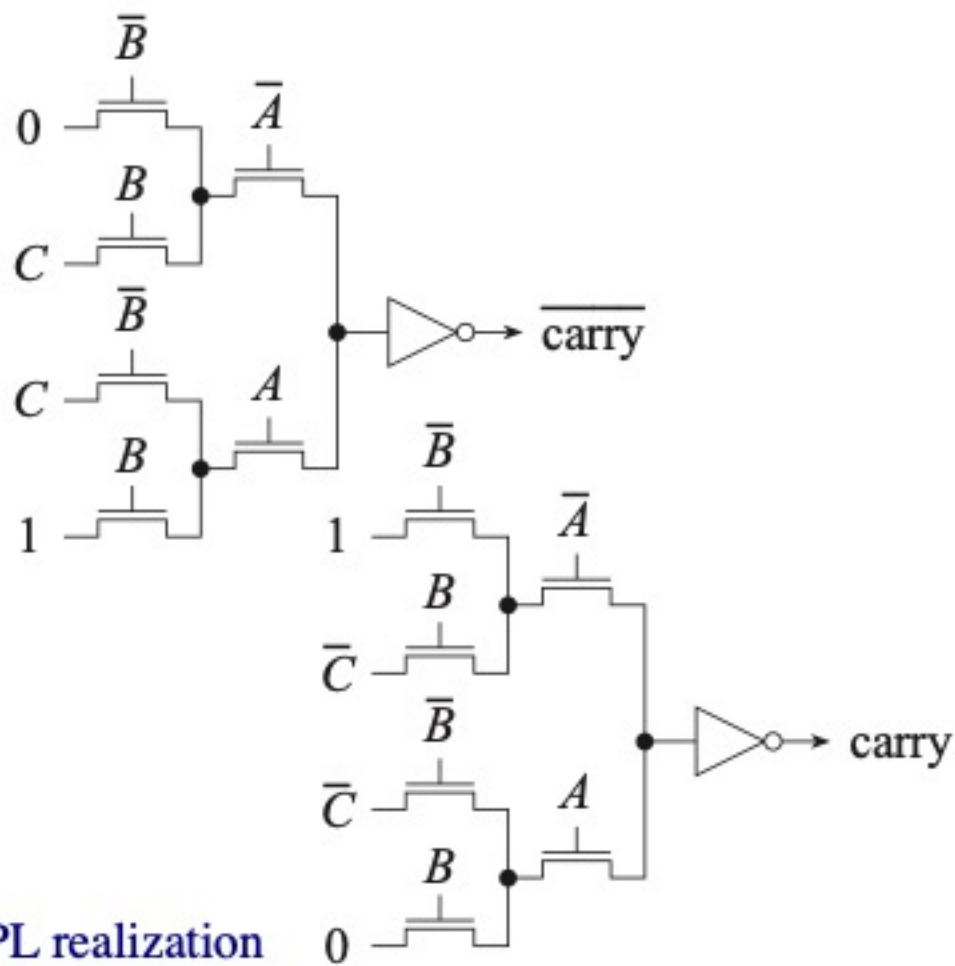
(b)



# Carry Function in CPL



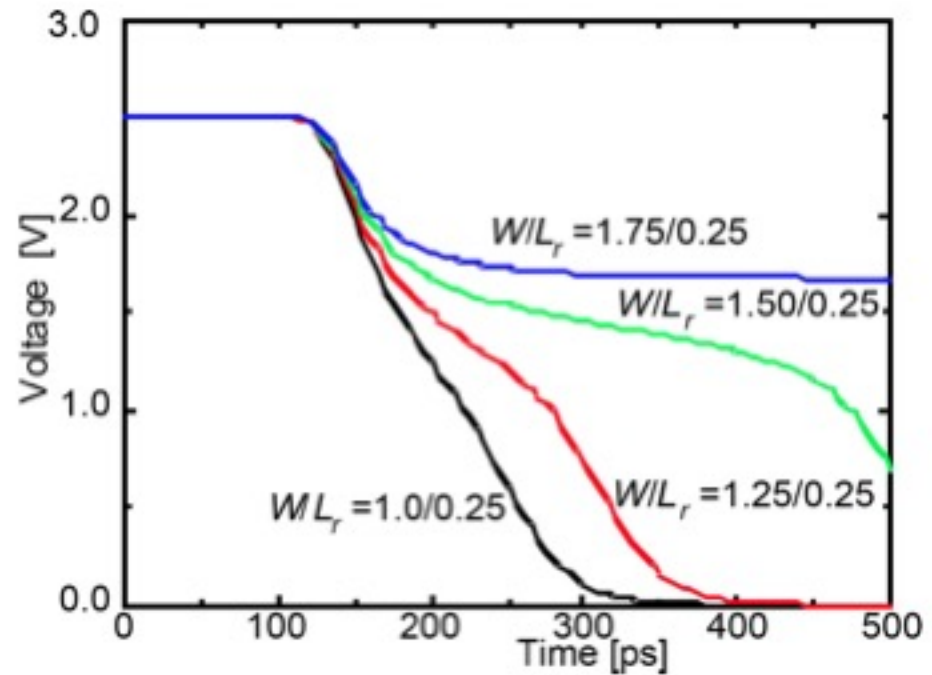
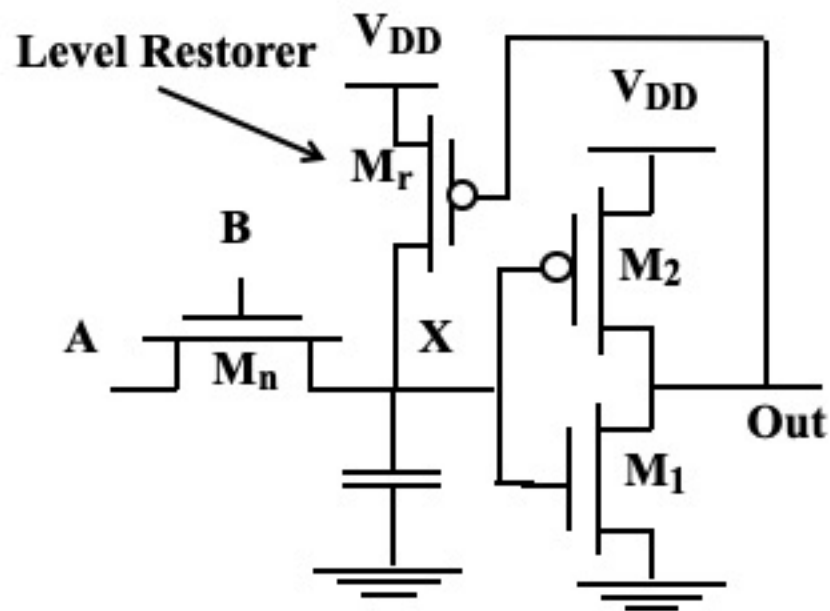
Binary carry tree



CPL realization



# Level Restoring Transistor



# Improved Switch: Transmission Gate

