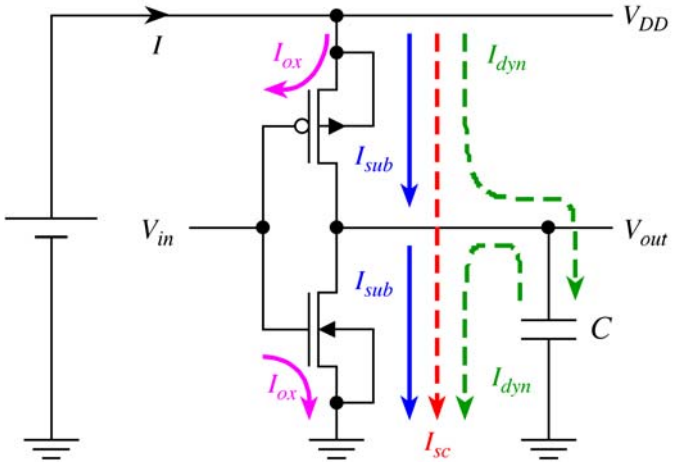
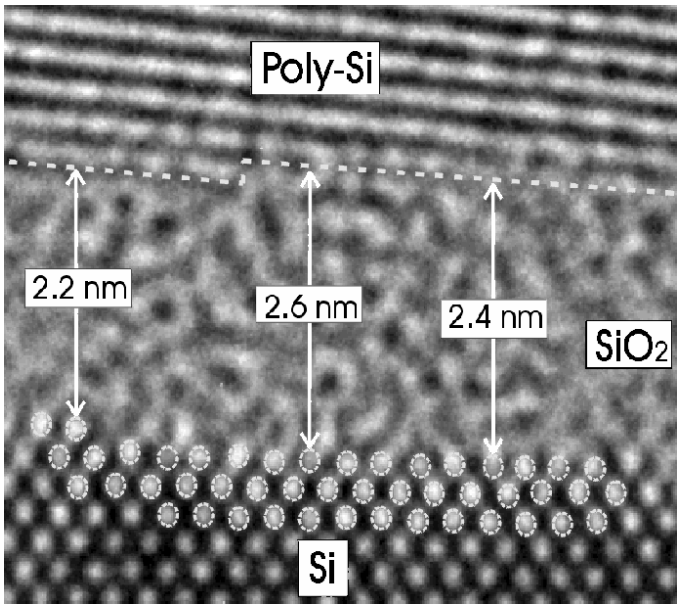
Power in nm-scale CMOS circuits



		Dynamic dissipation			Static dissipation
		Logic transitions		Short-circuit dissipation	Leakage
P_{total}	=	P_{switch}	+	$P_{short\text{-}circuit}$	+ $P_{leakage}$

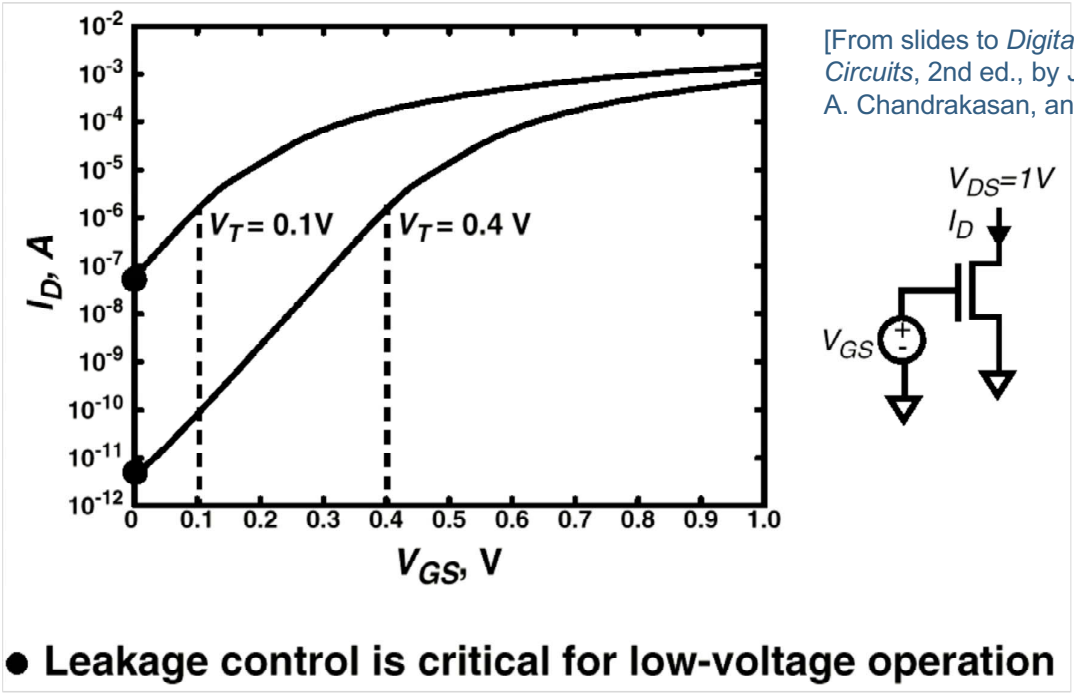
Gate-channel interface

- Precision is affected by single atoms
- Two devices do not look the same



[Picture from the book *Analog Circuit Design*, edited by H. Casier, M. Steyaert, and H.M. Arthur, Springer 2011]

Subthreshold leakage



[From slides to *Digital Integrated Circuits*, 2nd ed., by J.M. Rabaey, A. Chandrakasan, and B. Nikolic]

- **Leakage control is critical for low-voltage operation**

Trend in power dissipation

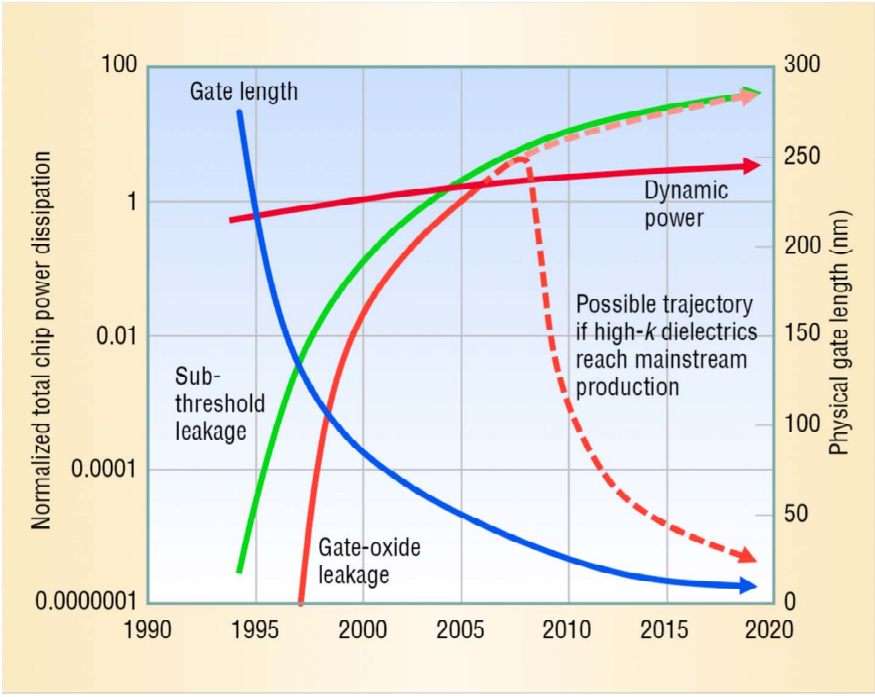


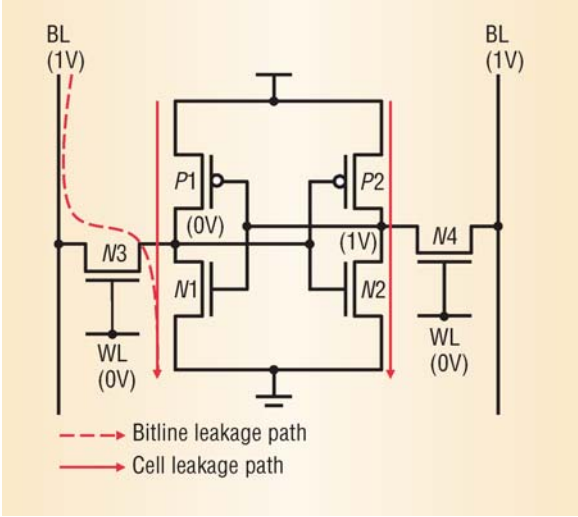
Figure 1

Cache memory leakage

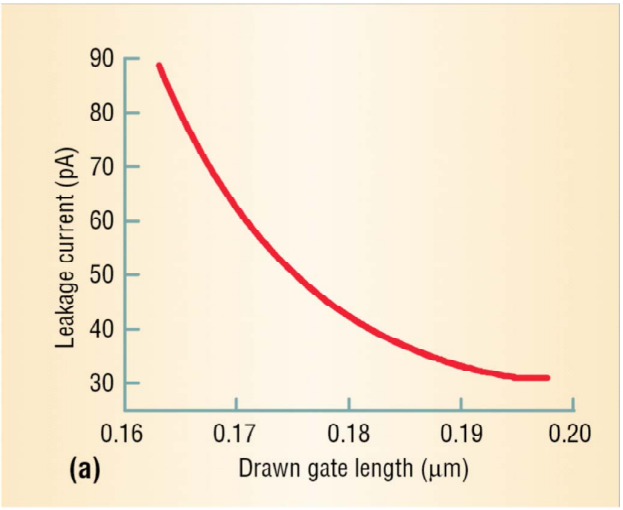
- Leakage is expected to account for major cache *P* contribution

- Reduction techniques
  - Turn-off part of cache
  - State preserving, 0.1*P*
    - low retention V_{DD}
    - adjusting V_T
    - asymmetric data
  - State destructive, 0.001*P*
    - gated V_{DD}
      - wake-up penalty

Figure 2



Leakage current and gate length



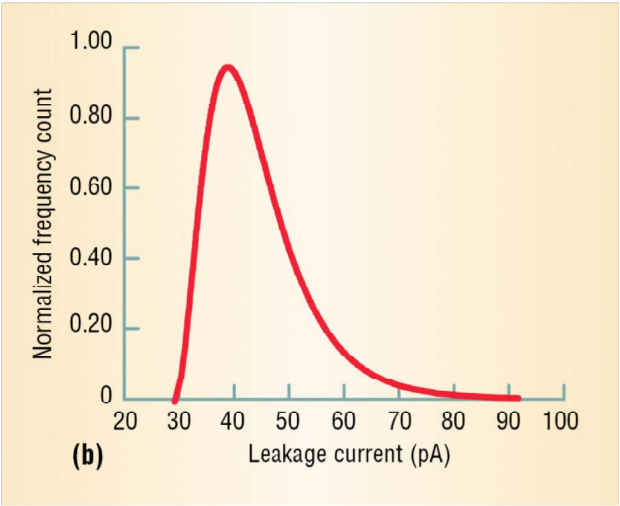


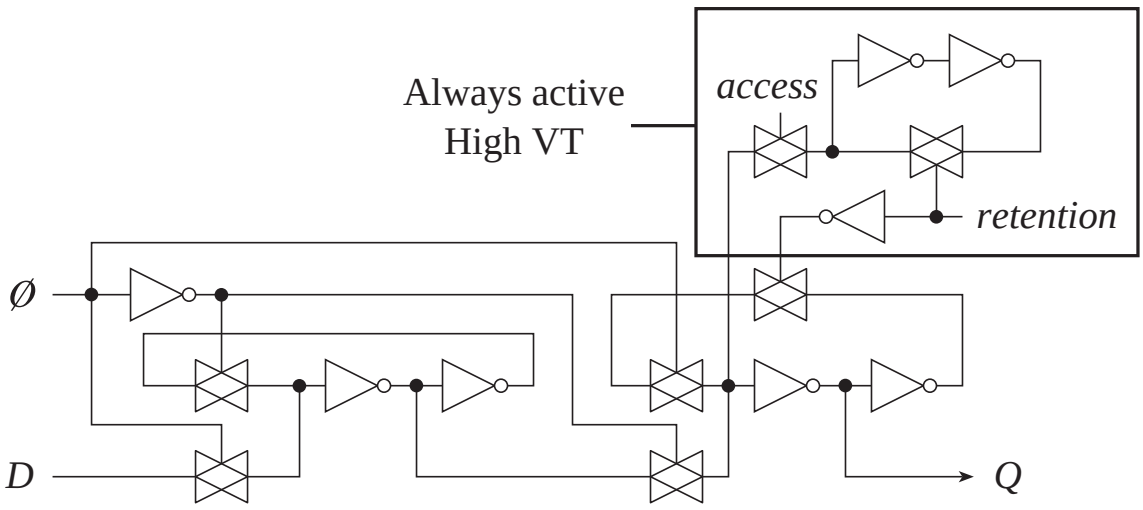
Figure 3

Voltage scaling in nm-scale CMOS

- Oxide and subthreshold leakage is proportional to gate width
  - Combined gate width is a measure of leakage, or
  - Gate count is a crude measure of leakage
- Parallel implementation add blocks
  - Voltage scaling reduces dynamic *P*
  - Increasing gate width increases leakage *P* proportionally
- Pipeline implementation add registers
  - Voltage scaling reduces dynamic *P*
  - Addition of registers increases leakage *P* marginally

Retention flip-flop

- Additional high-V_T latches may store sleep state



Sleep transistor design

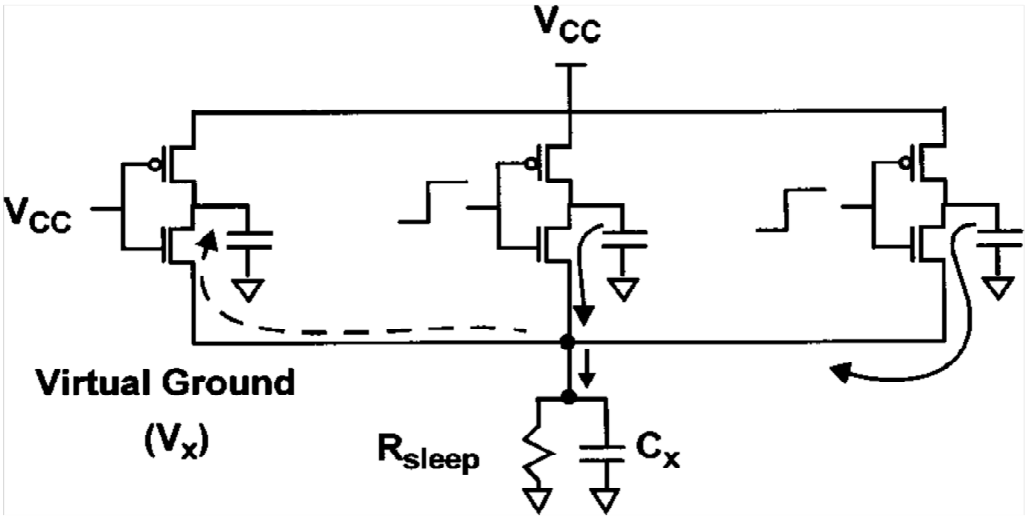


Fig. 2

Buffer with sleep transistor

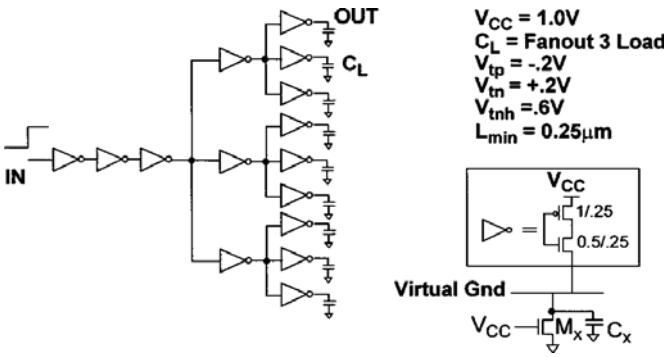


Fig. 3

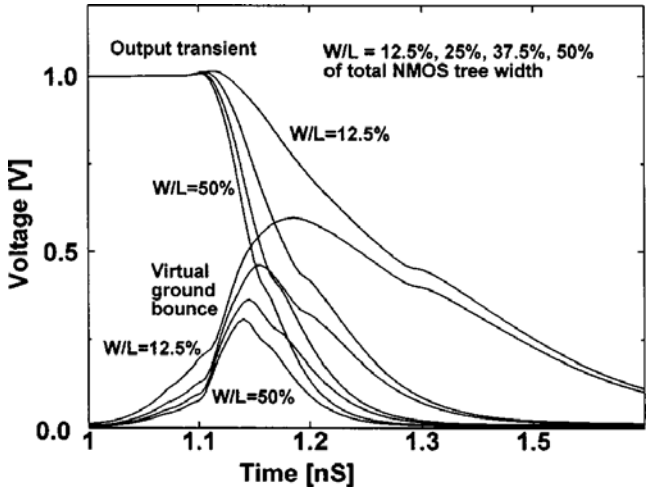


Fig. 4

Speed penalty from sleep transistor

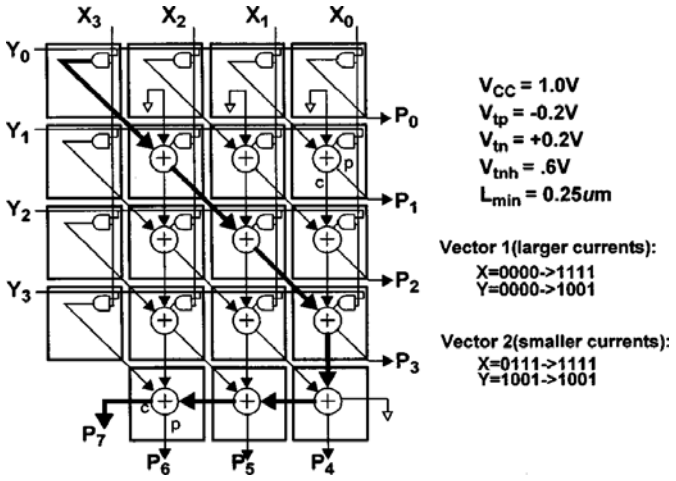


Fig. 5

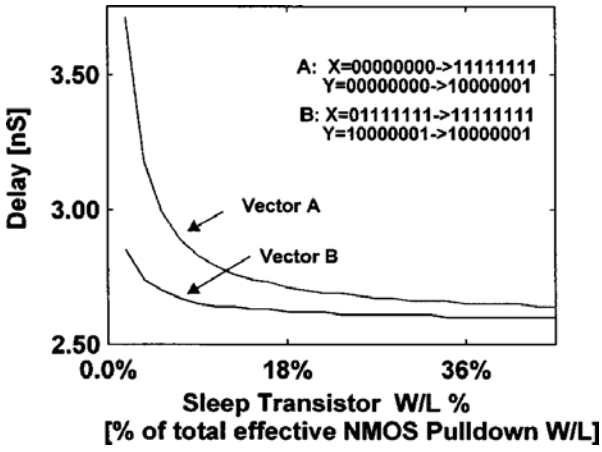


Fig. 6

Delay and power of 8x8-bit multiplier

Table 1—Delay

Initial X Y	Final X Y	Delay CMOS	% Degradation with W/L = 5.4%	% Degradation with W/L = 18%
0x 00 00	0x FF 81	2.59 ns	15.4%	4.6%
0x 7F 81	0x FF 81	2.58 ns	4.7%	1.6%

Table 2—Power

Circuit Approach	Dynamic Switching Energy per Event	Leakage Power Active Mode	Leakage Power Sleep Mode	Sleep Switching Energy per Event	Sleep Switching Breakeven Time
CMOS	~ 4e-12 [J]	1.5e-4 [W]	1.5e-4 [W]	NA	NA
MTCMOS W/L 18%	~ 4e-12 [J]	1.45e-4 [W]	2.2e-9 [W]	3.1e-14 [J]	2e-10 [S]

Sizing of sleep transistor in 6x6-bit mult.

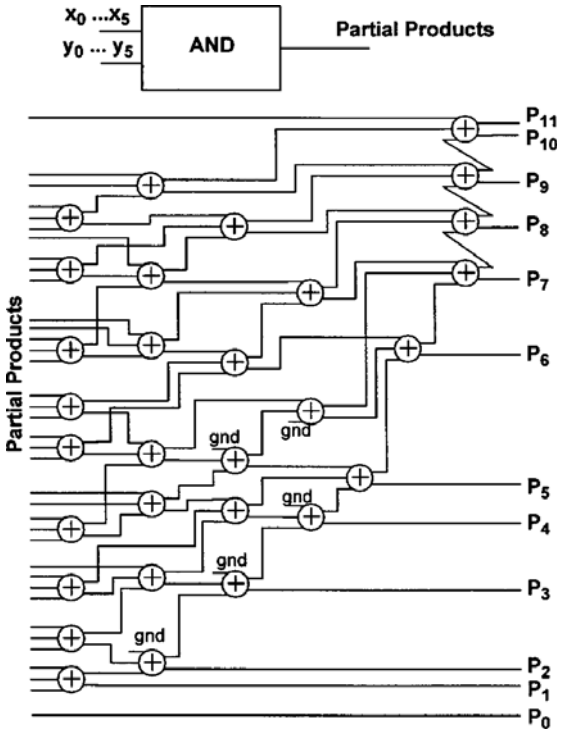
Ex: Design for max 5% speed degradation

i) 36 AND gates required $R_{AND} \approx 1350\ \Omega$
30 adders cells required $R_{CSA} \approx 800\ \Omega$

ii) mutually exclusive sets were identified

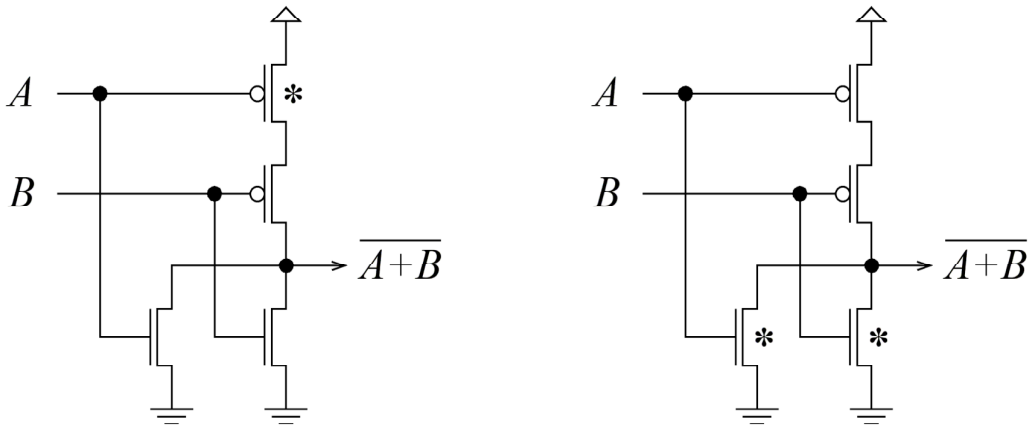
iii) worst-case R_{eq}:s were calculated

iv) $R_{tot} \approx 40\ \Omega$ for multiplier



Static CMOS with inherent sleep mode

- Force high V_T devices into off state during sleep
  - Ex: NOR and NAND gates (* = high V_T)



References

06.pdf **Leakage current: Moore's law meets static power**

N.S. Kim, T. Austin, D. Baauw, T. Mudge, K. Flautner, J.S. Hu, M.J. Irwin, M. Kandemir, and V. Narayanan

IEEE Computer, volume 36, issue 12, Dec. 2003, pages 68-75

07.pdf **Dual-threshold voltage techniques for low-power digital circuits**

J.T. Kao and A.P. Chandrakasan

IEEE Journal of Solid-State Circuits, volume 35, issue 7, July 2000, pages 1009-1018