SOLUTIONS. Exam June 05, 2008

TSTE08 and TSTE80 Analog and Discrete-time Integrated Circuits.

Excercise 1.

a) Transistor **M2** works in *saturation*.

Enclosed page of formulas gives:

$$I_{D2} = \frac{\mu_{0n} C_{ox}}{2} \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{tn})^2 (1 + \lambda(V_{DS2} - V_{eff2})) \tag{1}$$

Neglecting channal-length modulation (i.e. $\lambda = 0$) gives:

$$I_{D2} = \frac{\mu_{0n} C_{ox}}{2} \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{tn})^2 \tag{2}$$

Also transistor **M1** works in *saturation*. Neglecting channal-length modulation gives:

$$I_{D1} = I_0 = \frac{\mu_{0n} C_{ox}}{2} \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{tn})^2 \tag{3}$$

As $V_{GS1} = V_{GS2}$ equation (2) and equation (3) gives:

$$\frac{I_{D2}}{I_0} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \Rightarrow I_{D2} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_0 = K I_0 \tag{4}$$

Figure 1 gives:

$$V_{out} = V_{DD} - R I_{D2} \Rightarrow \underline{\underline{V_{out} = V_{DD} - RK I_0}} \tag{5}$$

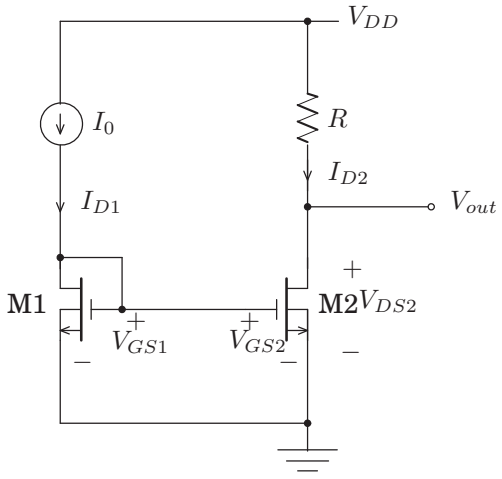

Figure 1: A commonly used analog circuit.

b) At the limit of saturation region

$$V_{DS} = V_{GS} - V_{tn} \tag{6}$$

In this case (note that $V_{GS2} = V_{GS1}$):

$$\left.\begin{array}{c} V_{DS2} = V_{out} \\ V_{GS2} - V_{tn} = V_{GS1} - V_{tn} = \sqrt{\frac{I_0}{\alpha_1}} \end{array}\right\} \overset{(6)}{\Rightarrow} V_{out} = \sqrt{\frac{I_0}{\alpha_1}} \tag{7}$$

But, as before in a):

$$V_{out} = V_{DD} - RKI_0 \tag{8}$$

Combining (7) and (8) yields

$$\sqrt{\frac{I_0}{\alpha_1}} = V_{DD} - RKI_0 \tag{9}$$

which is reformulated to

$$\underline{\underline{K = \frac{V_{DD} - \sqrt{\frac{I_0}{\alpha_1}}}{RI_0} = \frac{V_{DD}}{RI_0} - \frac{1}{R\sqrt{\alpha_1 I_0}}}} \tag{10}$$

which is the answer.

Exercise 2.

a) **Figure 2 a)** gives the complete small signal equivalent circuit (SSEC).

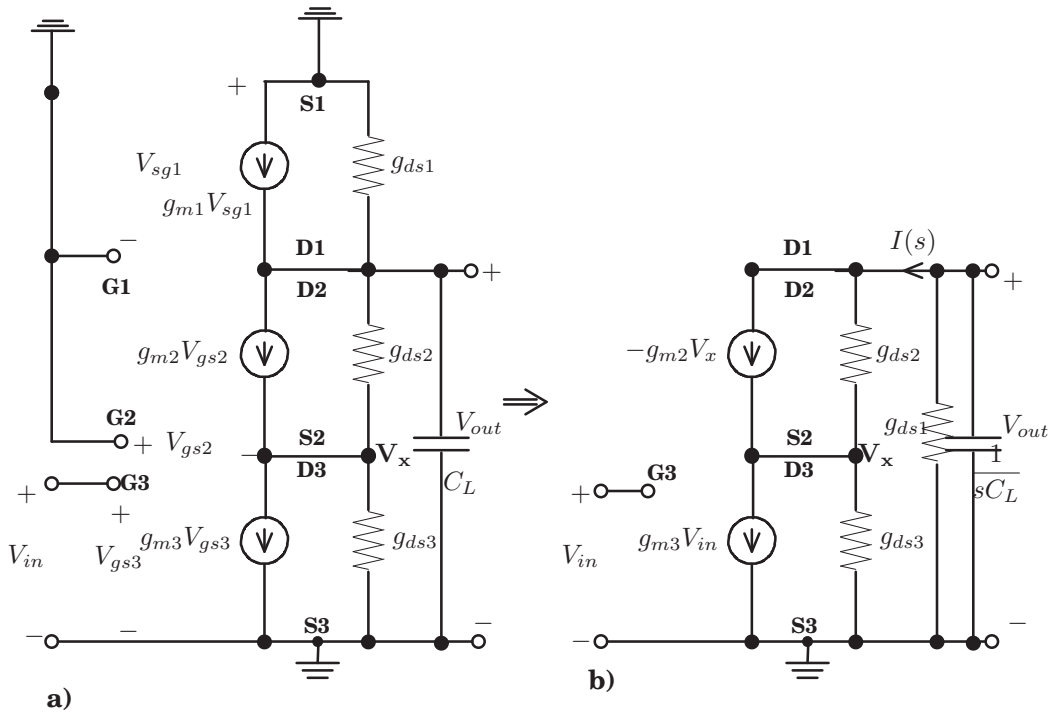

Figure 2: Small signal equivalent circuit.

In **Figure 2 b)** the SSEC has been redrawn noticing that:

- $V_{gs1} = 0$
- $V_{gs2} = 0 - V_{S2}$
- $V_{gs3} = V_{in}$
- g_{ds1} is parallel to $\frac{1}{sC}$

Introducing the voltage $\mathbf{V}_x$ in node **D3, S2** yields:

- $V_{gs2} = 0 - V_x = -V_x$

KCL in the output node and in ground node gives:

$$(0 - V_{out})(g_{ds1} + sC_L) - (-g_{m2}V_x) - g_{ds2}(V_{out} - V_x) = 0 \quad (11)$$

$$(V_{out} - 0)(g_{ds1} + sC_L) + g_{m3}V_{in} + g_{ds3}(V_x - 0) = 0 \quad (12)$$

$$(11) \Rightarrow V_x = \frac{V_{out}(g_{ds1} + g_{ds2} + sC_L)}{g_{m2} + g_{ds2}} \quad (13)$$

$$(12) \Rightarrow V_x = -\frac{V_{out}(g_{ds1} + sC_L) + g_{m3}V_{in}}{g_{ds3}} \quad (14)$$

I.e.

$$\frac{V_{out}(g_{ds1} + g_{ds2} + sC_L)}{g_{m2} + g_{ds2}} = -\frac{V_{out}(g_{ds1} + sC_L)}{g_{ds3}} - \frac{g_{m3}}{g_{ds3}}V_{in} \quad (15)$$

(15) gives:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{-g_{m3}}{g_{ds3}}}{\frac{(g_{ds1}+g_{ds2}+sC_L)}{g_{m2}+g_{ds2}} + \frac{(g_{ds1}+sC_L)}{g_{ds3}}} \quad (16)$$

Rewriting (16) gives the answer:

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{-g_{m3}}{\frac{g_{ds3}(g_{ds1}+g_{ds2})}{g_{m2}+g_{ds2}} + g_{ds1} + sC_L\left(1 + \frac{g_{ds3}}{g_{m2}+g_{ds2}}\right)}$$

b) Assuming $g_{mi} >> g_{dsj}$ gives following approximation of $H(s)$:

$$H(s) \approx \frac{-g_{m3}}{g_{ds1} + sC_L} = -\frac{g_{m3}}{g_{ds1}} \cdot \frac{1}{1 + \frac{sC_L}{g_{ds1}}} \quad (17)$$

(17) gives:

- DC-gain $A_0 = \frac{-g_{m3}}{g_{ds1}}$
- First (and only) pole $p_1 = -\frac{g_{ds1}}{C_L}$
- $$H(\omega) = \frac{-g_{m3}}{g_{ds1}} \cdot \frac{1}{1 + \frac{j\omega C_L}{g_{ds1}}} \Rightarrow |H(\omega)| = \frac{g_{m3}}{g_{ds1}} \cdot \frac{1}{\sqrt{1 + \left(\frac{\omega C_L}{g_{ds1}}\right)^2}}$$

  The 3-dB cut-off frequency ω_{3dB} is the frequency when
  $\sqrt{1 + \left(\frac{\omega C_L}{g_{ds1}}\right)^2} = \sqrt{2} \Rightarrow \omega_{3dB} = \frac{g_{ds1}}{C_L}$

Unity-gain frequency ω_u is the frequency when $|H(\omega)| = 1$.

$$|H(\omega)| = 1 \Rightarrow \frac{|A_0|}{\sqrt{1+\frac{\omega^2}{p_1^2}}} = 1 \Rightarrow \omega_u = |p_1|\sqrt{A_0^2 - 1} \approx |p_1||A_0|$$

In this case:

$$\omega_u \approx |p_1||A_0| = \frac{g_{ds1}}{C_L} \cdot \frac{g_{m3}}{g_{ds1}} = \frac{g_{m3}}{C_L} \tag{18}$$

Answer: $\underline{\underline{A_0 = \frac{-g_{m3}}{g_{ds1}}, \omega_{3dB} = \frac{g_{ds1}}{C_L}, \omega_u = \frac{g_{m3}}{C_L}}}$

c) As $g_{mi} \sim \sqrt{\frac{W_i}{L_i} I_{Di}}$ and $g_{dsi} \sim \frac{1}{L_i} I_{Di}$:

$$\underline{\underline{A_0 = \frac{-g_{m3}}{g_{ds1}} \sim \frac{\sqrt{\frac{W_3}{L_3} I_D}}{\frac{1}{L_1} I_D} = \sqrt{\frac{W_3 L_1^2}{L_3 I_D}}}} \tag{19}$$

Equation (19) yields that:

- $|A_0|$ decreases with a factor 2 when I_D increases with a factor 4.
- $|A_0|$ increases with a factor 2 when W_3 increases with a factor 4.

Exercise 3.

a) a) This exercise is solved using the charge redistribution analysis. The voltage at the node between C_1 and C_2 is here denoted $V_x(t)$. First, the reference direction of the charge is chosen. Next, the charge of the capacitors are computed for time t, $t+\tau$, and $t+2\tau$

For time t:

$$\begin{aligned} q_1(t) &= (0 - V_x(t))C_1 \\ q_2(t) &= (0 - V_x(t))C_2 \\ q_3(t) &= (V_{out}(t) - V_x(t))C_3 \\ q_4(t) &= (V_{out}(t) - 0)C_4 \end{aligned} \tag{20}$$

For time $t+\tau$:

$$\begin{aligned} q_1(t+\tau) &= (V_{in}(t+\tau) - 0)C_1 \\ q_2(t+\tau) &= 0 \\ q_3(t+\tau) &= q_3(t) \\ q_4(t+\tau) &= (V_{out}(t+\tau) - 0)C_4 \end{aligned} \tag{21}$$

For time $t+2\tau$:

$$\begin{aligned} q_1(t+2\tau) &= (0 - V_x(t+2\tau))C_1 \\ q_2(t+2\tau) &= (0 - V_x(t+2\tau))C_2 \\ q_3(t+2\tau) &= (V_{out}(t+2\tau) - V_x(t+2\tau))C_3 \\ q_4(t+2\tau) &= (V_{out}(t+2\tau) - 0)C_4 \end{aligned} \tag{22}$$

Equations for the charge conservation:

$$q_2(t) - q_4(t) = q_2(t+\tau) - q_4(t+\tau) \tag{23}$$

$$q_2(t+\tau) = q_2(t+2\tau) \tag{24}$$

$$-q_1(t+\tau) - q_2(t+\tau) - q_3(t+\tau) = -q_1(t+2\tau) - q_2(t+2\tau) - q_3(t+2\tau) \tag{25}$$

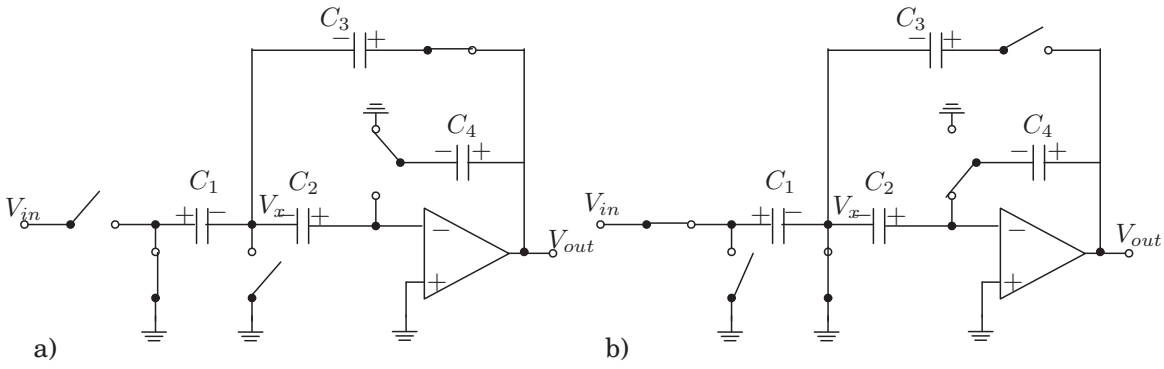

Figure 3: a) SC-circuit in clock phase 1. b) SC-circuit in clock phase 2.

As $q_2(t+\tau) = 0$ and $q_2(t+\tau) = q_2(t+2\tau)$ (24) also $q_2(t+2\tau) = 0$ and $V_x(t+2\tau) = 0$, which means that $V_x(t) = 0$ for all t.
Furthermore equation (23) gives:

$$(0 - V_x(t))C_2 - (V_{out}(t) - 0)C_4 = 0 - (V_{out}(t+\tau) - 0)C_4 \tag{26}$$

As $V_x(t) = 0$ equation (26) gives that:

$$V_{out}(t+\tau) = V_{out}(t) \tag{27}$$

As q_2 is zero for all t and $q_3(t+\tau) = q_3(t)$ equation (25) yields:

$$(V_{in}(t+\tau)-0)C_1+(V_{out}(t)-V_x(t))C_3 = (0-V_x(t+2\tau))C_1+(V_{out}(t+2\tau)-V_x(t+2\tau))C_3 \tag{28}$$

Using $V_x = 0$ for all t equation (28) can be simplified to:

$$V_{in}(t+\tau)C_1 + V_{out}(t)C_3 = V_{out}(t+2\tau)C_3 \tag{29}$$

Since $V_{in}(t+\tau) = V_{in}(t)$ (given in the exercise) equation (29) yields:

$$V_{in}(t)C_1 + V_{out}(t)C_3 = V_{out}(t+2\tau)C_3 \tag{30}$$

Setting $2\tau = T$ gives the differens equation:

$$C_1V_{in}(t) + C_3V_{out}(t) = C_3V_{out}(t+T) \tag{31}$$

Finally, z-transforming (31):

$$C_1V_{in}(z) + C_3V_{out}(z) = C_3zV_{out}(z) \tag{32}$$

Which gives the answer:

$$\underline{\underline{V_{out}(z) = \frac{C_1}{C_3} \cdot \frac{1}{z-1} \cdot V_{in}}}$$

b) Switches, capacitors, and the operational amplifier introduce parasitic capacitors into the circuit as is shown in **Figure 4**.

   * C_{pa} is connected between the ideal input voltage source and ground where the input source can source/sink as much charge as is required. Hence, this parasitics do not change the transfer function.

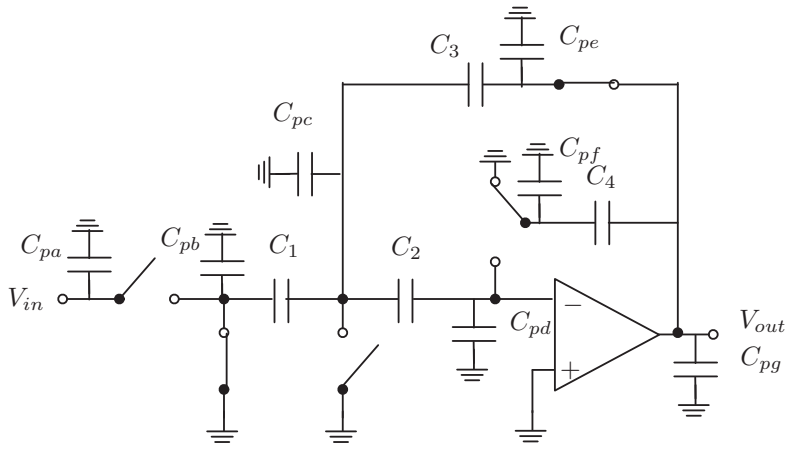

Figure 4: SC-circuit with parasitics in clock phase 1.

- C_{pb} is in one clock phase shorted to ground and the next connected to the ideal voltage source. Thus, the charge on the capacitor does not discharge into a sensitive node and this parasitic will not be part of the transfer function.
- C_{pc} is in one clock phase connected to virtual ground ($V_x = 0$) and the next connected to ground. Hence the transfer function will not be affected.
- C_{pd} is always connected to virtual ground and will not be part of the transfer function.
- C_{pe} is in one clock phase connected to the ideal output and the next connected to a floating node. Hence the transfer function will not be affected.
- C_{pf} is either shorted to ground or connected to virtual ground so the transfer function is not changed.
- C_{pg} is always connected to the ideal output of the operational amplifier and ground and thereby will not be a part of the transfer function.

Hence, the circuit is not sensitive to capacitive parasitics when the transfer function is of concern.

Exercise 4.

Figure 5 shows the circuit with voltages V_{GSi} and V_{DSi} introduced.

- For transistors **M1**, **M2**, **M5** and **M6**: $V_{DSi,min} = V_{effi} = \sqrt{\frac{I_{Di}}{\alpha_i}}$ and for transistor **M4** $V_{SD4,min} = \sqrt{\frac{I_{D4}}{\alpha_4}}$.
- For transistors **M7** and **M8**: $V_{DSi,min} = V_{GSi} = V_{effi} + V_{ti} = \sqrt{\frac{I_{Di}}{\alpha_i}} + V_{ti}$ and for transistor **M3** $V_{SD3,min} = \sqrt{\frac{I_{D3}}{\alpha_3}} + V_{t3}$.
- As **M5** and **M8** are identical the current mirror **M8**, **M5** will give the current I_0 through **M5** and **M6** as well as through **M7** and **M8**.
- As **M3** and **M4** are identical the currents trough **M1** and **M2**, as well as through **M3** and **M4**, will be $\frac{I_0}{2}$.

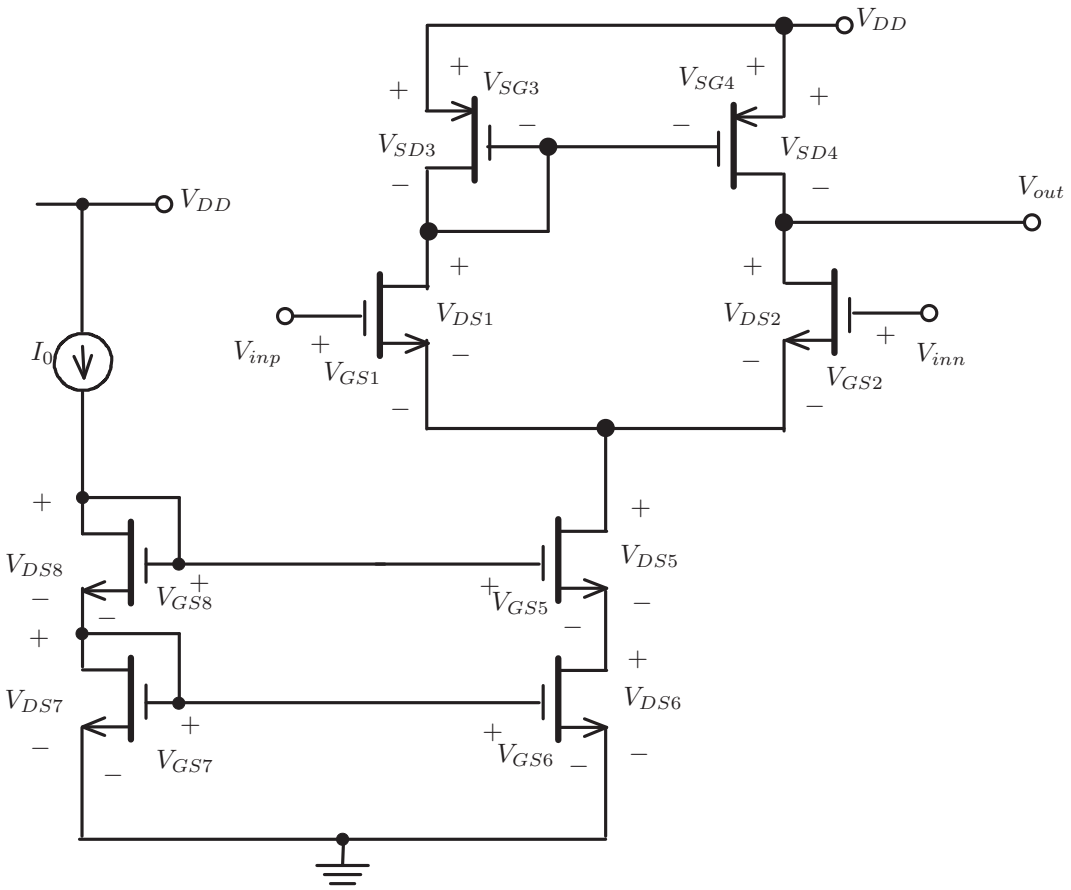

Figure 5: Differential gain-stage.

I. First we will determine $CMR = [V_{in,min}; V_{in,max}]$.

Because of symmetry $V_{inn,min} = V_{inp,min}$, so we just have to look at one of the input voltages, e.g. V_{inp}.

$V_{in,min}$ will be the **maximum value** of

$$V_{DS6,min} + V_{DS5,min} + V_{GS1} = \sqrt{\frac{I_0}{\alpha_6}} + \sqrt{\frac{I_0}{\alpha_5}} + \sqrt{\frac{I_0/2}{\alpha_1}} + V_{t1} \tag{33}$$

and

$$V_{DS7,min} + V_{GS8} - V_{GS5} + V_{DS5,min} + V_{GS1} \quad =$$

$$= \sqrt{\frac{I_0}{\alpha_7}} + V_{t7} + \sqrt{\frac{I_0}{\alpha_8}} + V_{t8} - V_{t5} + \sqrt{\frac{I_0/2}{\alpha_1}} + V_{t1} \tag{34}$$

As **M6** and **M7** are identical the first terms in (33) and (34) are the same, and as **M5** and **M8** are identical $\sqrt{\frac{I_0}{\alpha_5}} = \sqrt{\frac{I_0}{\alpha_8}}$ and $V_{t5} = V_{t8}$. Thus, (34) include all terms in (33) and also the term V_{t7}. That means that (34) must be larger than (33). I.e.

$$\underline{\underline{V_{in,min} = \sqrt{\frac{I_0}{\alpha_7}} + V_{t7} + \sqrt{\frac{I_0}{\alpha_8}} + \sqrt{\frac{I_0}{2\alpha_1}} + V_{t1}}} \tag{35}$$

$V_{in,max}$ will be the **smallest of** $V_{inn,max}$ and $V_{inp,max}$ i.e. the smallest of

$$V_{DD} - V_{SD4,min} - V_{DS2,min} + V_{GS2} = V_{DD} - \sqrt{\frac{I_0/2}{\alpha_4}} - \sqrt{\frac{I_0/2}{\alpha_2}} + \sqrt{\frac{I_0/2}{\alpha_2}} + V_{t2} \tag{36}$$

and

$$V_{DD} - V_{SD3,min} - V_{DS1,min} + V_{GS1} = V_{DD} - \sqrt{\frac{I_0/2}{\alpha_3}} - V_{t3} - \sqrt{\frac{I_0/2}{\alpha_1}} + \sqrt{\frac{I_0/2}{\alpha_1}} + V_{t1} \tag{37}$$

Because of matched transistor only the term V_{t3} differs in (37) compared to (36), making (37) smaller. Thus

$$\underline{\underline{V_{in,max} = V_{DD} - \sqrt{\frac{I_0/2}{\alpha_3}} - V_{t3} + V_{t1}}} \tag{38}$$

II. Determination of $OR = [V_{out,min}; V_{out,max}]$:

As when determining $V_{out,min}$ the path from ground through **M7** and **M8** will give a larger $V_{out,min}$ (compared to the path through **M6** and **M5**). Then you have to compare the path through **M2** and the path through **M1**, **M3** and **M4**.

The path through **M2** will give the contribution $V_{DS2,sat}$ to $V_{out,min}$ while the other path will give the contribution $V_{DS1,sat} + V_{SG4} - V_{SD4,sat} = V_{DS1,sat} + V_{t4}$. As $V_{DS2,sat} = V_{DS1,sat}$, because of matched transistors, $V_{DS1,sat} + V_{t4}$ will give the largest contribution to $V_{out,min}$. I.e.

$$\underline{\underline{V_{out,min}}} = V_{DS7,min} + V_{GS8} - V_{GS5} + V_{DS5,min} + V_{DS1,min} + V_{t4} \quad = \quad \underline{\underline{\sqrt{\frac{I_0}{\alpha_7}} + V_{t7} + \sqrt{\frac{I_0}{\alpha_8}} + \sqrt{\frac{I_0/2}{\alpha_1}} + V_{t4}}} \tag{40}$$

$V_{out,max}$ will be the smallest value of

$$V_{DD} - V_{SD4,min} = V_{DD} - \sqrt{\frac{I_0/2}{\alpha_4}} \tag{41}$$

and

$$V_{DD} - V_{SG3} - V_{DS1,min} + V_{DS2,min} = V_{DD} - V_{SG3} \tag{42}$$

The last equality comes from the fact that $V_{DS1} = V_{DS2}$ as $V_{GS1} = V_{GS2}$ in Common Mode (**M1** and **M2** are identical and $V_{inn} = V_{inp}$).

As $\alpha_3 = \alpha_4$ (42) gives the smallest value.

$$\underline{\underline{V_{out,max} = V_{DD} - \sqrt{\frac{I_0/2}{\alpha_3}} - V_{tp}}} \tag{43}$$

Exercise 5.

First, draw a small signal equivalent circuit for the amplifier.

The thermal noise kan be represented by a voltage source between Gate-Source with spectral density $R = \frac{8kT}{3} \cdot \frac{1}{g_m}$ or by a current parallel to Drain-Source with spectral density $R = \frac{8kT}{3} \cdot g_m$, as the small-signal drain current $i_d = g_m v_{gs}$.

In the small signal equivalent circuit we also use to have a current source $g_{bs}V_{bs}$, parallel to Drain-Source, when $V_{bs} \neq 0$. As the substrate noise is represented by a voltage souce V_{sn} between bulk and souce in the given figure, the substrate noise can be represented by a current souce $g_{bs}V_{sn}$ parallel to Drain-Source in the small signal equivalent circuit.

Thus, the thermal noise as well as the substrate noise are represented by current noise sources between Drain-Source.

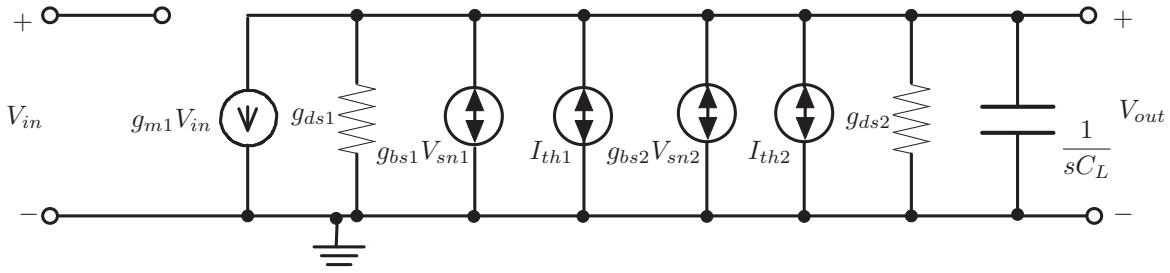

Figure 6: Determing $H_{thi} = V_{out}/I_{thi}$ and $H_{sni} = V_{out}/V_{sni}$.

As $V_{out} = I_{thi} \cdot \frac{1}{g_{ds1}+g_{ds2}+sC_L}$ when $V_{in} = 0$ and $V_{sni} = 0$, the transfer function $H_{thi}(s)$ from each current source I_{thi} to the output (zeroing the input signal, i.e. $V_{in} = 0$) will be:

$$H_{thi}(s) = \frac{V_{out}}{I_{thi}} = \frac{1}{g_{ds1} + g_{ds2} + sC_L} \Rightarrow H_{thi}(\omega) = \frac{1}{g_{ds1} + g_{ds2} + j\omega C_L} \tag{44}$$

$I_{thi} = g_{mi}V_{thi}$ givs spectral density $g_{mi}^2 V_{thi}^2 = \frac{8kT}{3} \cdot g_{mi}$ for I_{thi}

As $V_{out} = g_{bsi}V_{sni} \cdot \frac{1}{g_{ds1}+g_{ds2}+sC_L}$ when $V_{in} = 0$ and $I_{thi} = 0$, the transfer function $H_{sni}(s)$ from each voltage source V_{sni} to the output (zeroing the input signal, i.e. $V_{in} = 0$) will be:

$$H_{sni}(s) = \frac{V_{out}}{V_{sni}} = \frac{g_{bsi}}{g_{ds1} + g_{ds2} + sC_L} \Rightarrow H_{sni}(\omega) = \frac{g_{bsi}}{g_{ds1} + g_{ds2} + j\omega C_L} \tag{45}$$

As all noise-sources are uncorrelated, the output noise spectral density can be computed by the following formula

$$R_{out}(\omega) = \sum_i |H_i(\omega)|^2 R_i(\omega) = \frac{1}{(g_{ds1} + g_{ds2})^2 + (\omega C_L)^2}(R_0(g_{bs1}^2 + g_{bs2}^2) + \frac{8kT}{3}(g_{m1} + g_{m2})) \tag{46}$$

Answer:

$$\underline{\underline{R_{out} = \frac{R_0(g_{bs1}^2 + g_{bs2}^2) + \frac{8kT}{3}(g_{m1} + g_{m2})}{(g_{ds1} + g_{ds2})^2 + (\omega C_L)^2}}} \tag{47}$$