SOLUTIONS. Exam January 12, 2006

TSTE80 Analog and Discrete-time Integrated Circuits.

1. Large-signal analysis

a) M1 (n-channel) saturated if: $V_{GS} > V_{Tn}$ and $V_{DS} \geq V_{GS} - V_{Tn}$

$V_{Tn,max} = V_{Tn,0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}) = 0.5 + 0.5(\sqrt{2 \cdot 0.4 - (0 - 1.5)} - \sqrt{2 \cdot 0.4}) \approx 0.811$ V

($V_{BS} = V_B - V_S = 0 - V_{in}$; $V_{in,max} = 1.5$ V $\Rightarrow V_{BS} = -1.5$ V $\Rightarrow V_{Tn,max}$)

$$\left.\begin{array}{l} V_{DS} \geq V_{GS} - V_{Tn} \\ V_{DS} = V_{out} - V_{in} \end{array}\right\} \Rightarrow V_{out} - V_{in} \geq V_{GS} - V_{Tn} \Rightarrow V_{out} - V_{in} \geq V_{bias1} - V_{in} - V_{Tn} \Rightarrow V_{out} \geq V_{bias1} - V_{tn}$$

$V_{bias1} = 2.5$ V and $V_{Tn,max} = 0.811$ V gives $V_{out,min} \approx 1.7$ V

M2 (p-channel) saturated if: $V_{SG} > V_{Tp}$ and $V_{SD} \geq V_{SG} - V_{Tp}$:

$$\left.\begin{array}{l} V_{SD} \geq V_{SG} - V_{Tp} \\ V_{SD} = V_{DD} - V_{out} \\ V_{SG} = V_{DD} - V_{bias2} \end{array}\right\} \Rightarrow V_{DD} - V_{out} \geq V_{DD} - V_{bias2} - V_{Tp} \Rightarrow V_{out} \leq V_{bias2} + V_{Tp}$$

$V_{bias2} = 2$ V and $V_{Tp} = 0.6$ V gives $V_{out,max} = 2.6$ V

Answer: $V_{out,min} \approx 1.7$ V and $V_{out,max} = 2.6$ V

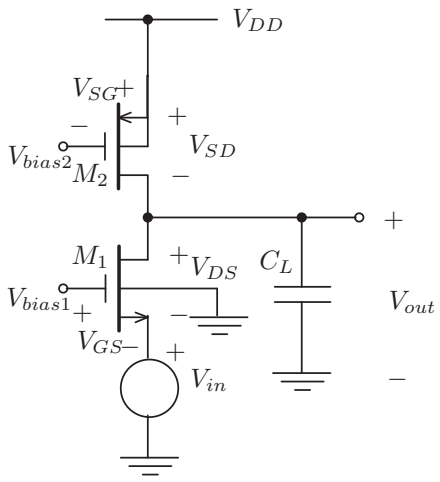

Figure 1: Amplifier. Large-signal analysis

b) M1:

$$I_D = \frac{\mu_{0n} C_{ox}}{2} \left(\frac{W}{L}\right)_1 (V_{GS} - V_{Tn})^2 (1 + \lambda_n V_{DS}) \Rightarrow \left(\frac{W}{L}\right)_1 = \frac{I_{Dsat}}{\frac{\mu_{0n} C_{ox}}{2} (V_{GS} - V_{Tn})^2 (1 + \lambda_n V_{DSsat})}$$

I_{Dsat} max. when V_{GS} max. and V_{DSsat} max.

$V_{GS} = V_{bias1} - V_{in}$ and $V_{DSsat} = V_{GS} - V_{Tn}$.

$V_{in,min} = 0 \Rightarrow V_{GS,max} = V_{bias1}$ and $V_{DSsat,max} = V_{bias1} - V_{Tn}$. (OBS! $V_{Tn} = V_{Tn,0} = 0.5$ when $V_{in} = 0$ because here $V_{BS} = 0$ when $V_{in} = 0$.)

I.e.

$$\left(\frac{W}{L}\right)_1 \leq \frac{I_{Dsat,max}}{\frac{\mu_{0n}C_{ox}}{2}\left(V_{bias1} - V_{Tn}\right)^2\left(1 + \lambda_n(V_{bias1} - V_{Tn})\right)} = \frac{0.1 \cdot 10^{-6}}{10 \cdot 10^{-9}(2.5 - 0.5)^2(1 + 0.03(2.5 - 0.5))} \approx 2.36$$

M2:

$$I_D = \frac{\mu_{0p}C_{ox}}{2}\left(\frac{W}{L}\right)_2\left(V_{SG} - V_{Tp}\right)^2(1+\lambda_p V_{SD}) \Rightarrow \left(\frac{W}{L}\right)_2 \leq \frac{I_{Dsat}}{\frac{\mu_{0p}C_{ox}}{2}\left(V_{SG} - V_{Tp}\right)^2(1 + \lambda_p V_{SDsat})}$$

$V_{SG} = V_{DD} - V_{bias2} = 3 - 2 = 1$ and $V_{SDsat} = V_{SG} - V_{Tp} = V_{DD} - V_{bias2} - V_{Tp} = 3 - 2 - 0.6 = 0.4$ V.

I.e.

$$\left(\frac{W}{L}\right)_2 \leq \frac{0.1 \cdot 10^{-6}}{3 \cdot 10^{-9}(1 - 0.6)^2(1 + 0.05 \cdot 0.4)} \approx 204$$

Answer: $\underline{\underline{\left(\frac{W}{L}\right)_1 \leq 2.36,\ \left(\frac{W}{L}\right)_2 \leq 204}}$

c) M1: $V_{GS} = V_{bias1} - V_{in}$ and $V_{GS} > V_{Tn,max}$ gives $V_{bias1} - V_{in} > V_{Tn,max} \Rightarrow V_{bias1} > V_{in,max} + V_{Tn,max} \approx 2.311$ V ($V_{Tn,max} \approx 0.811$ from a))

M2:

$V_{SB} = 0 \Rightarrow V_{Tp} = V_{T,0} = 0.6$ V

$V_{SG} = V_{DD} - V_{bias2}$ and $V_{SG} > V_{Tp}$ gives $V_{DD} - V_{bias2} > V_{Tp} \Rightarrow V_{bias2} < V_{DD} - V_{Tp} = 2.4$ V

Answer: $\underline{\underline{V_{bias1} > 2.311 \text{ V}, V_{bias2} < 2.4 \text{ V}}}$

2. Small-signal analysis

a) As the small signals $V_{gs2} = 0$ and $V_{bs2} = 0$ we can sketch following SSEC:

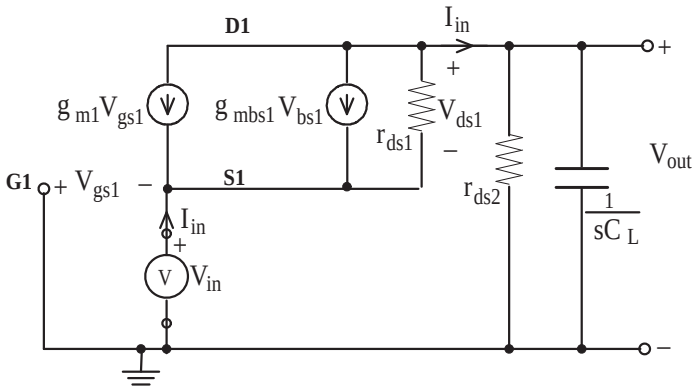

Figure 2: Amplifier. Small-signal analysis. Small-signal equivalent circuit

KCL in node D1 gives:

$$(V_{out} - 0)(g_{ds2} + sC_L) + V_{ds1}g_{ds1} + g_{m1}V_{gs1} + g_{mbs1}V_{bs1} = 0 \tag{1}$$

SSEC also gives: $V_{ds1} = V_{out} - V_{in}$ and $V_{gs1} = -V_{in}$.
Because bulk is grounded $V_{bs1} = 0 - V_{in}$.

(1) now gives:

$$V_{out}(g_{ds2} + sC_L) + (V_{out} - V_{in})g_{ds1} - g_{m1}V_{in} - g_{mbs1}V_{in} = 0 \tag{2}$$

(2) gives $H(s)$:

$$\underline{\underline{H(s)}} = \frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{m1} + g_{mbs1} + g_{ds1}}{g_{ds1} + g_{ds2} + sC_L} = \underline{\underline{\frac{g_{m1} + g_{mbs1} + g_{ds1}}{g_{ds1} + g_{ds2}} \cdot \frac{1}{1 + \frac{sC_L}{g_{ds1} + g_{ds2}}}}} \tag{3}$$

$s = 0$ in (3) gives DC gain A_0:

$$\underline{\underline{A_0 = \frac{g_{m1} + g_{mbs1} + g_{ds1}}{g_{ds1} + g_{ds2}}}}$$

b) $Z_{in} = \frac{V_{in}(s)}{I_{in}(s)}$

Noting that the current through $r_{ds2}//1/sC_L$ is I_{in}, V_{out} can be written as:

$$V_{out} = \frac{1}{g_{ds2} + sC_L} \cdot I_{in} \tag{4}$$

(3) gives:

$$V_{out} = \frac{g_{m1} + g_{mbs1} + g_{ds1}}{g_{ds1} + g_{ds2} + sC_L} \cdot V_{in} \tag{5}$$

(4), (5) gives:

$$\underline{\underline{Z_{in} = \frac{V_{in}}{I_{in}} = \frac{g_{ds1} + g_{ds2} + sC_L}{(g_{m1} + g_{mbs1} + g_{ds1})(g_{ds2} + sC_L)}}}$$

c) Setting the voltage source at the input to zero, i.e. replaceing it with a short-circuit, and introduceing V_{out} and I_{out} at the output (see **Figure 3)** gives $r_{out} = \frac{V_{out}}{I_{out}}$. (OBS! $V_{bs1} = 0$ now.)

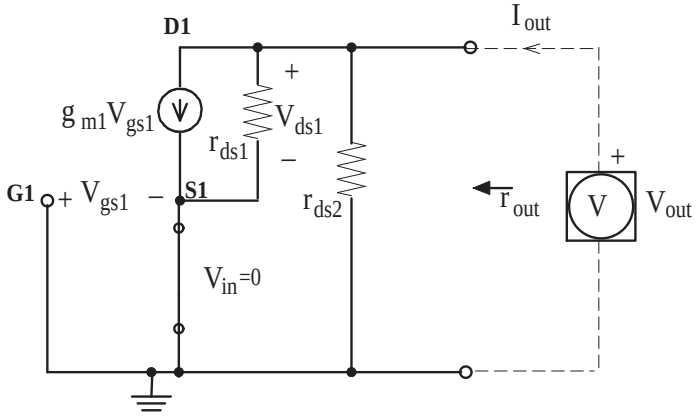

Figure 3: Small-signal equivalent circuit for determing r_{out}.

Apperently, from **Figure 3**, also $V_{gs1} = 0$ whereby $g_{m1}V_{gs1} = 0$, and so

$$\underline{\underline{r_{out} = r_{ds1}//r_{ds2} = \frac{r_{ds1}r_{ds2}}{r_{ds1} + r_{ds2}}}}$$

3. Noise in CMOS circuits

a) The ESSS is shown in **Figure ??**.

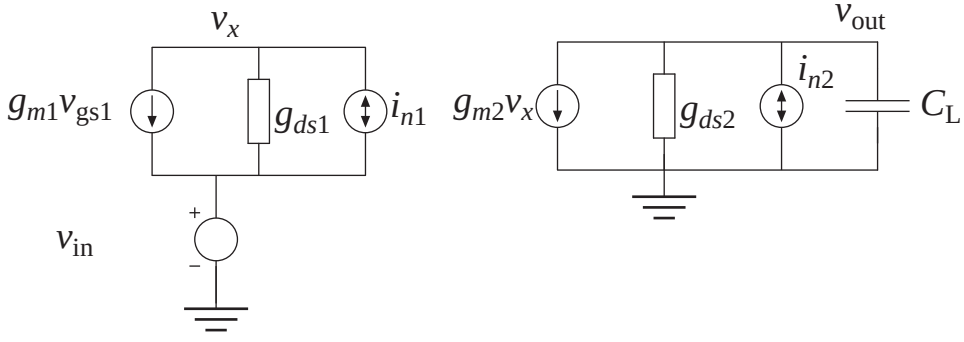

Figure 4: A noisy circuit.

We have to compute the transfer function from the drain-source of transistor M1 to the output, here denoted H_1, and from transistor M2 to the output, denoted H_2, and from V_{in} to the output, H.

The transfer functions are derived from the KCL equations

$$\begin{array}{c} g_{m1}(0 - v_{\text{in}}) + g_{ds1}(v_x - v_{\text{in}}) + i_{n1} = 0 \\ g_{m2}(v_x - 0) + (g_{ds2} + sC_L)v_{\text{out}} + i_{n2} = 0 \end{array} \tag{6}$$

Solving for v_x in the first equation results in

$$v_x = \frac{1}{g_{ds1}}[(g_{m1} + g_{ds1})v_{\text{in}} - i_{n1}] \tag{7}$$

Inserting into the second equation give the following transfer function

$$v_{\text{out}} = -\frac{1}{g_{ds2} + sC_L}(\frac{g_{m2}}{g_{ds1}}[(g_{m1} + g_{ds1})v_{\text{in}} - i_{\text{n1}}] + i_{\text{n2}}) \tag{8}$$

The transfer functions are determined by setting zeroing some of the input signals.

$$\begin{array}{c} H = \frac{v_{\text{out}}}{v_{\text{in}}} = -\frac{g_{m2}(g_{m1}+g_{ds1})}{g_{ds1}(g_{ds2}+sC_L)} \\ H_1 = \frac{v_{\text{out}}}{i_{n1}} = \frac{g_{m2}}{g_{ds1}(g_{ds2}+sC_L)} \\ H_2 = \frac{v_{\text{out}}}{i_{n2}} = -\frac{1}{g_{ds2}+sC_L} \end{array} \tag{9}$$

The spectral density of the output can be calculated as

$$S_{\text{out}}(f) = |H_1|^2 * i_{n1} + |H_2|^2 * i_{n2} \tag{10}$$

where $i_{ni} = \frac{8kT}{3}g_{mi} \forall i \in \{1, 2\}$.

Hence, the equivalent noise spectral density at the output is given by

$$S_{out}(f) = \frac{8kTg_{m2}}{3}|\frac{1}{g_{ds2} + j2\pi fC_L}|^2(1 + \frac{g_{m1}g_{m2}}{g_{ds1}^2}) \tag{11}$$

b) The input referred noise voltage can be obtain by dividing the output referred noise voltage by the squared magnitude of the transfer function from the input to the output, i.e., $|H|^2$.

This gives the answer

$$S_{in}(f) = \frac{8kT}{3g_{m2}}|\frac{g_{ds1}}{g_{m1} + g_{ds1}}|^2(1 + \frac{g_{m1}g_{m2}}{g_{ds1}^2}) \tag{12}$$

From this equation it is obvious that the input transistor generates more noise than the output transistor since $1 << g_{m1}g_{m2}/g_{ds1}^2$.

c) The SNR can be increased by decreasing the input-referred noise spectral density. This can for example be performed by increasing the transconductance g_{m1} of the input transistor, which can be done by increasing the biasing current or by increasing the relation W/L (W=width, L=length) of the transistor.

4. Switched Capacitor Circuit

a) The circuit in the two different clock phases is shown in **Figure ??**.

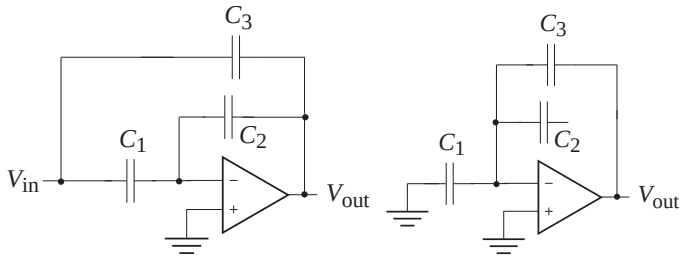

Figure 5: An SC circuit in clock phase 1 (to the left) and clock phase 2 (to the right).

Here, both the solution for exercise a) and c) is given. First, determine the reference directions of the charge on the capacitors. Here, we choose positive charge to the left of capacitor C_1 and to the right of C_2 and C_3. Express the capacitor charge at times t, $t+\tau$, and $t+2\tau$.

time t

$$\begin{aligned} q_1(t) &= C_1 * (V_{\text{in}}(t) - V_{\text{os}}) \\ q_2(t) &= C_2 * (V_{\text{out}}(t) - V_{\text{os}}) \\ q_3(t) &= C_3 * (V_{\text{out}}(t) - V_{\text{in}}(t)) \end{aligned} \tag{13}$$

time $t+\tau$

$$\begin{aligned} q_1(t+\tau) &= C_1 * (0 - V_{\text{os}}) \\ q_2(t+\tau) &= C_2 * (V_x(t+\tau) - V_{\text{os}}) \\ q_3(t+\tau) &= C_3 * (V_{\text{out}}(t+\tau) - V_{\text{os}}) \end{aligned} \tag{14}$$

time $t+2\tau$

$$\begin{aligned} q_1(t+2\tau) &= C_1 * (V_{\text{in}}(t+2\tau) - V_{\text{os}}) \\ q_2(t+2\tau) &= C_2 * (V_{\text{out}}(t+2\tau) - V_{\text{os}}) \\ q_3(t+2\tau) &= C_3 * (V_{\text{out}}(t+2\tau) - V_{\text{in}}(t+2\tau)) \end{aligned} \tag{15}$$

where V_x is the potential to the right of C_2. The charge conservation equations are

$$\begin{aligned} -q_1(t) - q_2(t) - q_3(t) &= -q_1(t+\tau) - q_2(t+\tau) - q_3(t+\tau) \\ -q_2(t) &= -q_2(t+\tau) \\ -q_1(t+\tau) - q_2(t+\tau) &= -q_1(t+2\tau) - q_2(t+2\tau) \end{aligned} \tag{16}$$

The second equations results in that $V_{\text{out}}(t) = V_x(t+\tau)$. Moreover, for the third equation, the following result is obtained.

$$\begin{aligned} -C_1(V_{\text{in}}(t+2\tau) - V_{\text{os}}) - C_2(V_{\text{out}}(t+2\tau) - V_{\text{os}}) = \\ C_1 V_{\text{os}} - C_2(V_{\text{out}}(t) - V_{\text{os}}) \Rightarrow \\ C_1 V_{\text{in}}(t+2\tau) + C_2 V_{\text{out}}(t+2\tau) = C_2 V_{\text{out}}(t) \end{aligned} \tag{17}$$

The first equation is not required in this case since this will only give the transfer function in clock phase 2 which is not what is required.

Performing the Z-transformation results in

$$V_{\text{out}}(z) = \frac{C_1}{C_2} \frac{z}{z-1} V_{\text{in}}(z) \tag{18}$$

Hence, the circuit is an accumulator and it is insensitive for offset voltages in the operational amplifier.

b) Capacitive parasitics in SC circuit arise in node connected to either a capacitor, amplifier or switch. In principle, each node in a circuit has an associated parasitic. **Figure ??** shows the parasitics in the circuit.

C_{pa} does not influence the transfer function since it is connected between the ideal input voltage source and ground. This input source can source/sink as much charge as required.

C_{pb} is charged in clock phase 1 by the ideal voltage source and discharge into ground. Hence, the transfer function is not affected.

C_{pc} is charged in clock phase 1 by the ideal voltage source and discharge into the sensitive virtual grounded node. Hence, the transfer function is affected by this parasitic.

C_{pd} connected between ground and virtual ground and thereby will not change the transfer function.

C_{pe} is connected to the output node what can source/sink as much charge as required.

C_{pf} is either connected to the output node or to a constant node. Hence, the transfer function is not affected.

All other parasitics are short circuited to ground and will thereby not change the transfer function. Thus, the circuit is sensitive to parasitics in that sense that the circuit's transfer function is changed due to the parasitic C_{pc}.

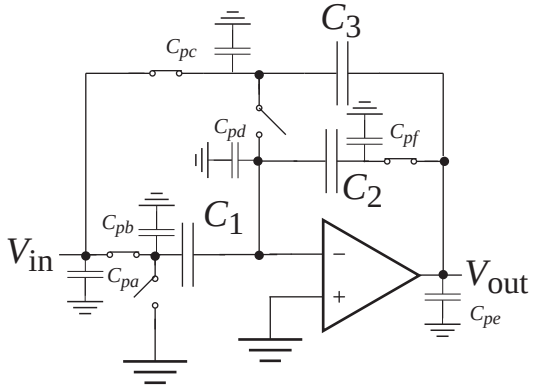

Figure 6: An SC circuit in clock phase 1 including capacitive parasitics.

5. A mixture of questions

a) Exercises a) and b) have very many solutions. The key point is to understand the difference between an operational amplifier and an operational transconductance amplifier. An operational amplifier has small output resistance and it has the possibility to drive load with low resistance. One solution can look like in **Figure ??**.

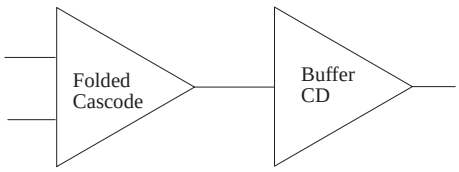

Figure 7: A common partitioning of an operational amplifier.

The Folded cascode amplifier has pmos input transistors to meet the CMR requirement and it has the following specification: $A_0 = 82$ dB, $f_u = 120$ MHz, SR= 80 V/μs, CMR= $[0.1 - 2.0]$ V, $P_{\text{diss}} = 7$ mW and OR= $[0.5 - 3.1]$V.

The buffer is a common drain amplifier with nmos transistors. The specification is: $A_0 = -1.9$ dB, $f_u = 200$ MHz, SR= 80 V/μs, $P_{\text{diss}} = 3$ mW and OR= $[0.3 - 2.3]$V, the CMR is not possible to define. However, the input swing must be at least 0.8 - 3.1 V which is not commonly a problem.

The operational transconductance amplifier has high output resistance and thereby it can only drive large load resistance.

Here, we only use a Folded cascode amplifier with pmos input devices and no buffer at the output. The Folded cascode amplifier will have following specification: $A_0 = 80$ dB, $f_u = 100$ MHz, SR= 80 V/μs, CMR= $[0.1 - 2.0]$ V, $P_{\text{diss}} = 10$ mW and OR= $[0.3 - 2.3]$V.

b) see a.

c) Tuning is performed by adjusting the time constants in active filters. This is required since the component values varies with the process parameters variations obtained in the manufacturing process. The time constants are determined by $1/RC$ in active RC filters. The resistances and capacitances varies commonly with about 20 - 50 %. These kind of variations is not acceptable in active filters.

The principle of tuning is as follows. Suitable filter parameters is measures (this can e.g., be the resonance frequency in a biquad, the cutoff frequency in the filter or the phase shift at a specific frequency). These measurements are compared with reference values and the difference is used to adjust the resistances or capacitances in the filter.

d) Benefits of fully differential circuit compared with single-ended circuits.

- Even-order harmonic distortion is ideally canceled.
- High noise rejection, i.e., increased PSRR and CMRR.
- No poles and zeros associated with the current mirrors in the differential to single-ended conversion.
- A little bit higher DC gain, unity-gain frequency, and phase margin.

The drawbacks are

- Common-mode stabilization is required to set the common-mode output voltage. This is commonly performed by a common-mode feedback circuit, CMFB.
- The design of a CMFB circuit is complicated especially if it should be a continuous-time circuit. These circuit typically reduce the output swing.