Correct (?) solutions to
Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	August 21, 2003
Time:	14 – 18
Max. no of points:	70; 40 from written test, 15 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Large-signal analysis

The circuit in Figure 1.1(a) is an analog circuits which can be a part of an opamp. In the exercise neglect the channel-length modulation.

a) Determine the output voltage, V_{out}, as a function of the input voltage, V_{in}, for the circuit shown in Figure 1.1(a). Assume that both transistors are saturated. Further, determine the DC gain of the circuit by using large-signal analysis.

The current through a transistor operating in the saturation region is given by

$$I_D = \alpha(V_{GS} - V_{TH})^2 \tag{1.1}$$

if the channel-length modulation is neglected. For the transistors M_1 and M_2 the current should be equal according to KCL. Hence,

$$I_{D1} = \alpha_1(V_{in} - V_{bias} - V_{TH1})^2 = \alpha_2(V_{out} - V_{TH2})^2 = I_{D2} \tag{1.2}$$

Solving for V_{out} yields

$$V_{out} = \sqrt{\frac{\alpha_1}{\alpha_2}}(V_{in} - V_{bias} - V_{TH1}) + V_{TH2} \tag{1.3}$$

which is the answer for this exercise. Further, the DC gain is derived as the derivative of the output voltage with respect to the input voltage when they are expressed in terms of large-signal quantities as in (1.3). Hence,

$$\frac{dV_{out}}{dV_{in}} = \sqrt{\frac{\alpha_1}{\alpha_2}} \tag{1.4}$$

the only way to increase the DC gain is to increase the size of the PMOS transistor and decrease the size of the NMOS transistor. This is for a first-order approximation of the performance of the circuit.

b) Assume that the transistor M_2 is replaces by a resistor, R, as is shown in Figure 1.1(b). Determine the output voltage as a function of the input

voltage, $V_{out} = f(V_{in})$. The input voltage ranges from zero to large input voltages, e.g., $V_{in} \gg V_{bias}$. In the graph denote the operation regions of transistor M_1.

For small input voltages below $V_{bias} + V_{TH1}$ the transistor is operating in the cut-off region. This means that the current through transistor M_1 is very small and can be considered zero. Hence, no voltage drop over the resistor replacing M_2 is the result which leads to zero volt at the output node.

Increasing the voltage above $V_{bias} + V_{TH1}$ results in a source-gate minus the threshold voltage smaller than the source-drain voltage and the transistor is operating in the saturation region. The output voltage is described as the resistance times the current through the transistor. Hence, in the saturation region the output voltage increases quadratically with the increase in the input voltage.

If we increase the input voltage even further, the source-drain voltage will be smaller than the source-gate voltage minus the threshold voltage which will lead that the transistor is operating in the linear region.In the linear region the current through the device will increase slower than in the saturation region. Hence, the output voltage increase rate will start to decrease. The output voltage as a function of the input voltage is shown in Figure 1.1.

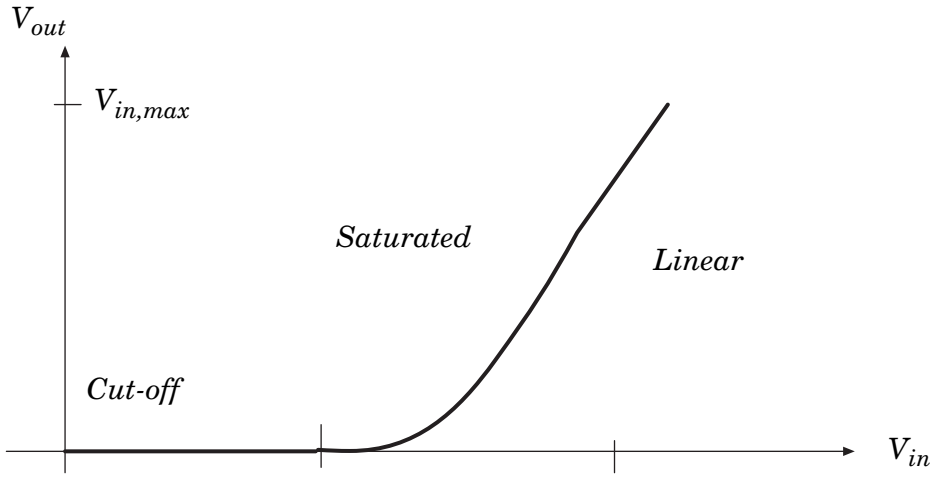

Figure 1.1 The output voltage as a function of the input voltage.

c) Determine the voltage for which the transistor M_1 switches from operating in the linear region to the saturation region in Figure 1.1(b). The answer should contain V_{bias} but not V_{out}.

The transition from saturated to the linear region appears when the source-drain voltage equals the source-gate voltage minus the threshold voltage. Hence,

$$V_{SD} = V_{in} - V_{out} = V_{in} - V_{bias} - V_{TH} = V_{SG} - V_{TH} \tag{1.5}$$

which can be simplified to

$$V_{out} = V_{bias} + V_{TH}. \tag{1.6}$$

Further, the output voltage is

$$V_{out} = RI_D \tag{1.7}$$

where

$$I_D = \alpha_1(V_{in} - V_{bias} - V_{TH})^2 . \tag{1.8}$$

Solving for V_{in} by combining Eq. (1.6) to Eq. (1.8) yields

$$V_{in} = \sqrt{\frac{V_{bias} + V_{TH}}{R\alpha_1}} + V_{bias} + V_{TH} \tag{1.9}$$

2. Small-signal analysis

A commonly used circuit in analog design is shown in Figure 2.1(a). In this exercise assume that all transistors are biased to operate in the saturation region.

a) Derive the transfer function, i.e., V_{out}/V_{in}, of the circuit shown in Figure 2.1(a). Do not neglect the bulk effects.

The small-signal model of the amplifier is shown in Figure 2.1.

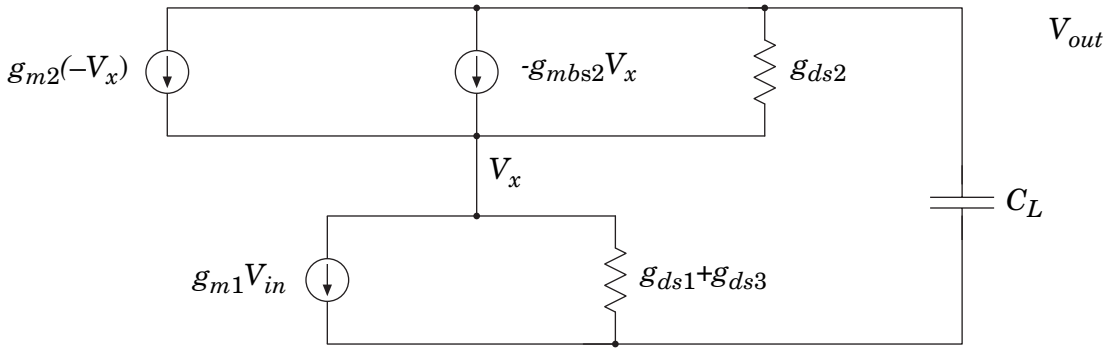

Figure 2.1 Small-signal model of the gain-boosted folded-cascode amplifier.

The transfer function can be derived by for example using nodal analysis in the nodes V_x and V_{out}.

$$g_{m1}V_{in} + V_x(g_{ds1} + g_{ds3}) + (g_{m2} + g_{mbs2})V_x + (V_x - V_{out})g_{ds2} = 0$$

$$(g_{m2} + g_{mbs2})V_x + (V_x - V_{out})g_{ds2} - V_{out}sC_L = 0$$

In the lowermost equation we can solve for V_x

$$V_x = \frac{g_{ds2} + sC_L}{g_{m2} + g_{msb2} + g_{ds2}} V_{out} . \tag{2.1}$$

Inserting this into the other equation and some simplifications yields

$$g_{m1}V_{in} + (g_{ds1} + g_{ds3})\frac{g_{ds2} + sC_L}{g_{m2} + g_{msb2} + g_{ds2}} V_{out} + sC_L V_{out} = 0$$

which is rewritten to

$-g_{m1}(g_{m2}+g_{msb2}+g_{ds2})V_{in} = (g_{ds1}+g_{ds3})g_{ds2}+sC_L(g_{ds1}+g_{ds3}+g_{m2}+g_{msb2}+g_{ds2})$.

The transfer function is given by

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}(g_{m2}+g_{msb2}+g_{ds2})}{(g_{ds1}+g_{ds3})g_{ds2}+sC_L(g_{ds1}+g_{ds3}+g_{m2}+g_{msb2}+g_{ds2})}$$

which is approximated to

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{\frac{(g_{ds1}+g_{ds3})g_{ds2}}{g_{m2}}+sC_L} \tag{2.2}$$

by assuming that $g_m \gg g_{mbs}$, $g_m \gg g_{ds}$.

b) Derive expressions for the DC gain, first pole, and the unity-gain frequency in terms of I, W, and L for the circuit shown in Figure 2.1(a). Neglect the influence of the bulk effect.

The DC gain is given by

$$A_0 = \frac{g_{m1}g_{m2}}{(g_{ds1}+g_{ds3})g_{ds2}} = \frac{\sqrt{\frac{W_1}{L_1}(I_1+I_3)}\sqrt{\frac{W_2}{L_2}I_1}}{\left(\frac{1}{L_1}(I_1+I_3)+\frac{1}{L_3}I_3\right)\frac{1}{L_2}I_1} = \sqrt{\frac{W_1L_1}{(I_1+I_3)+\frac{L_1}{L_3}I_3}}\sqrt{\frac{W_2L_2}{I_1}}.$$

The pole is expressed as

$$p_1 \approx \frac{(g_{ds1}+g_{ds3})g_{ds2}}{g_{m2}C_L} \approx \frac{\left(\frac{1}{L_1}(I_1+I_3)+\frac{1}{L_3}I_3\right)\frac{1}{L_2}I_1}{C_L\sqrt{\frac{W_2}{L_2}I_1}} = \frac{\left(\frac{1}{L_1}(I_1+I_3)+\frac{1}{L_3}I_3\right)}{C_L\sqrt{\frac{W_2L_2}{I_1}}}.$$

The unity-gain frequency is approximately given by

$$\omega_u \approx A_0p_1 \approx \frac{g_{m1}g_{m2}}{(g_{ds1}+g_{ds3})g_{ds2}}\frac{(g_{ds1}+g_{ds3})g_{ds2}}{g_{m2}C_L} = \frac{g_{m1}}{C_L} \propto \frac{\sqrt{\frac{W_1}{L_1}(I_3+I_1)}}{C_L}.$$

c) Determine the minimum output voltage that assures saturated transistors of the circuit shown in Figure 2.1(a).

The minimum output voltage is determined by the saturation voltage of both the transistors M_1 and M_2. Hence,

$$V_{out,\,min} = V_{DSAT1}+V_{DSAT2} = \sqrt{\frac{I_1+I_3}{\alpha_1}}+\sqrt{\frac{I_1}{\alpha_2}}. \tag{2.3}$$

d) Both the circuits shown in Figure 2.1 (a) and (b) has been designed and the sizes of the transistors are equally large. Compare these two

structures in terms of the minimum output voltage for equally large unity-gain frequency.

The unity-gain frequency of the cascoded transistor pairs can be determined from the unity-gain frequency of the special cascoded amplifier. The difference in the small-signal model is just the conductance g_{ds3} is not presented in the regular cascoded circuit. Hence, the unity-gain frequency is given by

$$\omega_u = \frac{g_{m1}}{C_L} \tag{2.4}$$

for both cases. However, the expressions of the g_{m1} for the two amplifiers are different. In the regular cascoded case the

$$g_{m1} = \sqrt{\frac{W_1 I_2}{L_1}} \tag{2.5}$$

while for the special cascoded amplifier it is given by

$$g_{m1} = \sqrt{\frac{W_1}{L_1}(I_1 + I_3)}\,. \tag{2.6}$$

In the minimum output swing for both circuits is given by the expressions

$$V_{out,\,min} = V_{DSAT1} + V_{DSAT2} = \sqrt{\frac{I_2}{\alpha_1}} + \sqrt{\frac{I_2}{\alpha_2}} \tag{2.7}$$

and Eq. (2.3) for the regular cascoded amplifier and the special cascoded amplifier, respectively. Hence, $I_1 + I_3 = I_2$ for the both circuit is have equally large unity-gain frequency, and diverting more current from I_1 to transistor M_3 in the special amplifier yields the same unity-gain frequency, but the minimum possible output voltage is decreased. This type of structure is good for low voltage applications and it is usually called current stealing techniques.

3. Noise Analysis

The circuit shown in Figure 3.1 is to be implemented in a CMOS process. The transistors are biased to operate in the saturation region and they generates thermal noise. Neglect the influence of the bulk effect. Further, also the resistor is generating thermal noise.

a) Compute the equivalent **output noise spectral density** caused by the thermal noise of the devices in the circuit shown in Figure 3.1.

The small-signal model of the circuit is shown in Figure 3.1. Typically, noise problems are solved using the formula

$$S_{out}(j\omega) = \sum \left|H_i(j\omega)\right|^2 S_i(j\omega)\,. \tag{3.1}$$

where $S_i(j\omega)$ is the spectral density of the ith noise source while $H_i(j\omega)$ is the transfer function from the noise source to the output node of the circuit.

Starting by solving the transfer function from the noise source of transistor M_1 to the output node. In this case is $V_{n2} = 0$. Using nodal analysis in the

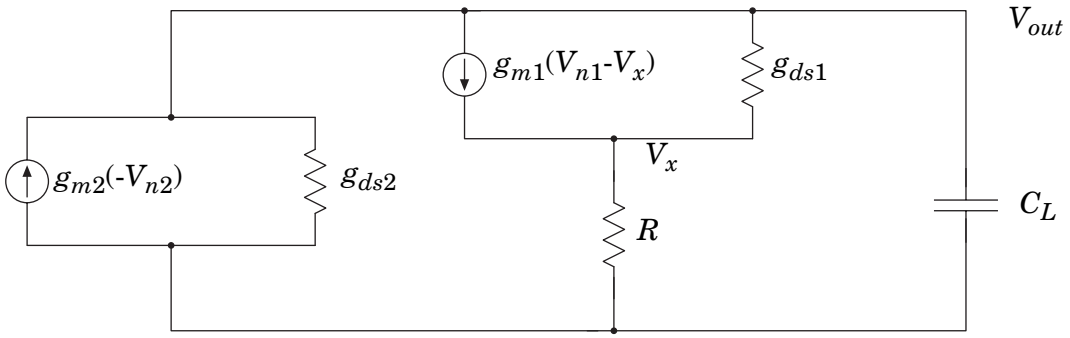

Figure 3.1 The small-signal model for the noisy circuit.

nodes V_x and V_{out} yields

$$g_{m1}(V_{n1}-V_x)+(V_{out}-V_x)g_{ds1}-V_xG\ =\ 0 \tag{3.2}$$

$$g_{m1}(V_{n1}-V_x)+(V_{out}-V_x)g_{ds1}+V_{out}(g_{ds2}+sC_L)\ =\ 0 \tag{3.3}$$

Solving this system of equation yields

$$H_1\ =\ \frac{V_{out}}{V_{n1}}\ =\ \frac{-g_{m1}G}{g_{ds2}(g_{ds1}+g_{m1})+G(g_{ds1}+g_{ds2})+sC_L(G+g_{m1}+g_{ds1})}$$

which has the DC gain of

$$A_{0H1}\ =\ \frac{-g_{m1}G}{g_{ds2}(g_{ds1}+g_{m1})+G(g_{ds1}+g_{ds2})} \tag{3.4}$$

and the pole is located at

$$p_{1H1}\ =\ \frac{g_{ds2}(g_{ds1}+g_{m1})+G(g_{ds1}+g_{ds2})}{C_L(G+g_{m1}+g_{ds1})}. \tag{3.5}$$

For the second noise source the nodal analysis equations is

$$g_{m1}(-V_x)+(V_{out}-V_x)g_{ds1}-V_xG\ =\ 0$$

$$g_{m1}(-V_x)+(V_{out}-V_x)g_{ds1}+V_{out}(g_{ds2}+sC_L)+g_{m2}V_{n2}\ =\ 0$$

which has the solution

$$H_2\ =\ \frac{V_{out}}{V_{n2}}\ =\ -\frac{g_{m2}(G+g_{ds1}+g_{m1})}{g_{ds2}(g_{ds1}+g_{m1})+G(g_{ds1}+g_{ds2})+sC_L(G+g_{m1}+g_{ds1})}$$

which has the DC gain of

$$A_{0H2}\ =\ -\frac{g_{m2}(G+g_{ds1}+g_{m1})}{g_{ds2}(g_{ds1}+g_{m1})+G(g_{ds1}+g_{ds2})} \tag{3.6}$$

and the same pole as for the other case.

For the resistor the noise model is a current source in parallel with the resistor. This yields the nodal analysis equations

$$g_{m1}(-V_x) + (V_{out} - V_x)g_{ds1} - V_x G + I_R = 0 \tag{3.7}$$

$$g_{m1}(-V_x) + (V_{out} - V_x)g_{ds1} + V_{out}(g_{ds2} + sC_L) = 0 \tag{3.8}$$

Solving for V_x in Eq. (3.8) and inserting it into Eq. (3.7) yields

$$H_R = \frac{V_{out}}{I_R} = -\frac{g_{m1} + g_{ds1}}{g_{ds2}(g_{ds1} + g_{m1}) + G(g_{ds1} + g_{ds2}) + sC_L(G + g_{m1} + g_{ds1})}$$

The output spectral noise density is

$$S_{out}(j\omega) = \left|H_1(j\omega)\right|^2 \frac{8kT}{3}\frac{1}{g_{m1}} + \left|H_2(j\omega)\right|^2 \frac{8kT}{3}\frac{1}{g_{m2}} + \left|H_R(j\omega)\right|^2 4kTG$$

b) How is the equivalent **input noise spectral density** and the DC gain effected if V_{bias} is decreased. Assume that all transistors remain in the saturation region.

The input-referred spectral density is the output-referred spectral density divided by the squared transfer function from the input to the output. In this case

$$S_{in}(j\omega) = \frac{\left|H_1(j\omega)\right|^2 \frac{8kT}{3}\frac{1}{g_{m1}} + \left|H_2(j\omega)\right|^2 \frac{8kT}{3}\frac{1}{g_{m2}} + \left|H_R(j\omega)\right|^2 4kTG}{\left|H_1(j\omega)\right|^2} \tag{3.9}$$

which yields

$$S_{in}(j\omega) = \frac{8kT}{3}\frac{1}{g_{m1}} + \frac{(g_{m2}(G + g_{ds1} + g_{m1}))^2}{(g_{m1}G)^2}\frac{8kT}{3}\frac{1}{g_{m2}} + \frac{(g_{m1} + g_{ds1})^2}{(g_{m1}G)^2}4kTG \tag{3.10}$$

This expression can be simplified to

$$S_{in}(j\omega) = \frac{8kT}{3}\frac{1}{g_{m1}} + \frac{(g_{m2}(G + g_{m1}))^2}{(g_{m1}G)^2}\frac{8kT}{3}\frac{1}{g_{m2}} + \frac{4kT}{G}. \tag{3.11}$$

Further, decreasing V_{bias} yields more current through the transistor and hence g_{mi} is increased. Which decreases the input-referred noise spectral density and the DC gain is decreased.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1 is shown in Figure. The input signal is sampled according to $V_{in}(t) = V_{in}(t + \tau)$.

a) Determine the transfer function, $V_{out}(z)/V_{in}(z)$, and plot the location of the possible poles and zeros in the z-plane for the circuit shown in Figure. Assume that the operational amplifier is ideal.

This exercise is solved using charge redistribution analysis. The reference directions are shown in Figure 4.1.

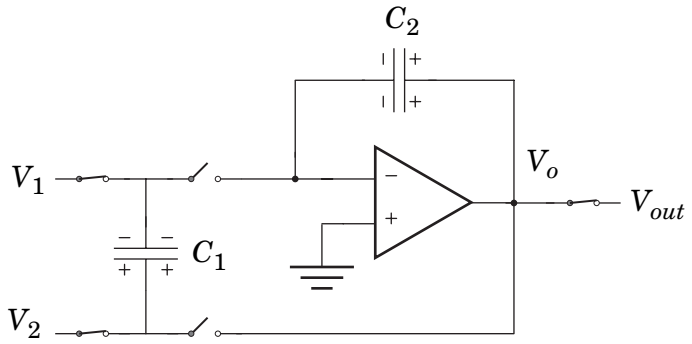

Figure 4.1 The switched-capacitor circuit with reference directions.

First we express the charges over all capacitors at times instances t, $t+\tau$, and $t+2\tau$.
$q_1(t) = C_1(V_2(t) - V_1(t))$, $q_2(t) = C_2(V_o(t) - 0)$.
At time $t+\tau$
$q_1(t+\tau) = C_1(V_o(t+\tau) - 0)$, $q_2(t+\tau) = C_2(V_o(t+\tau) - 0)$.
At time $t+2\tau$
$q_1(t+2\tau) = C_1(V_2(t+2\tau) - V_1(t+2\tau))$, $q_2(t+2\tau) = C_2(V_o(t+2\tau) - 0)$.

Charge conservation yields

$$q_1(t) + q_2(t) = q_1(t+\tau) + q_2(t+\tau) \tag{4.1}$$

and

$$q_2(t+\tau) = q_2(t+2\tau) \tag{4.2}$$

Further we know that $V_{out}(t) = V_{out}(t+\tau) = V_o(t)$.
Eq. (4.2) yields that the output voltage is constant between $t+\tau$ and $t+2\tau$.
Solving the charge conservation yields

$$C_1(V_2(t) - V_1(t)) + C_2V_o(t) = C_1V_o(t+\tau) + C_2V_o(t+\tau) \tag{4.3}$$

which is equal to

$$C_1(V_2(t) - V_1(t)) = (C_1 + C_2)V_o(t+2\tau) - C_2V_o(t). \tag{4.4}$$

Performing z-transformation yields

$$V_o(z)((C_1 + C_2)z - C_2) = C_1(V_2(z) - V_1(z)) \tag{4.5}$$

The output voltage is

$$V_{out}(z) = \frac{C_1}{C_1 + C_2}\frac{V_2(z) - V_1(z)}{z - \frac{C_2}{C_1 + C_2}} \tag{4.6}$$

which is a lossy accumulator, i.e., the pol is located at the positive real axis

in the z-plane with a magnitude smaller than one.

b) Is the circuit insensitive of capacitive parasitics. Motivate your answer carefully, $V_{out}(z) = f(V_1(z), V_2(z), V_{os})$.

No, the circuit is not insensitive to capacitive parasitics since the top plate of the capacitor C_1 is charged in the clock phase one and it will be discharged in clock phase two into the sensitive node. The transfer function will be

$$V_{out}(z) = \frac{1}{C_1 + C_2} \frac{C_1 V_2(z) - (C_1 + C_p) V_1(z)}{z - \frac{C_2}{C_1 + C_2}}. \tag{4.7}$$

c) The opamp exhibits both offset voltage and finite gain. Determine the output voltage as a function of the input and offset voltages.

The offset voltage is modelled as a voltage source in series with the positive node of the operational amplifier. The finite gain, A, yields that the negative node with the voltage V_x is varying compared to the output node according to

$$V_o = -V_x A \Rightarrow V_x = -V_o / A \tag{4.8}$$

for both clock phases.

The charge redistribution analysis yields

time t:

$$q_1(t) = C_1(V_2(t) - V_1(t)),$$

$$q_2(t) = C_2(V_o(t) - V_{os} - V_x(t)) = C_2\left(V_o(t)\left(1 + \frac{1}{A}\right) - V_{os}\right) \tag{4.9}$$

time $t + \tau$:

$$q_1(t + \tau) = C_1\left(V_o(t + \tau)\left(1 + \frac{1}{A}\right) - V_{os}\right)$$

$$q_2(t + \tau) = C_2\left(V_o(t + \tau)\left(1 + \frac{1}{A}\right) - V_{os}\right) \tag{4.10}$$

time $t + 2\tau$:

$$q_1(t + 2\tau) = C_1(V_2(t + 2\tau) - V_1(t + 2\tau))$$

$$q_2(t) = C_2(V_o(t + 2\tau) - V_{os} - V_x(t + 2\tau)) = C_2\left(V_o(t + 2\tau)\left(1 + \frac{1}{A}\right) - V_{os}\right).$$

The charge conservation equations are the same in exercise a).

$$q_1(t) + q_2(t) = q_1(t + \tau) + q_2(t + \tau) \tag{4.11}$$

and

$$q_2(t + \tau) = q_2(t + 2\tau) \tag{4.12}$$

Eq. (4.12) yields that the output voltage is constant between $t + \tau$ and

$t + 2\tau$. Solving the charge conservation yields

$$C_1(V_1(t) - V_2(t)) + C_2\left(V_o(t)\left(1 + \frac{1}{A}\right) - V_{os}\right) = (C_1 + C_2)\left(V_o(t + 2\tau)\left(1 + \frac{1}{A}\right) - V_{os}\right)$$

The transfer function after the z-transform is

$$V_{out}(z) = \frac{C_1}{(C_1 + C_2)\left(1 + \frac{1}{A}\right)} \frac{V_2(z) - V_1(z) + V_{os}}{z - \frac{C_2}{C_1 + C_2}}. \qquad (4.13)$$

Hence, the gain of the circuit is increase by the finite gain of the opamp.

5. A mixture of questions

a) Derive the power supply rejection ratio, PSRR, from V_{DD} for the circuit shown in Figure. How can the PSRR be improved by 3 dB?

The small-signal model of the circuit where the power supply voltage is assumed to be noisy is shown in Figure 5.1.

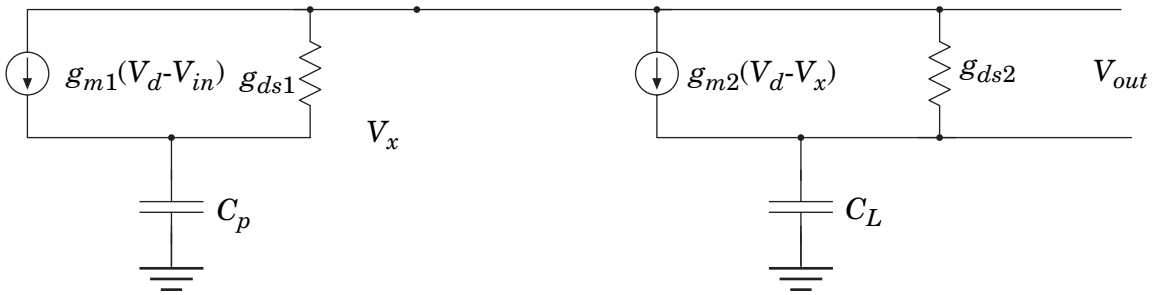

Figure 5.1 The small-signal model of the circuit where V_d is the contribution of the variations at the power supply voltage line.

The PSRR is the ratio between the transfer function from the input to the output compared to the transfer function from the power supply voltage to the output node.

The transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{ds1} + sC_p} \frac{g_{m2}}{g_{ds2} + sC_L} \qquad (5.1)$$

since V_d is zero. The transfer function from the power supply voltage to the V_x node is given by (assuming the $V_{in} = 0$)

$$\frac{V_x}{V_d} = \frac{g_{m1} + g_{ds1}}{g_{ds1} + sC_L} \qquad (5.2)$$

and the transfer function is than

$$\frac{V_{out}}{V_d} = \frac{g_{ds1}g_{ds2} - g_{m1}g_{m2} + sC_p(g_{m2} + g_{ds2})}{(g_{ds1} + sC_p)(g_{ds2} + sC_L)}. \qquad (5.3)$$

Hence, the power supply voltage is determined as

$$PSRR_p = \frac{V_{out}}{V_{in}} / \frac{V_{out}}{V_d} = \frac{g_{m1}g_{m2}}{g_{ds1}g_{ds2} - g_{m1}g_{m2} + sC_p(g_{m2} + g_{ds2})} \qquad (5.4)$$

which can be simplified to

$$PSRR_p = -\frac{1}{1 - s\frac{C_p}{g_{m1}}} \qquad (5.5)$$

Hence, the gain from the input node is about the same as the gain from the power supply voltage to the output node.

b) Why is it important to matched the two input transistors in a differential gain stage? Explain three approaches for improving the matching of two transistors.

It is important to have matched transistors in a differential pair in order to both suppress the distortion terms as well as decreasing the offset voltage of the circuit. Matching can be performed in several ways. Increasing the width times the length value is good for matching. Further, lay out the transistors close to each other using the same orientation. Try to decrease the effects of the gradients on the silicon, by utilizing symmetry, for example interdigitized or common centroid layout styles.

c) Determine the minimum output voltage of the circuit shown in Figure. Express it in terms of relevant design parameters.

The minimum output voltage is found by starting at the ground node and finding all paths to the output node. Starting from transistor M_1 yields the path

$$V_{GS1} + V_{GS2} - V_{GS4} - V_{GS6} + V_{DSAT6} = \sqrt{\frac{I_{in}}{\alpha_1}} + V_{TH1} + \sqrt{\frac{I_{in}}{\alpha_2}} + V_{TH2} - \left(\sqrt{\frac{I_{D3}}{\alpha_4}} + V_{TH4}\right) - V_{TH6}. \qquad (5.6)$$

Through the transistor M_3

$$V_{DSAT3} - V_{GS6} + V_{DSAT6} = \sqrt{\frac{I_{D3}}{\alpha_3}} - V_{TH6} \qquad (5.7)$$

while the path from M_5 yields

$$V_{DSAT5} + V_{DSAT6} = \sqrt{\frac{I_{out}}{\alpha_5}} + \sqrt{\frac{I_{out}}{\alpha_6}}. \qquad (5.8)$$

However, which path which is the limiting one depends on the currents in the branches. However, the path through M_3 is not the limiting factor. Hence, the minimum output node voltage is described by

$$V_{out,\,min} = max\left\{\sqrt{\frac{I_{in}}{\alpha_1}} + V_{TH1} + \sqrt{\frac{I_{in}}{\alpha_2}} + V_{TH2} - \left(\sqrt{\frac{I_{D3}}{\alpha_4}} + V_{TH4}\right) - V_{TH6}, \sqrt{\frac{I_{out}}{\alpha_5}} + \sqrt{\frac{I_{out}}{\alpha_6}}\right\}$$