Correct (?) solutions to
Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	May 28, 2003
Time:	8 - 12
Max. no of points:	70; 40 from written test, 15 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Large-signal analysis

The circuit in the Figure is a commonly used structure when designing analog circuits. In all following exercises assume that transistor M1 is biased in saturation. Also assume that the *W/L* ratio of transistor M2 is X times larger than that of transistor M1, i.e., $W_2/L_2 = XW_1/L_1$.

a) Derive the output voltage as a function of the factor X, i.e., $V_{out} = f(X)$, when transistor M2 is saturated. Express the output voltages in terms of the current I_0 and tr2ansistor design parameters, but not voltages other than the power supply voltage.

The ratio between the current when both transistors are operating in the saturation region is

$$\frac{I_{M2}}{I_{M1}} = \frac{\alpha_2(V_{SG}-V_{TH2})^2}{\alpha_1(V_{SG}-V_{TH1})^2} = \frac{X\alpha_1(V_{SG}-V_{TH})^2}{\alpha_1(V_{SG}-V_{TH})^2} = X \qquad (1.1)$$

The output voltage is then given by

$$V_{out}(X) = RI_{M2} = RI_0X \qquad (1.2)$$

b) Derive the output voltage as a function of the factor X, i.e., $V_{out} = g(X)$, when transistor M2 is operating in the linear region. Express the output voltages in terms of the current I_0 and transistor design parameters, but not voltages other than the power supply voltage.

In the linear region the current is given by

$$I_{M2,\,linear} = X\beta_1\left[(V_{SG}-V_{TH})V_{SD,2}-\frac{V_{SD,2}^2}{2}\right] \qquad (1.3)$$

while $V_{out}(X) = RI_{M2,\,linear}$.

The transistor M_1 is still in saturation, hence, the current is given by

$$I_{M1} = \alpha_1(V_{SG}-V_{TH})^2. \qquad (1.4)$$

Solving for $V_{SG}-V_{TH}$ yields

$$V_{SG} - V_{TH} = \sqrt{\frac{I_{M1}}{\alpha_1}} = \sqrt{\frac{I_0}{\alpha_1}}. \tag{1.5}$$

Further, $V_{SD,2} = V_{DD} - V_{out}$. The Eq. (1.3) can be reformulated to

$$\frac{V_{out}}{R} = X\beta_1\left[\sqrt{\frac{I_0}{\alpha_1}}(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})^2}{2}\right] \tag{1.6}$$

which is

$$2V_{out}\left(\frac{1}{RX\beta_1} - \sqrt{\frac{I_0}{\alpha_1}} - V_{DD}\right) + V_{DD}^2 - 2\sqrt{\frac{I_0}{\alpha e_1}}V_{DD} + V_{out}^2 = 0$$

where

$$V_{out} = -\left(\frac{1}{RX\beta_1} - \sqrt{\frac{I_0}{\alpha_1}} - V_{DD}\right) \pm \sqrt{\left(\frac{1}{RX\beta_1} - \sqrt{\frac{I_0}{\alpha_1}} - V_{DD}\right)^2 + V_{DD}^2 - 2\sqrt{\frac{I_0}{\alpha_1}}V_{DD}}$$

This is simplified to

$$V_{out} = \sqrt{\frac{I_0}{\alpha_1}} + V_{DD} - \frac{1}{RX\beta_1} \pm \sqrt{\left(\frac{1}{RX\beta_1}\right)^2 - \frac{1}{RX\beta_1}\left(\sqrt{\frac{I_0}{\alpha_1}} + V_{DD}\right) + 2\frac{I_0}{\alpha_1}}$$

c) Determine for which value of X transistor M2 switches from operating in the saturation region to the linear region.

The value X for which the circuit switches from operating in the saturation region to the linear region is when its source-drain voltage equals the source-gate voltage minus the threshold voltage, i.e.,

$$V_{SD,2} = V_{SG} - V_{TH} \tag{1.7}$$

The source-drain voltage is given by

$$V_{SD,2} = V_{DD} - RI_{M2} \tag{1.8}$$

while the gate-source voltage depends on I_0 according to

$$I_0 = I_{M1} = \alpha_1(V_{SG} - V_{TH})^2 \tag{1.9}$$

which yields

$$V_{SG} - V_{TH} = \sqrt{\frac{I_0}{\alpha_1}} \tag{1.10}$$

Hence,

$$V_{DD} - RI_{M2} = \sqrt{\frac{I_0}{\alpha_1}} \tag{1.11}$$

and

$$V_{DD} - RI_0 X = \sqrt{\frac{I_0}{\alpha_1}}. \tag{1.12}$$

Solving for the X factor

$$X = \frac{-\sqrt{\frac{I_0}{\alpha_1}} + V_{DD}}{RI_0}. \tag{1.13}$$

d) Sketch the output voltage as a function of the X, i.e., $V_{out} = h(X)$, for $X > 0$.

For small values of X there will be a small current through the transistor and thereby small voltage drop over the resistor and, hence, the transistor will be in the saturation region. The output voltage will follow Eq. (1.2) for small values of X. Increasing the value of X yields that the transistor will start to operate in the linear region (for X larger than Eq. (1.13)). The output voltage will then increase in a slower fashion according to the equations in (b). Hence, the output voltage will in principle look like Figure 1.1.

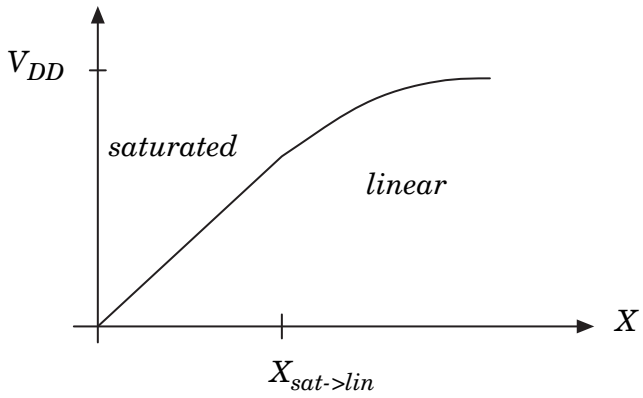

Figure 1.1 The output voltage as a function of the X factor.

2. Small-signal analysis

The circuit in the Figure is going to be implemented in a CMOS process. The parasitic of interest is the gate-source capacitor. The feedback amplifier has a gain of $-A$ where A is positive and $A \gg 1$. Further, assume that $C_{GS,2} \ll C_L$.

a) Derive the transfer function of the circuit shown in Figure. Do not neglect the bulk effects.

The small-signal model of the amplifier is shown in

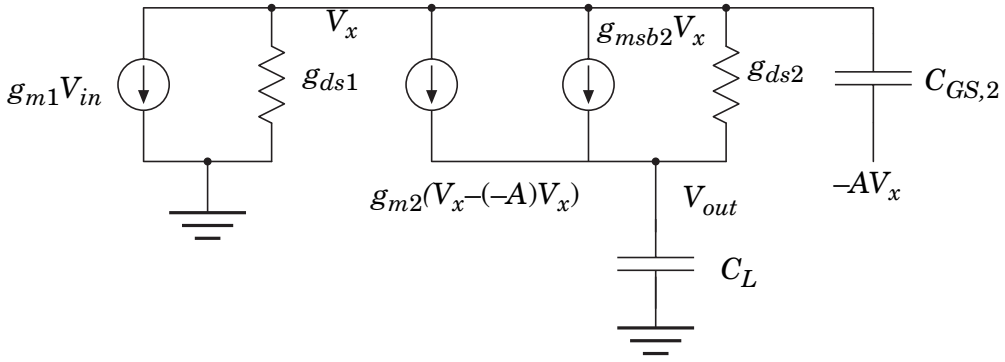

Figure 2.1 Small-signal model of the gain-boosted folded-cascode amplifier.

The transfer function can be derived by using for example nodal analysis in the nodes V_x and V_{out}.

$$g_{m1}V_{in} + V_x g_{ds1} + g_{m2}(V_x - (-A)V_x) + g_{msb2}V_x + (V_x - V_{out})g_{ds2} + sC_{GS,2}(1-(-A))V_x = 0$$

$$g_{m2}(V_x - (-A)V_x) + g_{msb2}V_x + (V_x - V_{out})g_{ds2} - V_{out}sC_L = 0$$

From the lowermost equation we can solve for V_x

$$V_x = \frac{g_{ds2} + sC_L}{g_{m2}(1+A) + g_{msb2} + g_{ds2}}V_{out} \qquad (2.1)$$

Inserting this into the other equation yields

$$g_{m1}V_{in} + (g_{ds1} + g_{m2}(1+A) + g_{msb2} + g_{ds2} + sC_{GS,2}(1+A))V_x = V_{out}g_{ds2}$$

which is simplified to

$$g_{m1}V_{in} = -\left((g_{ds1} + sC_{GS,2}(1+A))\frac{g_{ds2} + sC_L}{g_{m2}(1+A) + g_{msb2} + g_{ds2}} + sC_L\right)V_{out}.$$

The transfer function is given by

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}(g_{m2}(1+A) + g_{msb2} + g_{ds2})}{(g_{ds1} + sC_{GS,2}(1+A))(g_{ds2} + sC_L) + sC_L(g_{m2}(1+A) + g_{msb2} + g_{ds2})}$$

b) Derive expressions for the DC gain, first pole, second pole, possible zeros, and the unity-gain frequency in terms of I_1, I_2, W_1, W_2, L_1, and L_2. Neglect the influence of the bulk effect.

The DC gain is after some approximations

$$A_0 = -\frac{g_{m1}g_{m2}(1+A)}{g_{ds1}g_{ds2}} \approx -\frac{g_{m1}g_{m2}A}{g_{ds1}g_{ds2}} \propto$$

$$\frac{A\sqrt{\frac{W_1}{L_1}(I_1-I_2)}\sqrt{\frac{W_2}{L_2}I_2}}{\frac{1}{L_1}(I_1-I_2)\frac{1}{L_2}I_2} = A\sqrt{\frac{W_1L_1}{(I_1-I_2)}}\sqrt{\frac{W_2L_2}{I_2}}. \qquad (2.2)$$

The poles are found by some small approximation which holds if the poles are separated which is the case here. The denominator of a two pole system is

$$\left(1+\frac{s}{p_1}\right)\left(1+\frac{1}{s_p}\right) = 1+s\left(\frac{1}{p_1}+\frac{1}{p_2}\right)+\frac{s^2}{p_1p_2} \approx 1+\frac{s}{p_1}+\frac{s^2}{p_1p_2}$$

Using this approximation and identifying this with the transfer function yields

$$p_1 \approx \frac{g_{ds1}g_{ds2}}{C_L(g_{m2}(1+A)+g_{msb2}+g_{ds2}+g_{ds1})+g_{ds2}C_{GS,2}(1+A)} \approx \frac{g_{ds1}g_{ds2}}{C_Lg_{m2}A} \propto$$

$$\frac{\frac{1}{L_1}(I_1-I_2)\frac{1}{L_2}I_2}{AC_L\sqrt{\frac{W_2}{L_2}I_2}} = \frac{(I_1-I_2)}{L_1AC_L}\sqrt{\frac{I_2}{W_2L_2}}$$

while the second pole is given by

$$p_2 \approx \frac{C_L(g_{m2}(1+A)+g_{msb2}+g_{ds2}+g_{ds1})+g_{ds2}C_{GS,2}(1+A)}{C_{GS,2}C_L} \approx \frac{g_{m2}A}{C_{GS,2}} \propto \frac{A\sqrt{\frac{W_2}{L_2}I_2}}{C_{GS,2}}$$

.

The unity-gain frequency is approximately given by

$$\omega_u \approx A_0p_1 \approx -\frac{g_{m1}g_{m2}A}{g_{ds1}g_{ds2}}\frac{g_{ds1}g_{ds2}}{C_Lg_{m2}A} = \frac{g_{m1}}{C_L} \propto \frac{\sqrt{\frac{W_1}{L_1}(I_1-I_2)}}{C_L}.$$

c) How is the phase margin effected if the bias current I_1 is increased, i.e., how is the phase effected at the unity-gain frequency of the circuit?

Increasing the current I_1 yields larger unity-gain frequency. The second pole is not effected by the increase I_1. Hence, increased unity-gain frequency yields larger contribution to the phase which yields a lower phase margin.

3. Noise Analysis

An operational amplifier is used in a CMOS circuit. Assume that the OPamp is ideal.

a) Derive the transfer function of the circuit shown in Figure.

Using nodal analysis in the node where all capacitors are connected, V_x, and at the positive input node of the operational amplifier, V_p. V_p equals V_{out} since the operational amplifier is ideal.

$$sC_1(V_x - V_{in}) + sC_2V_x + sC_3(V_x - V_p) + G_2(V_x - V_{out}) = 0$$

$$sC_3(V_x - V_p) - G_1V_p = 0.$$

From the second equation we have that

$$V_x = \frac{G_1 + sC_3}{sC_3}V_p = \frac{G_1 + sC_3}{sC_3}V_{out}$$

inserting this into the first equation yields

$$(s(C_1 + C_2 + C_3) + G_2)\frac{G_1 + sC_3}{sC_3}V_{out} - sC_1V_{in} - (sC_3 + G_2)V_{out} = 0$$

Hence, the transfer function is then

$$\frac{V_{out}}{V_{in}} = \frac{sC_1sC_3}{(s(C_1 + C_2 + C_3) + G_2)G_1 + s(C_1 + C_2)sC_3}$$

which is simplified to

$$\frac{V_{out}}{V_{in}} = \frac{s^2C_1C_3}{G_1G_2 + s(C_1 + C_2 + C_3)G_1 + s^2(C_1 + C_2)C_3}$$

b) Derive the equivalent thermal output noise spectral density of the circuit. Assume that the operational amplifier is noiseless. The resistors generates thermal noise according to $V_R^2 = 4kTR$.

The noise sources can either be a voltage noise source or a current noise source. In this case we use a current noise source (but in principle it is not any difference to use a voltage noise source). The current noise source has the spectral density equal to

$$I_R^2 = \frac{4kT}{R}. \tag{3.1}$$

In order to compute the equivalent output noise spectral density generated by the resistors we need to compute the transfer functions from the noise sources to the output of the filter (circuit). Then the transfer functions are computed the total equivalent output noise spectral density is given by

$$V_{out}^2 = |H_{R1}|^2I_{R1}^2 + |H_{R2}|^2I_{R2}^2 \tag{3.2}$$

Setting up the same equation as for finding the transfer function but using the current noise sources as the input signal and the input signal, V_{in}, is zeroed yields the following transfer functions

$$H_{R1} = -\frac{G_2 + s(C_1 + C_2 + C_3)}{G_1G_2 + s(C_1 + C_2 + C_3)G_1 + s^2(C_1 + C_2)C_3} \qquad (3.3)$$

and

$$H_{R2} = -\frac{sC_3}{G_1G_2 + s(C_1 + C_2 + C_3)G_1 + s^2(C_1 + C_2)C_3}. \qquad (3.4)$$

Hence, the equivalent output noise spectral density is

$$V_{out}^2 = \frac{G_2^2 + \omega^2(C_1 + C_2 + C_3)^2}{(G_1G_2 - \omega^2(C_1 + C_2)C_3)^2 + \omega^2(C_1 + C_2 + C_3)^2G_1^2}\frac{4kT}{R_1} + \frac{\omega^2C_3^2}{(G_1G_2 - \omega^2(C_1 + C_2)C_3)^2 + \omega^2(C_1 + C_2 + C_3)^2G_1^2}\frac{4kT}{R_2}.$$

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase1 is shown in Figure. The input signal is sampled according to $V_{in}(t) = V_{in}(t + \tau)$. Express the output voltage, $V_{out}(z)$, for clock phase 1 of the switched capacitor circuit shown in Figure. Assume that the OTA is ideal.

This exercise is solved using charge redistribution analysis. The reference directions are shown in Figure 4.1.

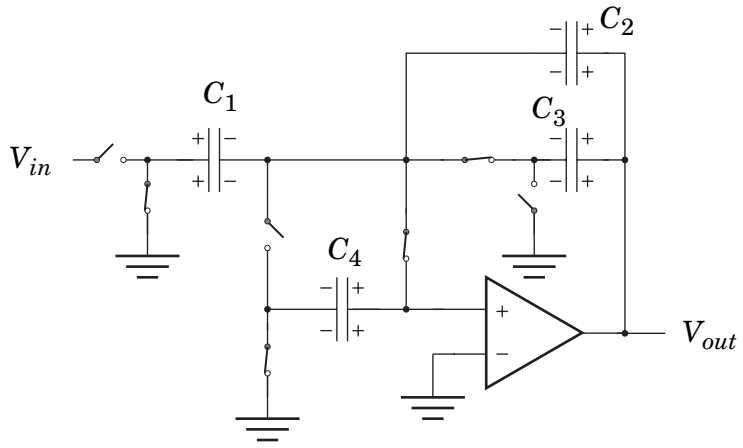

Figure 4.1 The switched-capacitor circuit with reference directions.

First we express the charges over all capacitors at times instances t, $t + \tau$, and $t + 2\tau$.

$q_1(t) = C_1(0 - 0)$,
$q_2(t) = C_2(V_{out}(t) - 0)$,
$q_3(t) = C_3(V_{out}(t) - 0)$,
$q_4(t) = C_4(0 - 0)$.

At time $t + \tau$

$q_1(t + \tau) = C_1(V_{in}(t + \tau) - V_x(t + \tau))$,
$q_2(t + \tau) = C_2(V_{out}(t + \tau) - V_x(t + \tau))$,
$q_3(t + \tau) = C_3(V_{out}(t + \tau) - 0)$,
$q_4(t + \tau) = C_4(0 - V_x(t + \tau))$.

At time $t + 2\tau$

$q_1(t + 2\tau) = C_1(0 - 0)$,
$q_2(t + 2\tau) = C_2(V_{out}(t + 2\tau) - 0)$,
$q_3(t + 2\tau) = C_3(V_{out}(t + 2\tau) - 0)$,
$q_4(t + 2\tau) = C_4(0 - 0)$.

Charge conservation yields

$$-q_1(t + 2\tau) - q_2(t + 2\tau) - q_3(t + 2\tau) + q_4(t + 2\tau) = -q_1(t + \tau) - q_2(t + \tau) - q_3(t + \tau) + q_4(t + \tau) \quad (4.1)$$

and

$$-q_1(t + \tau) - q_2(t + \tau) - q_4(t + \tau) = -q_1(t) - q_2(t) - q_4(t) \quad (4.2)$$

and

$$q_4(t + \tau) = q_4(t). \quad (4.3)$$

The transfer function is found using the above equations. V_x is solved from Eq. (4.3)

$$C_4(0 - V_x(t + \tau)) = C_4(0 - 0) \quad (4.4)$$

which yields that $V_x(t + \tau) = 0$. Inserting the charges into Eq. (4.1) and Eq. (4.2) yields

$$-(C_2 + C_3)V_{out}(t + 2\tau) = -C_1V_{in}(t + \tau) - (C_2 + C_3)V_{out}(t + \tau)$$

and

$$-C_1V_{in}(t + \tau) - C_2V_{out}(t + \tau) = -C_2V_{out}(t)$$

Eliminating $V_{out}(t + \tau)$ from the two above equations yields

$$-(C_2 + C_3)V_{out}(t + 2\tau) = -C_1V_{in}(t + \tau) - \frac{C_2 + C_3}{C_2}(C_2V_{out}(t) - C_1V_{in}(t + \tau))$$

which can be reformulated into

$$(C_2 + C_3)V_{out}(t + 2\tau) - (C_2 + C_3)V_{out}(t) = -C_1V_{in}(t + \tau) + \frac{C_2 + C_3}{C_2}C_1V_{in}(t + \tau)$$

We know that the input signal is sampled at t, $t + 2\tau$, $t + 4\tau$ and so on, hence, $V_{in}(t + \tau) = V_{in}(t)$.

$$(C_2 + C_3)(V_{out}(t + 2\tau) - V_{out}(t)) = \frac{C_1C_3}{C_2}V_{in}(t)$$

further, the sampling period is $T = 2\tau$.

$$(C_2 + C_3)(V_{out}(t + T) - V_{out}(t)) = \frac{C_1C_3}{C_2}V_{in}(t)$$

Performing Z-transformation yields

$$(C_2 + C_3)(z-1)V_{out}(z) = \frac{C_1 C_3}{C_2} V_{in}(z).$$

This results in the following transfer function

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1 C_3}{C_2(C_2 + C_3)} \frac{1}{z-1} \tag{4.5}$$

which is an accumulator.

5. A mixture of questions

a) You have designed and fabricated a digital-to-analog converter with 62dB SNR, where the noise power is dominated by the quantization noise. The application requires 86dB SNR. How can you increase the SNR of the data converter?

Increasing the number of effective bits in a data converter is usually performed using oversampling. This is possible if the input signal frequency is small so that it is possible to clock the data converter with as high sampling frequency as required. Oversampling has the benefits of spreading the quantization noise power over larger frequency range than for a nyquist range data converter. By applying a filter to filter out the signal band of interest the quantization noise is lowered which results in increased SNR, i.e., higher effective resolution is obtained. In order to further increase the effective number of bits in the data converter we can apply noise shaping to the converter. This means that the signal transfer function is not effected while the quantization noise is attenuated in the signal range of interest while it is amplified in the signal range which is not of concern.

b) Derive expressions for the common-mode and the output ranges of the circuit shown in Figure in terms of currents, I_{D5} and I_{D3}, and transistor parameters.T he amplifier circuit is symmetric with respect to the transistor sizes, i.e., $W_1/L_1 = W_2/L_2$ and so on.

The minimum input voltage in order to assure that all transistors are operating in the saturation region is

$$V_{in,min} = V_{ds,sat,3} + V_{sd,sat,1} - V_{sg1} = \sqrt{\frac{I_{D3}}{\alpha_3}} - V_{T1}.$$

The maximum input voltage for saturated transistors is

$$V_{in,max} = V_{DD} - V_{sd,sat,5} - V_{sg1} = V_{DD} - \sqrt{\frac{I_{D5}}{\alpha_5}} - \sqrt{\frac{I_{D5}}{2\alpha_1}} - V_{T1}.$$

The common-mode range is $CMR = [V_{in,min}, V_{in,max}]$.

The minimum output voltage to assure saturated transistors is

$$V_{out,min} = V_{ds,sat,4} + V_{ds,sat,7} = \sqrt{\frac{I_{D3}}{\alpha_4}} + \sqrt{\frac{I_{D3} - I_{D5}/2}{\alpha_7}}$$

and the maximum output voltage is

$$V_{out,\,max} = min\{V_{DD} - V_{sg11} - V_{sd,\,sat,\,9},\, V_{DD} - V_{sd,\,sat,\,10} - V_{sg8} + V_{sg9} - V_{sd9}\}$$

$$V_{out,\,max} = V_{DD} - \sqrt{\frac{I_{D3} - I_{D5}/2}{\alpha_{11}}} - V_{T11} - \sqrt{\frac{I_{D3} - I_{D5}/2}{\alpha_{9}}}$$

Hence, the output range is $OR = [V_{out,\,min},\, V_{out,\,max}]$.

c) A three terminal switch, Figure(a), is realized with two PMOS devices, Figure(b), in an SC circuit. The gates of the transistors are connected to the clocks ϕ_1 and ϕ_2, respectively. The waveforms for two different types of 2-phase clocks are shown in Figure(c) and (d), where ϕ_1 is solid and ϕ_2 is dashed. Which of these two 2-phase clocks ((c) or (d)) should be used in order to guarantee a good operation of the SC circuit. Motivate your answer carefully

(c) is the correct operation since otherwise both of the switches will be on at the same time which is not the desired operation. Hence, we like to have non-overlapping clocks in order to guarantee good operation.