Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	August 22, 2002
Time:	8 - 12
Max. no of points:	70; 40 from written test, 15 for project, and 15 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Basic building block

From the basics of the transistor we know that where are three different operation regions; cut-off, linear or triode region and saturation region. In the cut-off region is the $V_{gs} < V_{TH}$ and this occurs when $V_{in} > V_{bias} - V_{TH}$. when we decreases the input voltage slightly below the cut-off region the transistor will start to operate in the saturation region, since $V_{DS} > V_{GS} - V_{TH}$. A further decreased input voltage will result in a transistor operating in the linear region.

When the transistor is operating in the cut-off region very small current will flow through the transistor and thereby the output voltage will be very close to V_{DD}.

Decreasing the input voltage will result in a transistor in the saturation region. Hence the current is increased quadratically with respect to the gate source voltage while increase with respect to the drain source voltage, if it is increased. In principle will the current increase in square fashion.

Further decreased input voltage will result in a transistor in the linear region and thereby a linear increased current through the transistor and thereby through the resistor. So the output voltage will decrease towards zero in a linear way.

b) The maximum input voltage of have a transistor that is operating in the saturation region is $V_{in} = V_{bias} - V_{TH}$. Higher input voltage will result in a transistor operating in the cut-off region.

To compute the minimum voltage for saturation we need to set up some equation and solve them.

The current through the transistor when it is operating in the saturation region is defined as:

$$I_D = \alpha(V_{bias} - V_{in} - V_{TH})^2 \qquad (1.1)$$

if the channel length modulation is ignored. The current through the resistor is expressed as

$$I_R = \frac{V_{DD} - V_{out}}{R} \tag{1.2}$$

We know that the current through both these components must be equal. Furthermore, we know that $V_{DS} \geq V_{GS} - V_{TH}$ which give the following equation since we are at the edge of the saturation region.

$$V_{out} - V_{in} = V_{bias} - V_{in} - V_{TH} \tag{1.3}$$

Combining Eq. (1.1) and Eq. (1.3) together with Eq. (1.2) yields

$$\alpha(V_{out} - V_{in})^2 = \frac{V_{DD} - V_{out}}{R} \tag{1.4}$$

solving this second order equation gives the input voltage

$$V_{in} = V_{out} \pm \sqrt{\frac{V_{DD} - V_{out}}{R\alpha}} \tag{1.5}$$

Hence, the input voltage must be in the interval of

$$V_{out} \pm \sqrt{\frac{V_{DD} - V_{out}}{R\alpha}} < V_{in} < V_{bias} - V_{TH} \tag{1.6}$$

which can be rewritten using Eq. (1.3) according to

$$V_{bias} - V_{TH} \pm \sqrt{\frac{V_{DD} - V_{bias} + V_{TH}}{R\alpha}} < V_{in} < V_{bias} - V_{TH} \tag{1.7}$$

It is obvious that the plus sign is a false solution.

2. Small signal analysis

The minimum voltages at each node of the circuit are

$$V_{out,\,min} = max\{V_{dsat1} + V_{dsat2},\, V_{gs3} + V_{dsat2},\, V_{dsat3} - V_{gs2} + V_{ds2}\} =$$

$$V_{gs3} + V_{dsat2} = V_{TH3} + \sqrt{\frac{I_{bias2}}{\alpha_3}} + \sqrt{\frac{I_{bias1}}{\alpha_2}}$$

$$V_{x,\,min} = V_{gs3} = V_{TH3} + \sqrt{\frac{I_{bias2}}{\alpha_3}}$$

$$V_{y,\,min} = V_{x,\,min} + V_{gs2} = V_{TH3} + \sqrt{\frac{I_{bias2}}{\alpha_3}} + V_{TH2} + \sqrt{\frac{I_{bias1}}{\alpha_2}}$$

b) To compute the noise from the substrate to the output node we need to compute the transfer function from each transistors substrate contact to the output. Starting from a small signal model of the circuit shown in fig.xxxx The transfer functions from the bulk of transistor M_1 M_2 are computed using nodal analysis in nodes V_x, V_{out}, and V_y.

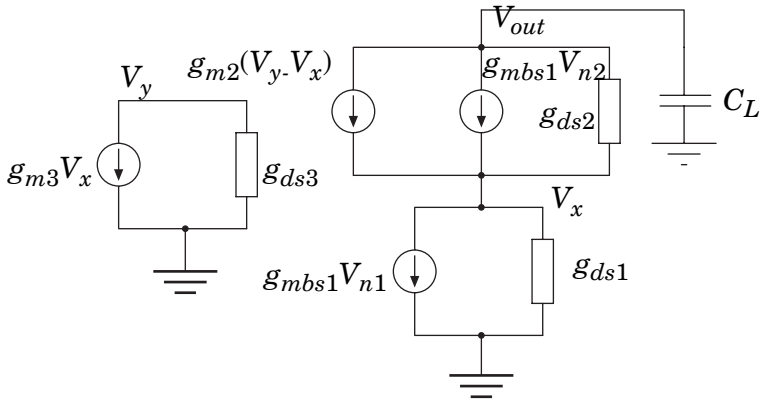

Figure 2.1 The small signal model of the circuit.

$$g_{mbs1}V_{n1} + V_x g_{ds1} + g_{m2}(V_y - V_x) - g_{mbs2}V_{n2} - (V_{out} - V_x)g_{ds2} = 0$$

$$g_{m2}(V_y - V_x) - g_{mbs2}V_{n2} - (V_{out} - V_x)g_{ds2} - V_{out}sC_L = 0$$

$$g_{m3}V_x + V_y g_{ds3} = 0$$

The equation in the bottom is rearranged to

$$V_y = \left(-\frac{g_{m3}}{g_{ds3}}\right)V_x \tag{2.1}$$

Solving the above equation directly or by identifying that the last three terms in the first equation is equal to minus the first two ones gives an expression of according to

$$V_x = -\left(\frac{g_{mbs1}}{g_{ds1}}V_{n1} + V_{out}sC_L\right) \tag{2.2}$$

Inserting Eq. (2.1) and Eq. (2.2) into the first equation gives after some manipulations

$$V_{out} = -\frac{g_{ds1}g_{mbs2}V_{n2} - g_{mbs1}\left(\left(1 + \frac{g_{m3}}{g_{ds3}}\right)g_{m2} + g_{ds2}\right)V_{n1}}{g_{ds1}g_{ds2} + sC_L\left(g_{ds1} + g_{ds2} + g_{m2}\left(1 + \frac{g_{m3}}{g_{ds3}}\right)\right)}$$

Which can be approximated by setting the term with s equal to

$$sC_L\left(g_{ds1} + g_{ds2} + g_{m2}\left(1 + \frac{g_{m3}}{g_{ds3}}\right)\right) \approx sC_L\frac{g_{m3}}{g_{ds3}}g_{m2} \tag{2.3}$$

Hence, the transfer functions are given by

$$H_1 = \frac{V_{out}}{V_{n1}} = -\frac{g_{ds3}g_{mbs1}}{g_{ds1}g_{ds2}g_{ds3} + sC_L g_{m3}g_{m2}}\left(\left(1 + \frac{g_{m3}}{g_{ds3}}\right)g_{m2} + g_{ds2}\right)$$

$$H_2 = \frac{V_{out}}{V_{n2}} = -\frac{g_{ds1}g_{ds3}g_{mbs2}}{g_{ds1}g_{ds2}g_{ds3} + sC_L g_{m3}g_{m2}}$$

The equivalent output noise spectrum is then given by:

$$S_{out} = (|H_1|^2 + |H_2|^2)S_{sub} \tag{2.4}$$

To minimize the equivalent output noise the transistor with the largest value of the transfer function must be shielded. In this case M_1 must be shielded.

3. An amplifier in a context

The transfer function is found by using KCL at the negative input terminal of the amplifier.

$$(V_{in} - V_n)G_1 + (V_{out} - V_n)sC_1 = 0 \tag{3.1}$$

Furthermore, the output voltage of the amplifier is expressed as

$$V_{out} = (V_p - V_n)A(s) = A(s)(0 - V_n) = -\frac{A_0}{1 + \frac{s}{p_1}}V_n \tag{3.2}$$

Combining Eq. (3.1) and Eq. (3.2) and eliminating V_n yields the following transfer function.

$$\frac{V_{out}}{V_{in}} = -\frac{G_1}{sC_1 + (sC_1 + G_1)\frac{1 + \frac{s}{p_1}}{A_0}} = -\frac{A_0}{1 + s\left(\frac{C_1(1 + A_0)}{G_1} + \frac{1}{p_1}\right) + s^2\frac{C_1}{p_1 G_1}}$$

In the design we know that $C_1R_1 > 1/p_1$ which yields that $C_1(1 + A_0)R_1 \gg 1/p_1$ since an operational amplifier has large gain. This leads to that the poles of the closed loop system can be extracted from the expression above.

$$p_I \approx \frac{G_1}{C_1(1 + A_0)} \approx \frac{G_1}{A_0 C_1} \tag{3.3}$$

and

$$p_{II} \approx \frac{A_0 C_1}{G_1}\frac{p_1 G_1}{C_1} = A_0 p_1 \approx \omega_u \tag{3.4}$$

by using the approximation that

$$\left(1+\frac{s}{p_I}\right)\left(1+\frac{s}{p_{II}}\right)=1+s\left(\frac{1}{p_I}+\frac{1}{p_{II}}\right)+\frac{s^2}{p_I p_{II}}\approx 1+\frac{s}{p_I}+\frac{s^2}{p_I p_{II}}$$

and identify with the expression for the transfer function. The DC gain of the circuit is equal to the DC gain of the open loop amplifier.

b) The phase of the closed loop circuit is defined as

$$\phi = -\text{atan}\frac{Im\{H(j\omega)\}}{Re\{H(j\omega)\}} = -\text{atan}\,Q \tag{3.5}$$

This means that a Q-value of 100 yields a phase of $\tan\phi = -Q$.

The phase is defined as

$$\phi = -\text{atan}\left(\frac{\omega}{p_I}\right)-\text{atan}\left(\frac{\omega}{p_{II}}\right)\approx -\frac{\pi}{2}-\text{atan}\left(\frac{\omega}{p_{II}}\right) \tag{3.6}$$

Since the first pole is located at very low frequencies.

We also know that

$$\tan(a+b) = \frac{\cos a\sin b+\cos b\sin a}{\cos a\cos b-\sin a\sin b} \tag{3.7}$$

Using this fact yields the following expression for the Q value

$$Q = -\tan\phi = -\tan\left(-\frac{\pi}{2}-\text{atan}\left(\frac{\omega}{p_{II}}\right)\right) =$$

$$\frac{\cos\text{atan}\left(\frac{\omega}{p_{II}}\right)}{\sin\text{atan}\left(\frac{\omega}{p_{II}}\right)} = \frac{1}{\tan\left(\text{atan}\left(\frac{\omega}{p_{II}}\right)\right)} = \frac{p_{II}}{\omega} \tag{3.8}$$

The minimum value of the quantity is when the frequency is as large as possible. The Q-value should be at least 100 for the frequency interval of 100kHz to 2MHz. The minimum value of $p_{II} = 100\omega = 2\pi\cdot 200 Mrad/s$ to achieve a minimum Q value of 100 in the frequency range of 100kHz to 2MHz.

4. Switched capacitor circuit

A switched capacitor circuit in clock cycle 1 is shown in the figure.

a) Derive the transfer function for the clock cycle 1 of the switched capacitor circuit, i.e., $V_{out}(z)/V_{in}(z)$. Assume that the OTA is ideal.

The circuit in Figure 4.1 shows the circuit for both clock cycles.

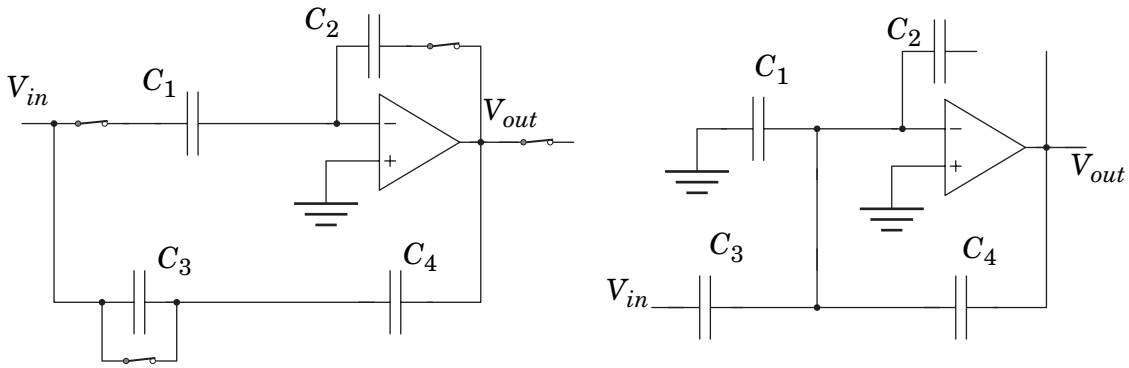

Figure 4.1 The SC circuit in both clock phases. Left ϕ_1, Right ϕ_2.

To compute the transfer function for the circuit charge redistribution analysis is used.

For clock cycle 1, ϕ_1, at time t

$q_1(t) = C_1(V_{in}(t) - 0)$; $q_2(t) = C_2(V_{out}(t) - 0)$; $q_3(t) = 0$;
$q_4(t) = C_4(V_{out}(t) - V_{in}(t))$

For clock cycle 2, ϕ_2, at time $t + \tau$

$q_1(t + \tau) = 0$; $q_2(t + \tau) = q_2(t)$;
$q_3(t + \tau) = C_3(V_{in}(t + \tau) - 0)$ $q_4(t + \tau) = C_4(V_{out}(t + \tau) - 0)$

The charge on the plates of capacitor C_2 will be unchanged since it is not connected on both terminals during clock phase 2.

For clock cycle 1, ϕ_1, at time $t + 2\tau = t + T$:

$q_1(t + 2\tau) = C_1(V_{in}(t + 2\tau) - 0)$; $q_2(t + 2\tau) = C_2(V_{out}(t + 2\tau) - 0)$;
$q_3(t + 2\tau) = 0$ $q_4(t + 2\tau) = C_4(V_{out}(t + 2\tau) - V_{in}(t + 2\tau))$

The charge conservation equations are

$$q_1(t) + q_2(t) + q_3(t) + q_4(t) = q_1(t + \tau) + q_2(t + \tau) + q_3(t + \tau) + q_4(t + \tau)$$

$$q_1(t + \tau) + q_2(t + \tau) = q_1(t + 2\tau) + q_2(t + 2\tau)$$

Inserting the charges into the lower one of the equations above gives the following expression

$$0 + C_2 V_{out}(t) = C_1 V_{in}(t + 2\tau) + C_2 V_{out}(t + 2\tau)$$

Perform Z transformation on the expression gives

$$-C_1 z V_{in}(z) = C_2(z - 1)V_{out}(z)$$

The transfer function is then

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2}\frac{z}{z-1} = -\frac{C_1}{C_2}\frac{1}{1-z^{-1}} \qquad (4.1)$$

It is a inverting accumulator

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully.

The circuit with parasitic capacitors are shown in

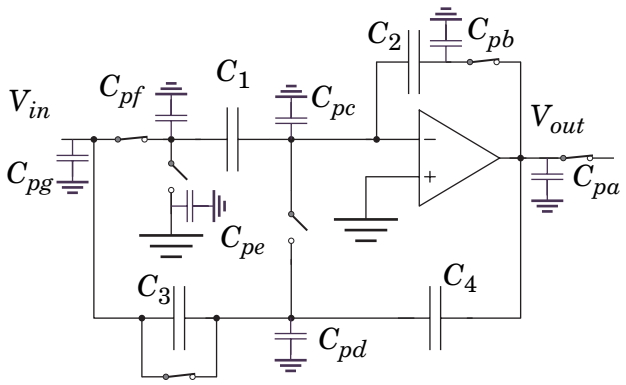

Figure 4.2 The SC circuit with parasitics capacitors

C_{pa} is connected to the ideal output of the OPamp and ground and thereby not changing the transfer function.

C_{pb} Charged by the output of the operational amplifier in clock cycle 1 and does not discharge during clock cycle 2. Not changing the transfer function.

C_{pc} is connected between the virtual ground and ground and thereby not changing the transfer function.

C_{pd} is charged by the input voltage during clock cycle 1 and discharged during clock cycle 2 into the virtual ground and thereby changing the transfer function.

C_{pe} is connected with both terminal to ground and not changing the transfer function

C_{pf} Connected between ground and the input voltage or ground and ground so it will be charged in clock cycle 1 and discharged to ground in clock cycle 2. Hence, not affecting the transfer function.

C_{pg} Charged by the input source and discharged to ground and thereby not changing the transfer function.

The circuit is sensitive to parasitics since the value of the parasitic capacitor C_{pd} will be a part of the over all transfer function if they are included in the computation of the transfer function.

c)

An offset voltage is modelled as a voltage source at the positive input of the amplifier. The voltage source will have the value of V_{os}.

Performing the charge redistribution analysis gives:

For clock cycle 1, ϕ_1, at time t

$q_1(t) = C_1(V_{in}(t) - V_{os})$; $q_2(t) = C_2(V_{out}(t) - V_{os})$; $q_3(t) = 0$;
$q_4(t) = C_4(V_{out}(t) - V_{in}(t))$

For clock cycle 2, ϕ_2, at time $t + \tau$

$q_1(t + \tau) = -C_1 V_{os}$; $q_2(t + \tau) = q_2(t)$;
$q_3(t + \tau) = C_3(V_{in}(t + \tau) - V_{os})$ $q_4(t + \tau) = C_4(V_{out}(t + \tau) - V_{os})$

The charge on the plates of capacitor C_2 will be unchanged since it is not connected on both terminals during clock phase 2.

For clock cycle 1, ϕ_1, at time $t + 2\tau = t + T$:

$q_1(t+2\tau) = C_1(V_{in}(t+2\tau) - V_{os})$; $q_2(t+2\tau) = C_2(V_{out}(t+2\tau) - V_{os})$;
$q_3(t+2\tau) = 0$ $q_4(t+2\tau) = C_4(V_{out}(t+2\tau) - V_{in}(t+2\tau))$
The charge conservation equations are

$$q_1(t) + q_2(t) + q_3(t) + q_4(t) = q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) + q_4(t+\tau)$$

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau)$$

Inserting the charges into the lower one of the equations above gives the following expression
$-C_1V_{os} + C_2(V_{out}(t) - V_{os}) =$
$C_1(V_{in}(t+2\tau) - V_{os}) + C_2(V_{out}(t+2\tau) - V_{os})$
Here we can see that the V_{os} can be cancelled. Hence, the transfer function is the same in exercise a.

5. A mixture of questions

a)

Accurate matching is achieved if we are using unit sized elements or elements with at least the same area or perimeter ration. Furthermore, the area to perimeter for the unit sized capacitors should be as large as possible.

Using common-centroid layout techniques makes the capacitor array less sensitive to temperature gradient and slow oxide thickness variations.

Another important point is to ensure that the neighborhood of each capacitor is equal. This is done by adding dummy capacitor around the capacitor array.

Matching of components depends of the distance of the devices. Hence, a structure with as short maximum distance is desired.

b)

The process technology can make it impossible to have two different voltages at the bulk of two transistors, as our case (M1, M2 and M5).

It is not possible to connect the bulk of transistor M1 and M2 to the substrate if we are not using an p-well in a p-substrate process. It comes from the fact that there is low resistance between the substrate contacts of the three transistors.

It is possible to implement this amplifier in n-substrate and the twin well process but not the n-substrate and P-well process.

c)

The positive PSRR is found by adding an ac source at the positive power supply line and compute the transfer function to the output. By taking the absolute value and dividing the transfer function from the input to the output with the transfer function from the positive power supply to the output we achieve the positive PSRR.

The transfer function from the input to the output is given by

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}} \tag{5.1}$$

The transfer function from the positive power supply to the output is given by

$$\frac{V_{out}}{V_{ps}} = \frac{g_{m2} + g_{ds2}}{g_{ds1} + g_{ds2}} \tag{5.2}$$

Hence, the positive PSRR equals

$$pPSRR = \frac{g_{m1}}{g_{m2} + g_{ds2}} \tag{5.3}$$

6. Extra exercise

NOTE: This exercise is only for the students that have taken the course before 2002 and not handed in three assignments during the course.

a)Draw the small signal scheme for the amplifier. Do not forget the most important parasitics.

The small signal scheme will look like the one shown in Figure 6.1. $C_{p1} \approx C_{gs3} + C_{gs4}$ and $C_1 \approx C_{gs6}$.

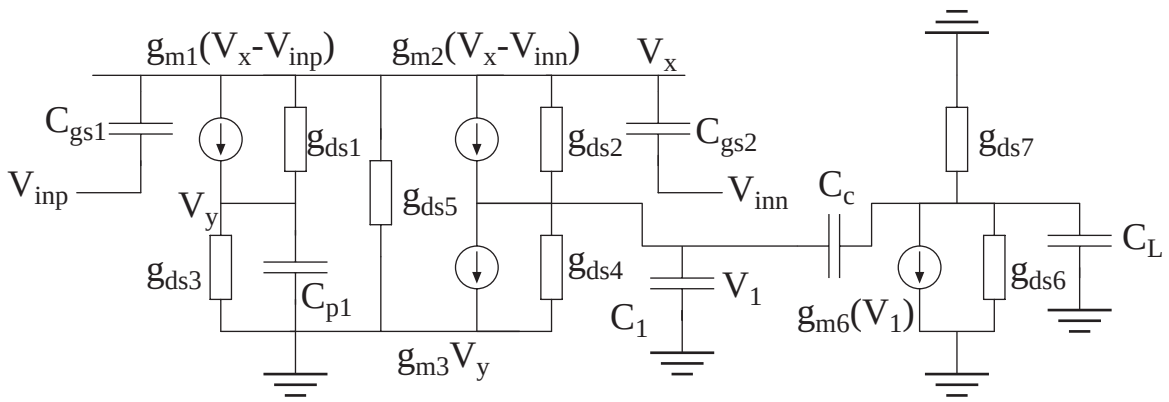

Figure 6.1 Small signal schematic with parasitics.

b) Derive the gain, poles, and zeros of the amplifier. Motivate all the approximations you are doing.

The first approximation come from the fact that C_{p1} is much smaller than C_c and C_L since the output node is often connected to many other stages and thereby is it large. The C_c is often even larger than C_L and $W_6 » W_3 = W_4$. Furthermore, the output resistance of transistor M5 is assumed to be very large which means that the g_{ds5} disappears at the same time as V_x can be considered small signal ground. The ESSS of the differential gain stage is simplified to the one shown in Figure 6.2.

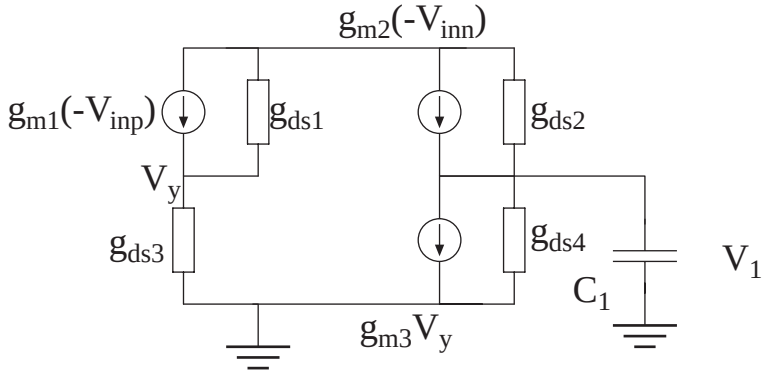

Figure 6.2 Simplified ESSS for the differential gain stage.

Nodal analysis in node V_y and V_1 gives

$$g_{m1}V_{inp} + V_y(g_{ds1} + g_{ds3}) = 0 \tag{6.1}$$

$$g_{m2}V_{inn} + V_1(g_{ds2} + g_{ds4} + sC_L) + g_{m3}V_y = 0 \tag{6.2}$$

Solving for V_y in Eq. (6.1) and inserting it in Eq. (6.2) give the transfer function from the input to the output.

$$V_1 = \frac{1}{g_{ds2} + g_{ds4}}\left(g_{m1}\frac{g_{m4}}{g_{m3} + g_{ds3} + g_{ds1}}V_{inp} - g_{m2}V_{inn}\right) \approx$$

$$\frac{g_{m2}}{g_{ds2} + g_{ds4}}(V_{inp} - V_{inn})$$

The approximation step comes from the fact the $g_{m3} \gg g_{ds1} + g_{ds3}$ together with the matching between the transistors M1-M2 and M3-M4.

The differential gain stage can be simplified to the first part of Figure 6.3

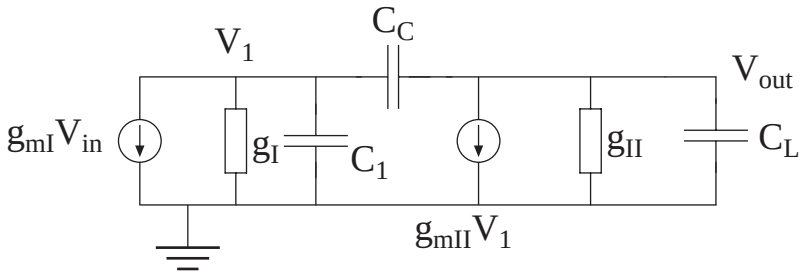

Figure 6.3 Simplified ESSS for the two stage amplifier

where

$$g_{mI} = g_{m2}$$

$$g_I = g_{ds2} + g_{ds4}$$

$$g_{mII} = g_{m6}$$

$$g_{II} = g_{ds6} + g_{ds7}$$

The second part of the ESSS comes from the common source gain stage at the output of the OTA.

Use nodal analysis to the left and right of the compensation capacitor gives the following equations.

$$g_{mI}(V_{inp} - V_{inn}) + V_1(g_I + sC_I) + sC_c(V_1 - V_{out}) = 0 \quad (6.3)$$

$$g_{mII}V_1 + V_{out}(g_{II} + sC_L) + (V_{out} - V_1)sC_c = 0 \quad (6.4)$$

The transfer function can be found by combining Eq. (6.3) and Eq. (6.4).

$$\frac{V_{out}}{V_{inp} - V_{inn}} = \frac{g_{mI}(g_{mII} - sC_c)}{g_I g_{II} + s(g_I(C_L + C_c) + g_{II}(C_I + C_c) + C_c g_{mII}) + s^2 C_L C_c} \quad (6.5)$$

We can now determine the DC-gain, poles, and zeros directly from the transfer function.

$$A_0 = \frac{g_{mI}g_{mII}}{g_I g_{II}}$$

$$p_1 \approx \frac{g_I g_{II}}{g_{mII} C_c}$$

$$p_2 \approx \frac{g_I}{C_c} + \frac{g_I + g_{II} + g_{mII}}{C_L} + \frac{C_I g_{II}}{C_c C_L} \approx \frac{g_{mII}}{C_L} \approx \frac{\sqrt{2\mu C_{ox}\frac{W_6}{L_6} I_{D6}}}{C_L}$$

$$z_1 = -\left(\frac{g_{mII}}{C_c} \approx \frac{\sqrt{2\mu C_{ox}\frac{W_6}{L_6} I_{D6}}}{C_C} \right)$$

c) Determine two ways to increase the unity-gain frequency of the amplifier. What will happen to the phase margin, common-mode range, and the DC voltage at node x?

The unity-gain frequency of the amplifier with separated poles is

$$w_u = A_o p_1 = \frac{g_{mI}}{C_c} \approx \frac{\sqrt{2\mu_n C_{ox} \frac{W_2}{L_2} I_{D2}}}{C_c}$$

There are three different ways to increase the unity-gain frequency.

1) Increase W_2/L_2.

This will only increase the unity-gain not the second pole or the zero and thereby the phase margin will decrease, since the unity-gain frequency will be closer to the second pole.

The common-mode range is

$$\sqrt{\frac{I_{D2}}{\alpha_3}} + V_{T3} - V_{T1}, V_{DD} - \sqrt{\frac{I_{D2}}{2\alpha_5}} - \sqrt{\frac{I_{D2}}{\alpha_1}} - V_{T1} \tag{6.6}$$

Increasing W_2/L_2 will increase α_1 and thereby the common-mode range will increase.

If we start by looking at the drain current expression for a saturated transistor:

$$I_D = K\frac{W_2}{L_2}(V_{sg2} - V_{T2})^2(1 + \lambda V_{sd2}) \tag{6.7}$$

Furthermore, we know that I_D will constant while W_2/L_2 will increase at the same time as V_{g2} and V_{d2} will be constant. This results in a decreased V_x voltage.

2) Increase the current through transistor M2, I_{D2}.

This increment will not change the phase margin of the amplifier, since the unity-gain frequency will increase as fast as both the second pole as the zero.

The common-mode range will decrease and the voltage at node x will increase since V_{g2} will be constant and V_{d2} will increase.

3) Decrease C_c

The phase margin will decrease since p2 will lay still while z_1 will increase.

The common-mode range and V_x will be constant.