Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	June 3, 2002
Time:	8 - 12
Max. no of points:	70; 50 from written test, 15 for project, and 5 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Basic building block

In an operational amplifier a buffer at the output is needed to increase the output conductance of the amplifier and thereby be able to drive resistive loads. The buffer is shown in the figure. In this exercise neglect the influence of the channel length modulation.

a) Derive a large signal expression for the output voltage as a function of the input voltage. Assume that all transistors are operating in the saturation region.

We know that the large signal current equation in saturation for an NMOS transistor when we have ignored without channel length modulation is given by

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2 \tag{1.1}$$

From the KCL we know that the current through both transistors must be equal. This gives the following equation.

$$\frac{\mu C_{ox}}{2}\frac{W_1}{L_1}(V_{in} - V_{out} - V_{T1})^2 = \frac{\mu C_{ox}}{2}\frac{W_2}{L_2}(V_{bias} - V_{T2})^2 \tag{1.2}$$

Taking the square root of both sides gives

$$\sqrt{\frac{\mu C_{ox}}{2}\frac{W_1}{L_1}}(V_{in} - V_{out} - V_{T1}) = \sqrt{\frac{\mu C_{ox}}{2}\frac{W_2}{L_2}}(V_{bias} - V_{T2}) \tag{1.3}$$

Solving for V_{out} gives

$$V_{out} = V_{in} - \sqrt{\frac{W_2}{L_2} \diagup \frac{W_1}{L_1}}(V_{bias} - V_{T2}) - V_{T1} \tag{1.4}$$

b) Express the first pole as a function of the bias voltage, V_{bias}.

To find a small signal expression for the first pole we need to draw the equivalent small signal model for the amplifier. Here we do not either use the channel length modulation and thereby the output conductance of the transistor is zero, i.e., infinite output resistance. The small signal equivalent is shown in Figure 1.1.

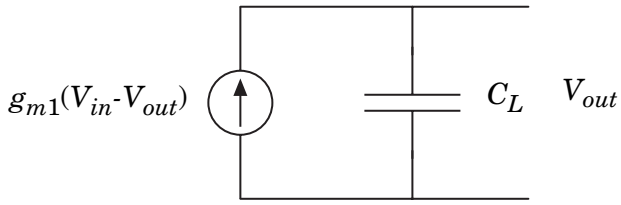

Figure 1.1 The equivalent small signal model for the common drain amplifier.

The transfer function of the amplifier is found by using the nodal analysis which yields

$$g_{m1}(V_{in} - V_{out}) - sC_L V_{out} = 0. \tag{1.5}$$

The transfer function is found to be

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m1} + sC_L} = \left(\frac{1}{1 + \frac{s}{g_{m1}/C_L}} \right) \tag{1.6}$$

The first pole is given by

$$p_1 = \frac{g_{m1}}{C_L} \tag{1.7}$$

When the channel length modulation is ignored the transconductance value is given by

$$g_{m1} = \sqrt{2\mu C_{ox} \frac{W_1}{L_1} I_D} \tag{1.8}$$

The current through transistor M_1 is given by the current source transistor M_2. The current generated by M_2 is

$$I_D = \frac{\mu C_{ox}}{2} \frac{W_2}{L_2} (V_{bias} - V_{T2})^2 \tag{1.9}$$

Combining (1.8) and (1.9) give the expression for the first pole as a function of the bias voltage according to

$$p_1 = \frac{g_{m1}}{C_L} = \sqrt{2\mu C_{ox}\frac{W_1}{L_1}\frac{\mu C_{ox}}{2}\frac{W_2}{L_2}(V_{bias}-V_{T2})^2} = \mu C_{ox}\sqrt{\frac{W_1}{L_1}\frac{W_2}{L_2}}(V_{bias}-V_{T2}) \quad (1.10)$$

Hence, the first pole is linearly controlled by the bias voltage of transistor M_2.

c) What is the maximum value of the pole when both transistors are operating in the saturation region?

The maximum value of the pole is according to (1.10) maximized when we have as large bias voltage as possible. The problem is to find the maximum possible bias voltage so that the transistor are operating in the saturation region. For the saturation region of the transistor

$$V_{DS} \geq V_{GS} - V_T \quad (1.11)$$

For the output voltage the maximum value is limited by the input voltage V_{in}.

$$V_{out,\,max} = V_{in,\,min} - V_{T1} \quad (1.12)$$

The maximum bias voltage is

$$V_{bias,\,max} = V_{DS,\,max} + V_{T2} = V_{out,\,max} + V_{T2} \quad (1.13)$$

Hence the maximum bias voltage is

$$V_{bias,\,max} = V_{in,\,min} - V_{T1} + V_{T2} \quad (1.14)$$

and thereby the maximum value of the first pole is

$$p_{1,\,max} = \mu C_{ox}\sqrt{\frac{W_1}{L_1}\frac{W_2}{L_2}}(V_{in,\,min} - V_{T1}) \quad (1.15)$$

2. Small signal analysis

A new type of transistor has been developed. The approximate expression for the transistor is as follows:

$$I_1 = I_2 / V_{AC} \quad (2.1)$$

$$I_2 = I_{BS} e^{\frac{V_{AC}}{V_T}}\left(1 + \frac{V_{BC}}{K}\right) \quad (2.2)$$

$$I_3 = I_1 + I_2 \quad (2.3)$$

where I_{BS} and K are process dependent constants and $V_T = \frac{kT}{q}$.

a) Derive a small signal model equivalent to the one shown in the figure for the transistor.

The small signal model is found by taking the derivative of the current into the transistor with respect to the voltages V_{AC} and V_{BC}. It can also be seen as a first order multidimensional Taylor expansion around a specific operation point.

$$i_{ac} = \frac{\partial I_1}{\partial V_{AC}} v_{ac} + \frac{\partial I_1}{\partial V_{BC}} v_{bc} = g_1 v_{ac} + g_2 v_{bc} \tag{2.4}$$

$$i_{bc} = \frac{\partial I_2}{\partial V_{AC}} v_{ac} + \frac{\partial I_2}{\partial V_{BC}} v_{bc} = g_3 v_{ac} + g_4 v_{bc} \tag{2.5}$$

Solving the differentials gives the following values of the components

$$g_3 = \frac{\partial I_2}{\partial V_{AC}} = \frac{I_{BS}}{V_T} e^{\frac{V_{AC}}{V_T}} \left(1 + \frac{V_{BC}}{K}\right) = \frac{I_2}{V_T} \tag{2.6}$$

$$g_4 = \frac{\partial I_2}{\partial V_{BC}} = I_{BS} e^{\frac{V_{AC}}{V_T}} \frac{1}{K} = \frac{I_2}{V_{BC} + K} \tag{2.7}$$

$$g_1 = \frac{\partial I_1}{\partial V_{AC}} = -\frac{I_2}{V_{AC}^2} + \frac{I_2}{V_T} \frac{1}{V_{AC}} = \frac{I_2}{V_{AC}} \left(\frac{1}{V_T} - \frac{1}{V_{AC}}\right) \tag{2.8}$$

$$g_2 = \frac{\partial I_1}{\partial V_{BC}} = \frac{I_2}{(V_{BC} + K) V_{AC}} \tag{2.9}$$

All of these variables is a current source between either node A or node B to node C. A current source in that is voltage controlled with the voltage across the current source is equal to a resistor.

b) Is it good to use this transistor as input transistor in an operational amplifier what are going to be used in a switched capacitor circuit? Motivate your answer carefully.

A switched capacitor circuit must not loose charge at the negative input of the operational amplifier. Since this transistor have DC current into the transistor, charge will be lost, and thereby the correct operation of the circuit will not be achieved.

3. Operational amplifier / Operational transconductance amplifier

An operational amplifier is used in a feedback configuration shown in the figure. The transfer function of the amplifier is given by

$$A(s) = \frac{A_0}{1 + \frac{s}{p_1}} \tag{3.1}$$

a) Find an expression for the feedback factor, β. Sketch the magnitude and phase responses of the loop gain as a function of the frequency. Assume that $R_2 = 10R_1$ and that $R_2 C = 0.5/p_1$

The feedback factor is found be open the feedback loop to the right of the capacitor in parallel with the resistor R_2, then compute the transfer function from that point to the input of the amplifier when the input signal is zeroed. In this case we see that

$$\beta = \frac{R_1}{R_1 + \frac{1}{sC} \parallel R_2} = \frac{R_1}{R_1 + \frac{R_2}{1 + sR_2C}} = \frac{R_1(1 + sR_2C)}{R_1(1 + sR_2C) + R_2} = = \frac{R_1}{R_1 + R_2} \frac{1 + \frac{s}{z_\beta}}{1 + \frac{s}{p_\beta}}$$

where $z_\beta = 1/(R_2C)$ and

$$p_\beta = \frac{R_1 + R_2}{R_1R_2C} = \frac{1}{(R_1 \parallel R_2)C} \tag{3.2}$$

The zero is always lower in frequency than the pole. The magnitude and phase response of the feedback factor and the OPamp gain are shown in Figure 3.1.

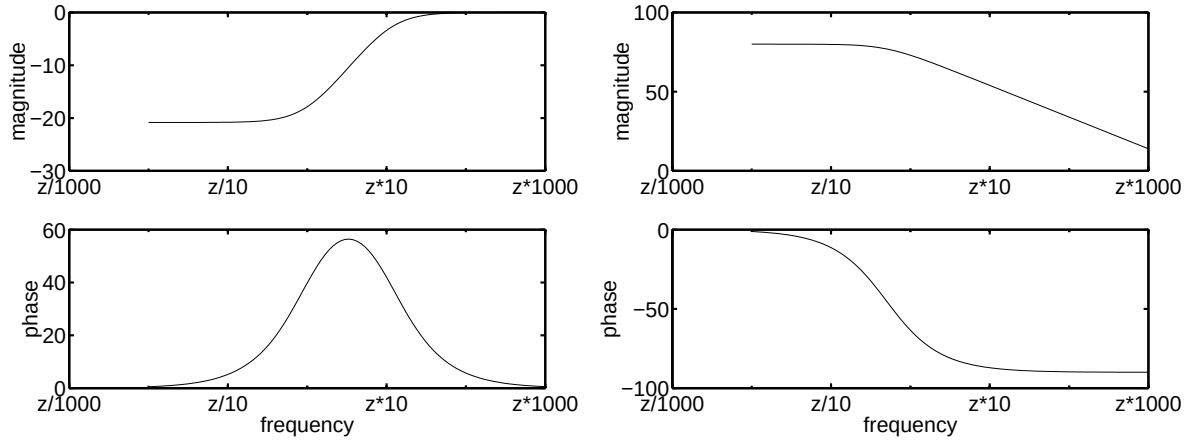

Figure 3.1 The magnitude and phase response of the a) feedback factor, b) OPamp.

The magnitude and phase response of the loop gain is the sum of the phases and the product of the magnitudes. The result is shown in

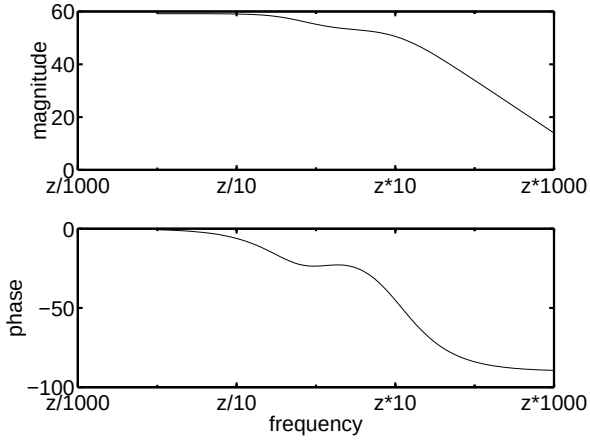

Figure 3.2 The magnitude and phase response of the loop gain of the lossy integrator.

b) Assume that the last stage, a common drain gain stage, in the operational amplifier is the stage that limits the slew rate. How large must the current through the last stage be to have a slew rate of $SR = 40V/\mu s$.

The last stage must be able to drive the capacitor at the output. Here we can use the Miller theorem to achieve the equivalent capacitor, C_{eq}, at the output connected to ground. The gain of the circuit is negative.

$$C_{eq} = \left(1 - \frac{1}{A}\right)C_L \tag{3.3}$$

The slew rate is defined as

$$SR = max\left\{\frac{dV_{out}}{dt}\right\} = \frac{max\{I_{out}\}}{C_{eq}} \tag{3.4}$$

This means that the maximum output current should be $I_{out,\,max} = SR \cdot C_{eq}$.

c) In the circuit shown in the figure the capacitor and the resistor forms the time constant in the building block.Process and temperature variations yields a large component spread, low matching of the time constant. Assume instead that we can form the time constant by a capacitor ratio. State three ways to improve the matching of the two capacitors where $C_2 = C_1 = 50\text{pF}$.

Improved matching is achieved using unit sized capacitor connected in parallel. A layout technique with results in a common centroid is preferable to achieve tight matching. Another way is to place all unit sized capacitors as close to each other as possible so that all transistors have nearly the same surroundings. Some dummy capacitors can be placed at the edges of the capacitor array to achieve the same surroundings. Furthermore, Maximizing the area-to-perimeter helps to increase the matching.

4. Switched capacitor circuit

A switched capacitor circuit in clock cycle 1 is shown in the figure.

a) Derive the transfer function for the clock cycle 1 of the switched capacitor circuit, i.e., $V_{out}(z)/V_{in}(z)$. Assume that the OTA is ideal.

The circuit in Figure 4.1 shows the circuit for both clock cycles.

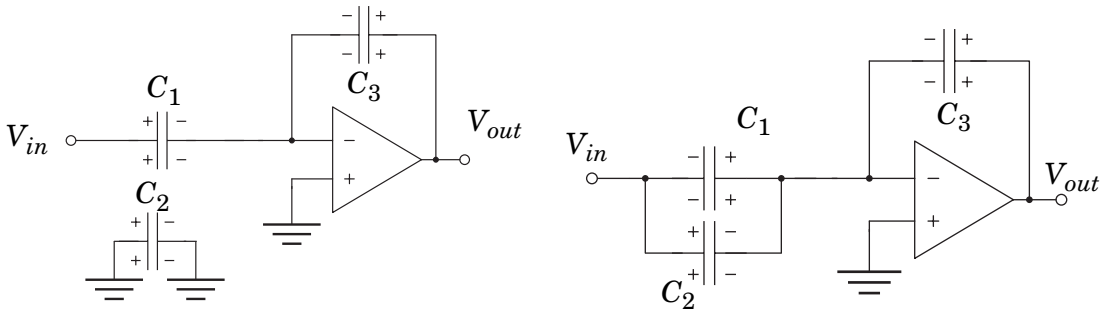

Figure 4.1 The SC circuit in both clock phases. Left ϕ_1, Right ϕ_2.

To compute the transfer function for the circuit charge redistribution analysis is used.

For clock cycle 1, ϕ_1, at time t

$q_1(t) = C_1(V_{in}(t) - 0)$; $q_2(t) = C_2(0 - 0)$; $q_3(t) = C_3(V_{out}(t) - 0)$

For clock cycle 2, ϕ_2, at time $t + \tau$

$q_1(t + \tau) = C_1(0 - V_{in}(t + \tau))$; $q_2(t + \tau) = C_2(V_{in}(t + \tau) - 0)$;
$q_3(t + \tau) = C_3(V_{out}(t + \tau) - 0)$

For clock cycle 1, ϕ_1, at time $t + 2\tau = t + T$:

$q_1(t + 2\tau) = C_1(V_{in}(t + 2\tau) - 0)$; $q_2(t + 2\tau) = C_2(0 - 0)$;
$q_3(t + 2\tau) = C_3(V_{out}(t + 2\tau) - 0)$

The charge conservation equations are

$$q_1(t) - q_2(t) - q_3(t) = q_1(t + \tau) - q_2(t + \tau) - q_3(t + \tau) \qquad (4.1)$$

$$-q_1(t + \tau) - q_3(t + \tau) = -q_1(t + 2\tau) - q_3(t + 2\tau) \qquad (4.2)$$

Inserting the charges into both equations above gives the following expressions

$$C_1V_{in}(t) - 0 - C_3V_{out}(t) = -C_1V_{in}(t + \tau) - C_2V_{in}(t + \tau) - C_3V_{out}(t + \tau)$$

$$C_1V_{in}(t + \tau) - C_3V_{out}(t + \tau) = -C_1V_{in}(t + 2\tau) - C_3V_{out}(t + 2\tau)$$

Eliminating the $V_{out}(t + \tau)$ term in both the equations gives the following equation

$C_1V_{in}(t) - 0 - C_3V_{out}(t) = -(2C_1 + C_2)V_{in}(t + \tau) - C_1V_{in}(t + 2\tau) - C_3V_{out}(t + 2\tau)$

Some simplifications gives

$C_1V_{in}(t) + (2C_1 + C_2)V_{in}(t + \tau) + C_1V_{in}(t + 2\tau) = C_3V_{out}(t) - C_3V_{out}(t + 2\tau)$

Perform Z transformation on the expression gives

$(C_1 + 2(C_1 + C_2)z^{1/2} + C_1z)V_{in}(z) = -C_3(z - 1)V_{out}(z)$

The transfer function is then

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_3}\frac{1+z}{z-1} - \frac{2(C_1+C_2)}{C_3}\frac{z^{1/2}}{z-1} \tag{4.3}$$

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_3}\frac{1+z^{-1}}{1-z^{-1}} - \frac{2(C_1+C_2)}{C_3}\frac{z^{-1/2}}{1-z^{-1}} \tag{4.4}$$

The transfer function is the sum of an inverting bilinear accumulator and an delayed version of an inverting accumulator.

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully.

The circuit with parasitic capacitors are shown in

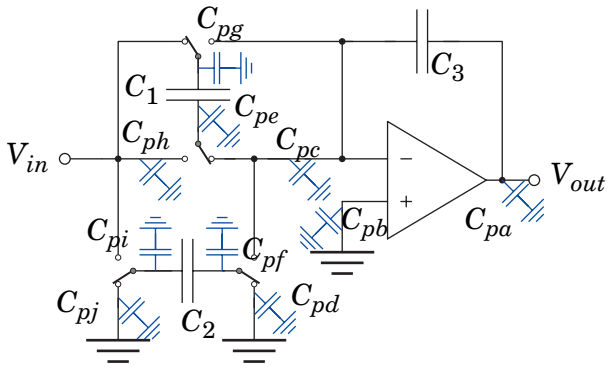

Figure 4.2 The SC circuit with parasitics capacitors

C_{pa} is connected to the ideal output of the OPamp and ground and thereby not changing the transfer function.

C_{pb} not in the signal path and short circuited, not changing the transfer function.

C_{pc} is connected between the virtual ground and ground and thereby not changing the transfer function.

C_{pd} and C_{pj} is connected with both terminal to ground and not changing the transfer function

C_{pe} Charged in clock cycle 2 to $q = C_{pe}V_{in}(t+\tau)$ and discharge to the virtual ground node and thereby adding charge. Hence, it is sensitive to parasitics.

C_{pf} Connected between ground and virtual ground or ground and ground so it will never be charged. Hence, not affecting the transfer function.

C_{pg} The same as C_{pe} but charged in clock cycle 1 and discharged at clock cycle 2. It will affect the transfer function.

C_{ph} Always connected to the input voltage source that charges the capacitor. It will not affect the transfer function

C_{pi} Charged by the input source and discharged to ground and thereby not changing the transfer function.

The circuit is sensitive to parasitics no both sides of the capacitor C_1.

c) What are the benefits and drawbacks of an SC circuit compared to a continuos time circuit?

An SC circuit suffers from the fact that the sampling frequency must be much larger than the maximum signal frequency, we will also need a sample-and-hold circuit to produce the input signals. The benefits is the matching between two capacitors instead of matching of a resistor and a capacitor or a transconductor and a capacitor. Hence, no extra circuitry is needed to achieve an accurate output from the circuit.

5. A mixture of questions

a) Linus has a 10-bit digital to analog converter och needs a SNR of more than 65dB. Propose one way to achieve this SNR.

The SNR of a 10-bit digital to analog converter is defined by the formula

$$\text{SNR} = 6.02N + 1.76\text{dB} = 60.2 + 1.76\text{dB} = 61.96\text{dB} \qquad (5.1)$$

which is smaller than the 65dB that he like to have in his application. If he uses oversampling the SNR can be improved according to the following formula

$$SNR = 6.02N + 1.76\text{dB} + 10\log OSR \qquad (5.2)$$

where the OSR is the over sampling ratio. In his case he needs to have an OSR of

$$OSR = 10^{\frac{65 - 61.96}{10}} = 2.01 \qquad (5.3)$$

b) We have designed a folded cascode operational transconductance amplifier but the Common-Mode Rejection Ratio is too low. This comes from the fact that when the input common-mode voltage is increased the current generated by current source transistor will increase. How can we decrease this sensitivity to common-mode signals?

The CMRR can be increased by decreasing the sensitivity of the drain of the transistor in the current source connected to either the ground or V_{DD} depending on the input transistors. This sensitivity can be decreased by using a cascode current source.

c) In mixed signal designs it is common that the noise from the digital circuits is passed via the substrate to the analog circuits. Assume that we have a common source amplifier with resistive load that are close to a digital switching network. We assume that the switching noise can be modelled as a white noise source with the spectral density of $V_n^2 = S_{sub}$. Derive the equivalent input referred noise spectral density. The only noise to be considered except the substrate noise is the thermal noise of the transistor and the resistor.

For a noise analysis we must compute the transfer function from the noise

sources to the output. This can be done by super position. Starting from the input transistor the transfer function is given by

$$H_1 = -\frac{g_m}{g_{ds} + \frac{1}{R} + sC_L} = -\frac{g_m}{g_{ds}+G}\frac{1}{1+\frac{s}{\frac{g_{ds}+G}{C_L}}} \tag{5.4}$$

The spectral density of the transistor thermal noise can be modelled as a voltage source at the input with the spectral density of $s_1 = (8kT)/(3g_m)$. For the resistor the thermal noise spectral density is given by $s_2 = (4kT)/R$, where the transfer function is given by

$$H_2 = \frac{V_{out}}{I_n} = \frac{1}{g_{ds}+G+sC_L} = \frac{1}{g_{ds}+G}\frac{1}{1+\frac{1}{\frac{g_{ds}+G}{C_L}}} \tag{5.5}$$

The substrate noise from the digital circuit, $s_3 = S_{sub}$, have the following transfer function to the output

$$H_3 = -\frac{g_{mbs}}{g_{ds}+G+sC_L} = -\frac{g_{mbs}}{g_{ds}+G}\frac{1}{1+\frac{1}{\frac{g_{ds}+G}{C_L}}} \tag{5.6}$$

The total output noise power is then

$$S_{n,\,out} = \left|H_1^2\right|s_1 + \left|H_2^2\right|s_2 + \left|H_3^2\right|s_3 \tag{5.7}$$

The total input referred noise value can be related to the output noise value according to

$$S_{n,\,out} = S_{n,\,in}\left|H_1(j\omega)\right|^2 \tag{5.8}$$

so the input referred noise can be computed by dividing the output referred noise by the square of the DC gain of the circuit

$$\begin{aligned} S_{n,\,in} &= s_1 + \left|\frac{H_2}{H_1}\right|^2 s_2 + \left|\frac{H_3}{H_1}\right|^2 s_3 \\ &= \frac{8kT}{3g_m} + \frac{1}{g_m^2}4kTG + \left(\frac{g_{mbs}}{g_m}\right)^2 S_{sub} \end{aligned}$$

d) State two ways to decrease the input noise power in exercise c) and thereby the SNR (if the input signal power is constant) by changing two different relevant design parameters? What will happen to the DC gain of the circuit in both cases? Assume that the resistance R is much smaller than the output resistance of the transistor.

The input referred noise power is decreased if the spectral density is decreased. This is done by increasing the transconductance value of the transistor. This is done by either increasing the current through the transistor which will decrease the possible output swing, or by increasing the size of the input transistor. Increasing the maximum current will increase the DC gain since $G \gg g_{ds}$. Increased size of the transistor will also increase the DC gain of the circuit.

6. Extra exercise

NOTE: This exercise is only for the students that have taken the course before 2002 and not handed in three assignments during the course.

The circuit shown in the figure is to be used in a analog signal processing circuit.

a) Draw a small signal model of the amplifier, neglect the influence of the parasitic capacitances introduced in the transistors.

The small signal model for the folded cascode amplifier is shown in Figure 6.1)

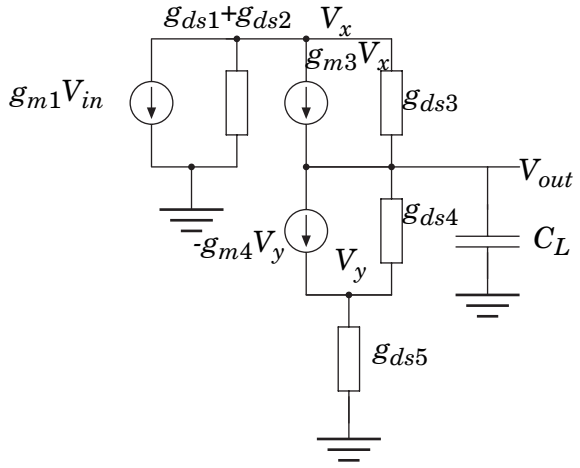

Figure 6.1 The small signal model for the folded cascode amplifier.

b) The transfer function of the amplifier can be computed to

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}(g_{m3}+g_{ds3})\alpha}{(g_{ds4}g_{ds5}+\alpha sC_L)(g_{ds3}+g_{m3})+(g_{ds1}+g_{ds2})(g_{ds4}g_{ds5}+(g_{ds3}+sC_L)\alpha)}$$

where $\alpha = g_{ds4}+g_{ds5}+g_{m4}$ when the body effect is neglected.
Approximate the transfer function and find simple expressions for the DC gain, first pole, and the unity-gain frequency.

The DC gain, first pole and the unity-gain frequency is found from the transfer function. To arrive in a small expression we approximate the transfer function. First we collect all terms containing α is the denominator.

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}(g_{m3}+g_{ds3})\alpha}{g_{ds4}g_{ds5}(g_{ds3}+g_{m3}+g_{ds1}+g_{ds2})+(g_{ds1}+g_{ds2})(g_{ds3}+sC_L)\alpha+(g_{ds3}+g_{m3})\alpha sC_L}$$

Move the factors $(g_{m3}+g_{ds3})\alpha$ to the denominator this gives the following transfer function

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{\frac{g_{ds4}g_{ds5}(g_{ds3}+g_{m3}+g_{ds1}+g_{ds2})}{(g_{m3}+g_{ds3})\alpha}+\frac{\alpha((g_{ds1}+g_{ds2})(g_{ds3}+sC_L)+(g_{ds3}+g_{m3})sC_L)}{(g_{m3}+g_{ds3})\alpha}}$$

Use the approximation that $g_m \gg g_{ds}$.

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{\frac{g_{ds4}g_{ds5}(g_{ds3}+g_{m3})}{(g_{m3}+g_{ds3})\alpha}+\frac{(g_{ds1}+g_{ds2})g_{ds3}+(g_{ds3}+g_{m3})sC_L}{(g_{m3}+g_{ds3})}}$$

Some further simplifications gives

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{\frac{g_{ds4}g_{ds5}}{g_{m4}}+\frac{(g_{ds1}+g_{ds2})g_{ds3}}{g_{m3}}+sC_L}$$

The transfer function can be reformulated as

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{\frac{g_{ds4}g_{ds5}}{g_{m4}}+\frac{(g_{ds1}+g_{ds2})g_{ds3}}{g_{m3}}}\frac{1}{1+\frac{s}{\frac{\frac{g_{ds4}g_{ds5}}{g_{m4}}+\frac{(g_{ds1}+g_{ds2})g_{ds3}}{g_{m3}}}{C_L}}}$$

The DC gain is thereby

$$A_0 \approx -\frac{g_{m1}}{\frac{g_{ds4}g_{ds5}}{g_{m4}}+\frac{(g_{ds1}+g_{ds2})g_{ds3}}{g_{m3}}} \tag{6.1}$$

The first pole is

$$p_1 \approx \frac{\frac{g_{ds4}g_{ds5}}{g_{m4}}+\frac{(g_{ds1}+g_{ds2})g_{ds3}}{g_{m3}}}{C_L} \tag{6.2}$$

In a one pole system the unity-gain frequency is approximately given by the expression

$$\omega_u \approx |A_0| p_1 \approx \frac{g_{m1}}{C_L} \tag{6.3}$$

c) What will happen to the DC gain and the first pole if we ...
...increase the current through transistor M_2.
...increase the size of the load capacitor.
...insert a gain boosting stage to transistor M_3 and M_4

Assume that the increased sizes does not change the operation region of the transistors.

To solve this we have to formulate the small signal parameters as functions of the design variables.

$$g_m \approx \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \propto \sqrt{\frac{WI_D}{L}} \tag{6.4}$$

$$g_{ds} = \lambda I_D \propto \frac{I_D}{L} \tag{6.5}$$

In this exercise we are not interested of the influence of the channel length so $g_m \propto \sqrt{WI_D}$ and $g_{ds} \propto I_D$. Inserting this expressions into Eq. (6.1) and Eq. (6.2) gives

$$A_0 = \frac{g_{m1}}{g_{out}} \propto \frac{\sqrt{W_1 I_{D1}}}{\frac{I_{D4}I_{D5}}{\sqrt{W_4 I_{D4}}} + \frac{(I_{D1}+I_{D2})I_{D3}}{\sqrt{W_3 I_{D3}}}} = \frac{\sqrt{W_1 I_{D1}}}{\frac{I_{D5}^{3/2}}{\sqrt{W_4}} + \frac{(2I_{D1}+I_{D5})I_{D5}^{1/2}}{\sqrt{W_3}}}$$

$$p_1 = \frac{g_{out}}{C_L} \propto \frac{\frac{I_{D4}I_{D5}}{\sqrt{W_4 I_{D4}}} + \frac{(I_{D1}+I_{D2})I_{D3}}{\sqrt{W_3 I_{D3}}}}{C_L} = \frac{\frac{I_{D5}^{3/2}}{\sqrt{W_4}} + \frac{(2I_{D1}+I_{D5})I_{D5}^{1/2}}{\sqrt{W_3}}}{C_L}$$

In the last equality we have used the fact that $I_{D3} = I_{D4} = I_{D5}$ and that $I_{D2} = I_{D1} + I_{D5}$.

An increased current through transistor M_2 gives an increased current through transistor M_1 but M_5 will have nearly the same current. Hence, only I_{D1} will increase. The output conductance, g_{out}, will increase so the first pole will increase in frequency. If we instead look at the DC gain we have two cases. First, if the I_{D5} factors in the denominator are dominating then will the DC gain increase as the current increases. Second, when the I_{D1} term is dominating then will the DC gain be decreased as I_{D1} increases.

Increasing the load capacitor will not change the DC gain but the first pole will decrease in magnitude.

Adding a gain boosting stage to the amplifier will increase the gain by a factor of the gain in the gain boosting stage. On the other hand the first pole will also move towards lower frequencies by a factor of about the gain in the gain boosting stage.