Correct(?) Solutions to Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	January 11, 2002
Time:	14 - 18
Place:	Kårallen
Max. no of points:	70; 50 from written test, 15 for project, and 5 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. Written material and downloaded web-material except old exams. No textbooks are allowed.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no on a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

This exam covers nearly the whole course except the filter chapters. Our advise to you is to start by reading through the exam and then begin to solve the exercises that you are familiar with.

Exercise

1. Basic CMOS building blocks

a) Assume that a voltage source with a input resistance, R_{in}, is connected to the node v_1. Derive the transfer function from v_{in} to v_{out}. Assume that all transistors are operating in the saturation region

The equivalent small signal is shown in Figure 1.1.

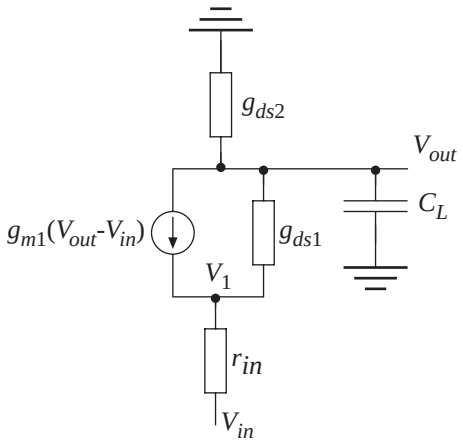


Figure 1.1 ESSS for the Common Gate amplifier

Using nodal analysis in the nodes V_1 and V_{out} gives the following equations

$$g_{m1}V_1 + (V_1 - V_{out})g_{ds1} + (V_1 - V_{in})G_{in} = 0 \quad (1.1)$$

$$g_{m1}V_1 + (V_1 - V_{out})g_{ds1} - V_{out}(g_{ds2} + sC_L) = 0 \quad (1.2)$$

Solving for V_1 in Eq. (1.1) and inserting it into Eq. (1.2) results in

$$\frac{V_{out}}{V_{in}} = \frac{G_{in}(g_{m1} + g_{ds1})}{(g_{ds2} + sC_L)(g_{m1} + g_{ds1} + G_{in}) + g_{ds1}G_{in}} \approx \frac{G_{in}(g_{m1} + g_{mbs1})}{(g_{ds2} + sC_L)(g_{m1} + G_{in}) + g_{ds1}G_{in}} \tag{1.3}$$

where $g_{m1} \gg g_{ds1}$ is assumed.
The DC-gain and the location of the first pole is found from Eq. (1.3) according to

$$A_0 \approx \frac{G_{in}(g_{m1})}{g_{ds2}(g_{m1} + G_{in}) + g_{ds1}G_{in}} \tag{1.4}$$

$$p_1 = \frac{g_{ds2}(g_{m1} + G_{in}) + g_{ds1}G_{in}}{(g_{m1} + G_{in})C_L} \tag{1.5}$$

b) What will happen with the gain and the first pole of the circuit in the figure if the width of the transistor M_1 is made larger?
The transconductance

$$g_{m1} \approx \sqrt{\mu_n C_{ox} \frac{W_1}{L_1} I_D} = E\sqrt{W_1} \tag{1.6}$$

and the output conductance is given by

$$g_{dsi} \approx \lambda_i I_D \tag{1.7}$$

where I_D is the current through the gain stage. Transistor M_2 is considered as a current source and a constant current will flow through the circuit.
The expression for the DC-gain is

$$A_0 \approx \frac{G_{in}E\sqrt{W_1}}{\lambda_2 I_D(E\sqrt{W_1} + G_{in}) + \lambda_1 I_D G_{in}} \approx \frac{G_{in}}{\lambda_2 I_D + \frac{I_D G_{in}}{E\sqrt{W_1}}(\lambda_1 + \lambda_2)} \tag{1.8}$$

Increasing W_1 will increase the DC-gain of the circuit. Continuing to the first pole the expression is computed to

$$p_1 \approx \frac{\lambda_2 I_D(E\sqrt{W_1}) + I_D(\lambda_1+\lambda_2)G_{in} + \lambda_1 I_D(E\sqrt{W_1}) - \lambda_1 I_D(E\sqrt{W_1})}{(E\sqrt{W_1}+G_{in})C_L} = \frac{(\lambda_1+\lambda_2)I_D}{C_L} - \frac{\lambda_1 I_D}{\left(1+\frac{G_{in}}{E\sqrt{W_1}}\right)C_L} \tag{1.9}$$

Increasing the width of M_1 will decrease the frequency of the first pole.

c) An ideal voltage source is connected to node V_1. Determine the operation regions of the transistor M_1 when node V_1 ramps from V_{dd} to ground. Assume that transistor M_2 operates as an ideal current source delivering the current I_{bias}. Explain how to find the input voltage where transistor M_1 start to operate in the linear operation region.

The transistor M_1 is in the cut-off regime as long as $V_{b1} - V_{T1} < V_1$ no (very small) current will flow through transistor M_1 so the output voltage will be equal to V_{dd}.
When the input voltage is lower than $V_{b1} - V_{T1}$ the transistor will be in saturation since $V_{ds} > V_{b1} - V_1 - V_T > 0$. Depending of the value of V_{b1} will the transistor operate in the linear region. The input voltage this will happen can be computed as follows.
The current through transistor M_1 in saturation is

$$I_{D1} = \alpha(V_{b1} - V_1 - V_{T1})^2(1 + \lambda V_{out}) \tag{1.10}$$

In saturation the current through transistor M_1 must equal I_{bias}.

$$I_{bias} = \alpha(V_{b1} - V_1 - V_{T1})^2(1 + \lambda(V_{out} - V_1)) \tag{1.11}$$

Solving for $V_{out} - V_1$ gives thew following expression.

$$V_{out} - V_1 = \frac{1}{\lambda\alpha}\frac{I_{bias}}{(V_{b1} - V_1 - V_{T1})} - 1 \tag{1.12}$$

The transistor operates in the saturation region when $V_{out} - V_1 = V_{b1} - V_1 - V_{T1}$. Inserting Eq. (1.12) into previous equation and solving for V_1 gives the input voltage where the transition between the saturation and linear operation point appears.

d) Determine the maximum possible output swing for saturated transistors if the bias voltages V_{b1} and V_{b2} are connected to $V_{dd}/2$ and V_1 is assumed to be connected to ground.

The maximum output voltage for M_2 to operate in saturation is

$$V_{dd} - V_{sd2sat} = V_{dd} - (V_{sg2} - V_{T2}) = V_{dd}/2 + V_{T2} \tag{1.13}$$

The minimum output voltage for M_1 to operate in saturations $V_{out} - V_1 > V_{b1} - V_1 - V_T$ which can be simplified to

$$V_{out} > V_{dd}/2 - V_{T1} \tag{1.14}$$

Which means that V_{out} can range from $V_{dd}/2 + V_{T2}$ to $V_{dd}/2 - V_{T1}$.

2. Operational amplifier

a) Derive the differential voltage gain of the circuit. No parasitic capacitances needs to be considered.

To simplify the small signal computation we assume that the output conductance of transistor M_5 is zero, and thereby setting the common node of the differential pair to small signal ground. Further, the circuit is a fully differential gain stage and thereby it is sufficient to compute the small signal transfer function of half the circuit.

The Equivalent small signal scheme is shown in Figure 2.1

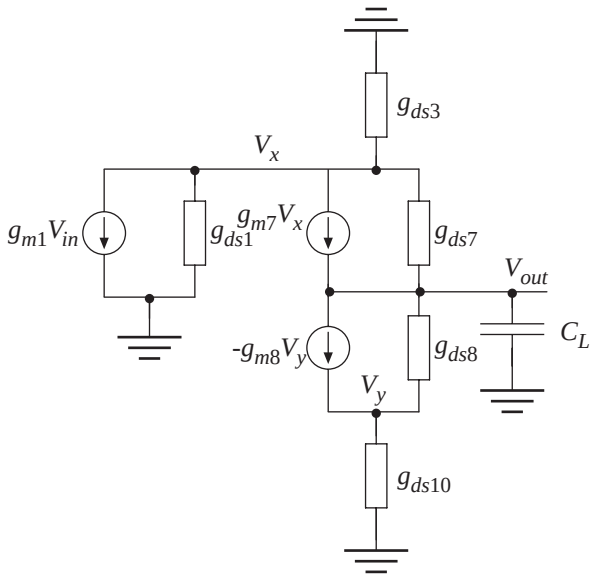


Figure 2.1 ESSS for the Folded cascode amplifier.

Performing nodal analysis in the nodes V_x, V_y, and V_{out} results in the following equations

$$\begin{gathered} g_{m1}V_{in} + V_x g_{ds1} + V_x g_{ds1} + g_{m7}V_x + (V_x - V_{out})g_{ds7} = 0 \\ g_{m8}V_y + (V_y - V_{out})g_{ds8} + V_y g_{ds10} = 0 \\ g_{m7}V_x + (V_x - V_{out})g_{ds7} - V_{out}sC_L + g_{m8}V_y + (V_y - V_{out})g_{ds8} = 0 \end{gathered} \tag{2.1}$$

Solving for V_{out} in the system of equations gives

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}(g_{m7} + g_{ds7})(g_{m8} + g_{ds8} + g_{ds10})}{(g_{ds1} + g_{ds3})g_{ds7}(g_{m8} + g_{ds8} + g_{ds10}) + (g_{ds1} + g_{ds3} + g_{ds7} + g_{m7})(g_{ds8} + g_{ds10}) + sC_L} \tag{2.2}$$

dividing by the two expression within the parenthesis in the numerator and assuming that $g_m \gg g_{ds}$ gives the following expression

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{\frac{(g_{ds1}+g_{ds3})g_{ds7}}{g_{m7}} + \frac{g_{ds8}g_{ds10}}{g_{m8}} + sC_L} \tag{2.3}$$

The DC-gain is extracted from Eq. (2.3).

$$A_0 = \frac{-g_{m1}}{\frac{(g_{ds1}+g_{ds3})g_{ds7}}{g_{m7}} + \frac{g_{ds8}g_{ds10}}{g_{m8}}} = \frac{-g_{m1}}{g_{out}} \tag{2.4}$$

and the first pole is given by

$$p_1 = \frac{g_{out}}{C_L} \tag{2.5}$$

b) The second pole arises from the parasitic capacitance in node v_x in the figure. The expression for this pole is $p_2 = g_{m7}/C_x$ where C_x is the parasitic capacitance in node V_x.

How do you increase the phase margin...

...if the area is limited?

...if the power is critical?

...if the unity-gain and power is critical?

In each case what are the drawbacks of the circuit performance?

The phase margin is increased if the ratio between the second pole and the unity-gain frequency is increased. The unity-gain frequency can be expressed as

$$\omega_u \approx A_o p_1 \approx \frac{g_{m1}}{C_L} \approx \frac{\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}I_{diff}}}{C_L} \tag{2.6}$$

where I_{diff} is the current through transistor M_1. The second pole is given in the text to be

$$p_2 \approx \frac{g_{m7}}{C_x} \approx \frac{g_{m7}}{C_{gs7}} \approx \frac{\sqrt{2\mu_p C_{ox}\frac{W_7}{L_7}I_{casc}}}{\frac{2}{3}C_{ox}W_7L_7} = \frac{\sqrt{2\mu_p}}{\frac{2}{3}\sqrt{C_{ox}}}\frac{\sqrt{I_{casc}}}{L_7\sqrt{W_7L_7}} \tag{2.7}$$

where I_{casc} is the current through transistors M_7, M_8 and M_{10}. The expression for the ratio between the second pole and the unity-gain frequency is given by

$$\frac{p_2}{\omega_u} \approx \frac{\frac{\sqrt{2\mu_p}}{2}\frac{\sqrt{I_{casc}}}{\sqrt{C_{ox}}}L_7\sqrt{W_7L_7}}{\frac{\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}I_{diff}}}{C_L}} = \frac{3}{2}\sqrt{\frac{\mu_p}{\mu_n}}\frac{\sqrt{L_1}C_L}{C_{ox}L_7\sqrt{W_7L_7W_1}}\sqrt{\frac{I_{casc}}{I_{diff}}} \tag{2.8}$$

Further, the DC-gain can be expressed as

$$A_0 \approx \frac{-g_{m1}}{\frac{(g_{ds1}+g_{ds3})g_{ds7}}{g_{m7}} + \frac{g_{ds8}g_{ds10}}{g_{m8}}} \approx \frac{\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}I_{diff}}}{\frac{(\lambda_1 I_{diff}+\lambda_3(I_{diff}+I_{casc}))\lambda_7 I_{casc}}{\sqrt{2\mu_p C_{ox}\frac{W_7}{L_7}I_{casc}}} + \frac{\lambda_8\lambda_{10}I_{casc}^2}{\sqrt{2\mu_n C_{ox}\frac{W_8}{L_8}I_{casc}}}} \approx \sqrt{2\mu_n C_{ox}}\frac{\sqrt{\frac{W_1}{L_1}I_{diff}}}{\frac{\left(\frac{1}{L_1}I_{diff}+\frac{1}{L_3}(I_{diff}+I_{casc})\right)\sqrt{I_{casc}}}{\sqrt{W_7L_7}} + \frac{I_{casc}^{3/2}}{\sqrt{2\mu_n C_{ox}}\sqrt{W_8L_8}L_{10}}} \tag{2.9}$$

From Eq. (2.8) and Eq. (2.9) the solution can be found.

The phase margin can be increased if the area is limited by for example:
- Increasing I_{casc} the drawbacks will be higher power dissipation and lower DC-gain.

The phase margin can be increase if the power is critical by for example:
- Increasing C_L, the drawbacks is decreased Slew-Rate and unity-gain but the DC-gain will not be changed.
- Decrease W_7, the drawback is decreased DC-gain, no changes to the unity-gain or the Slew-Rate.

The phase margin can be increase if the unity-gain and the power is critical for example by:
- Decrease W_7, the drawback is decreased DC-gain, no changes to the unity-gain or the Slew-Rate.

c) What is slew-rate? Derive the Slew-Rate of the circuit in the figure. Motivate your solution carefully

Slew-Rate is maximum possible voltage change at the output of the device, for example an amplifier. This maximum possible voltage change is set by the ability of the device to drive current.
The Slew-Rate is defined as

$$max\left\{\frac{dV_{out}}{dt}\right\} \tag{2.10}$$

The Folded cascode amplifier drives capacitive load and thereby the well-known relationship

$$I = C_L\frac{dV}{dt} \tag{2.11}$$

can be used as gives the following

$$SR = max\left\{\frac{dV_{out}}{dt}\right\} = max\left\{\frac{I_{out}}{C_L}\right\} = \frac{max\{I_{out}\}}{C_L} = \frac{I_{casc}+I_{diff}}{C_L} \tag{2.12}$$

3. Noise in CMOS circuits

a) Derive the equivalent output noise of the circuit, shown in the figure, due to the thermal noise generated by the transistors M_1 and M_2.

The equivalent small signal scheme for the circuit is shown in Figure 3.1.

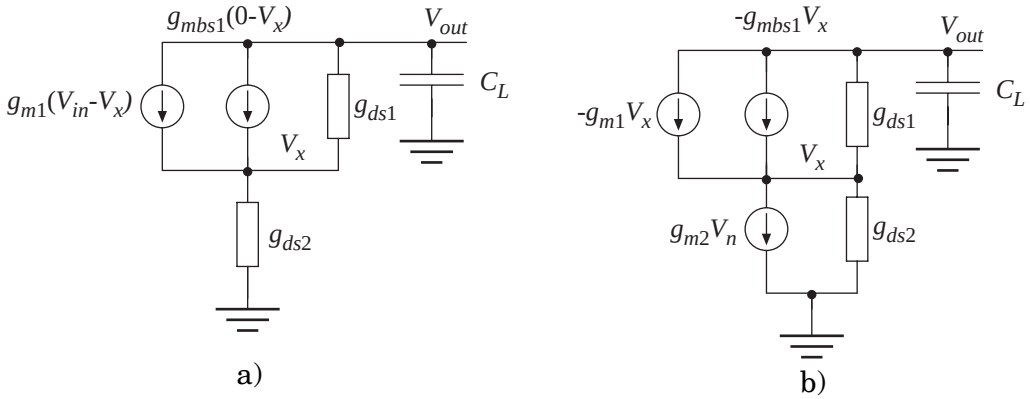


Figure 3.1 ESSS for the source-degenerated CS stage. a) Input to output. b) bias to output.

To compute the equivalent output noise the transfer function from V_{in} to V_{out} and from V_b to V_{out} is performed. We start by setting up the equations needed to compute the transfer function from the input to the output.

$$g_{m1}(V_{in}-V_x)-g_{mbs1}V_x+(V_{out}-V_x)g_{ds1}-V_xg_{ds2} = 0 \tag{3.1}$$

$$g_{m1}(V_{in}-V_x)-g_{mbs1}V_x+(V_{out}-V_x)g_{ds1}+V_{out}sC_L = 0 \tag{3.2}$$

Solving for V_{out} by eliminating V_x gives the following transfer function

$$H_1 = \frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{ds1}} \frac{1}{1 + \frac{s}{\frac{g_{ds1}g_{ds2}}{C_L(g_{m1} + g_{mbs1} + g_{ds1} + g_{ds2})}}} \tag{3.3}$$

The equations for the transfer function between V_b and V_{out} is given by

$$g_{m2}V_n + g_{ds2}V_x + g_{m1}V_x + g_{mbs1}V_x + (V_x - V_{out})g_{ds1} = 0 \tag{3.4}$$

$$g_{m1}V_x + g_{mbs1}V_x + (V_x - V_{out})g_{ds1} - V_{out}sC_L = 0 \tag{3.5}$$

Solving for V_{out} by eliminating V_x results in

$$\begin{aligned} H_2 = \frac{V_{out}}{V_b} &= \frac{(g_{m1} + g_{mbs1} + g_{ds1})g_{m2}}{g_{ds1}g_{ds2}} \frac{1}{1 + \frac{s}{\frac{g_{ds1}g_{ds2}}{C_L(g_{m1} + g_{mbs1} + g_{ds1} + g_{ds2})}}} \\ &\approx \frac{(g_{m1} + g_{mbs1})g_{m2}}{g_{ds1}g_{ds2}} \frac{1}{1 + \frac{s}{\frac{g_{ds1}g_{ds2}}{C_L(g_{m1} + g_{mbs1} + g_{ds1} + g_{ds2})}}} \end{aligned} \tag{3.6}$$

The rms output noise is given by

$$V_{no}^2 = \int |H_1|^2 V_{in}^2 df + \int |H_2|^2 V_b^2 df \tag{3.7}$$

where

$$V_{in}^2 = \frac{8kT}{3}\frac{1}{g_{m1}} \tag{3.8}$$

and

$$V_b^2 = \frac{8kT}{3}\frac{1}{g_{m2}} \tag{3.9}$$

The last two equations comes from the fact that the thermal noise power of a transistor is modelled as a gaussian white noise source.

The two integrals in Eq. (3.7) can be calculated using the concept of noise bandwidth which results in the following computation.

$$V_{no}^2 = \left(\frac{g_{m1}}{g_{ds1}}\right)^2 \frac{p_1}{4} V_{in}^2 + \left(\frac{(g_{m1} + g_{mbs1})g_{m2}}{g_{ds1}g_{ds2}}\right)^2 \frac{p_1}{4} V_b^2 \tag{3.10}$$

$$V_{no}^2 = \frac{2kT}{3C_L}\left(\frac{g_{m1}}{g_{ds1}}g_{ds2} + \frac{(g_{m1}+g_{mbs1})^2 g_{m2}}{g_{ds1}g_{ds2}}\right)\frac{1}{g_{m1}+g_{mbs1}+g_{ds1}+g_{ds2}} \approx$$

$$\approx \frac{2kT}{3C_L}\left(\frac{g_{m1}}{g_{ds1}(g_{m1}+g_{mbs1})}g_{ds2} + \frac{(g_{m1}+g_{mbs1})g_{m2}}{g_{ds1}g_{ds2}}\right)$$

$$\approx \frac{2kT}{3C_L}\left(\frac{g_{ds2}}{g_{ds1}} + \frac{g_{m1}g_{m2}}{g_{ds1}g_{ds2}}\right) \tag{3.11}$$

b) Describe two ways to decrease the equivalent output noise by changing relevant design parameters. What will happen to the gain, unity-gain and slew-rate of the circuit?

Relevant design parameters are for example the current through the circuit and the size of the transistor.
Rewriting the Eq. (3.11) with the design parameters yields

$$V_{no}^2 = \frac{2kT}{3}\frac{1}{C_L}\left(\frac{L_2}{L_1} + \frac{\sqrt{2\mu_n C_{ox} W_1 L_1}\sqrt{2\mu_n C_{ox} W_2 L_2}}{I_{bias}}\right) \tag{3.12}$$

The DC-gain from the input to the output is given by

$$A_0 = \frac{g_{m1}}{g_{ds1}} \approx \sqrt{\frac{2\mu_n C_{ox} W_1 L_1}{I_{bias}}} \tag{3.13}$$

and the unity-gain is given by

$$\omega_u \approx A_0 p_1 \approx \frac{g_{ds2}g_{m1}}{(g_{m1}+g_{mbs1}+g_{ds1}+g_{ds2})C_L} \approx \frac{g_{ds2}}{C_L} \approx \frac{I_{bias}}{L_2 C_L} \tag{3.14}$$

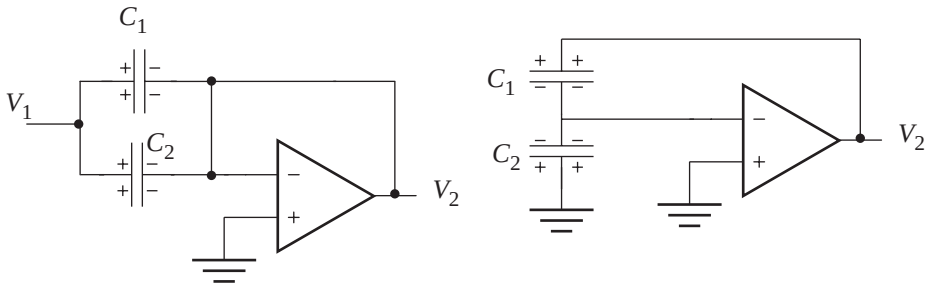
The equivalent output noise can be reduced by:

- Increase the bias current -> Decreased DC-gain, Increased unity-gain, and Increased Slew-rate.
- Decreased W_2 -> No change to the DC-gain, unity-gain or Slew-Rate.
- Decrease L_2 -> No change to the DC-gain, increased unity-gain frequency and no change to the Slew-Rate.

4. Switched capacitor

a) Derive the transfer function of the switched capacitor circuit shown in the figure, i.e, $V_2(z)/V_1(z)$. Assume that the operational transconductance amplifier is ideal.

The the two different clock cycles of the circuit is shown Figure 4.1



clock cycle 1 clock cycle 2

Figure 4.1 The circuit in the two different clock cycles.

Starting in the clock cycle 1 at time t:

$q_1(t) = (V_1(t) - 0)C_1$

$q_2(t) = (V_1(t) - 0)C_2$

At time $t + \tau$

$q_1(t + \tau) = V_2(t + \tau)C_1$

$q_2(t + \tau) = 0$

At time $t + 2\tau$

$q_2(t + s\tau) = (V_1(t + 2\tau) - 0)C_1$

$q_2(t + 2\tau) = (V_1(t + 2\tau) - 0)C_2$

The last equation comes from the charge conservation. The charge at the end of clock cycle t is equal to the charge during clock cycle $t + \tau$ since no charge can vanish into the operational amplifier.

$$q_1(t) + q_2(t) = q_1(t + \tau) + q_2(t + \tau) \tag{4.1}$$

Inserting the above equations into Eq. (4.1) gives.

$$V_1(t)C_1 + V_1(t)C_2 = V_2(t + \tau)C_1 + 0 \tag{4.2}$$

performing z-transformation on both sides gives

$$V_1(z)(C_1 + C_2) = z^{1/2}V_2(z)C_1 \tag{4.3}$$

which gives the following transfer function

$$\frac{V_2(z)}{V_z(z)} = z^{-1/2}\frac{C_1 + C_2}{C_1} = z^{-1/2}\left(1 + \frac{C_2}{C_1}\right) \tag{4.4}$$

The factor $z^{-1/2}$ is just a time delay from the input to the output, it means that when the input is sampled at time t, the output will not be available until the time $t + \tau$.

b) Is the circuit insensitive to parasitics? Motivate your answer carefully.

There will be parasitic capacitances at both sides of each switch and the input and output of the operational amplifier as shown in Figure 4.2.

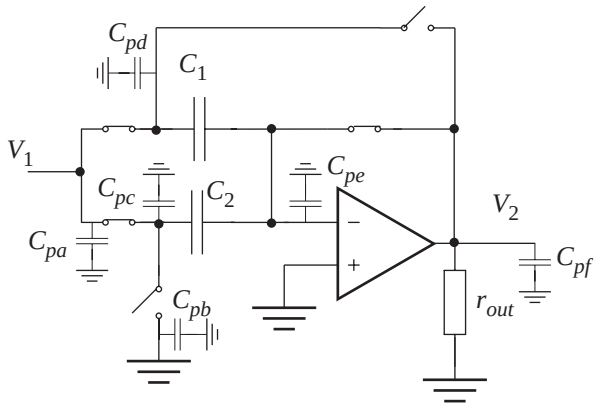


Figure 4.2 The SC-circuit with all parasitic capacitances.

C_{pa} is connected between the ideal input and ground. Not changing the transfer function

C_{pb} is always connected to ground. Will not change the transfer function.

C_{pc} is connected between the ideal input and ground or between ground and ground and thereby not interacting with the transfer function.

C_{pd} is connected ideal input and ground or the ideal output of the opamp and ground and thereby no change in the transfer function will appear.

C_{pe} is connected between the virtual ground and ground not causing any change in the transfer function.

C_{pf} is connected between the ideal output of the opamp and ground and thereby not changing the transfer function.

Hence, the circuit is insensitive of capacitive parasitics with respect to the transfer function.

c) Assume that the operational transconductance amplifier suffers from finite gain, A, and input offset voltage, V_{os}. Derive the transfer function.

At time t, $t + 2\tau$, $t + 4\tau$ and so on, the potential at the negative input of the operational amplifier, V_x, will be equal to $V_x(t + n\tau) = V_{os}$.
At time $t + \tau$, $t + 3\tau$, $t + 5\tau$ and so on, the potential at the negative input of the operational amplifier will be equal to

$$V_x(t + (n + 1)\tau) = V_{os} - \frac{V_2(t + (n + 1)\tau)}{A}. \qquad (4.5)$$

Using charge analysis gives:

$$q_1(t) = (V_1(t) - V_{os})C_1$$

$$q_2(t) = (V_1(t) - V_{os})C_2$$

$$q_1(t+\tau) = (V_2(t+\tau) - V_x(t+\tau))C_1 = \left(V_2(t+\tau)\left(1+\frac{1}{A}\right) - V_{os}\right)C_1$$

$$q_2(t+\tau) = -V_x(t+\tau)C_1 = \left(V_2(t+\tau)\frac{1}{A} - V_{os}\right)C_1$$

$$q_1(t+2\tau) = (V_1(t+2\tau) - V_{os})C_1$$

$$q_2(t+2\tau) = (V_1(t+2\tau) - V_{os})C_2$$

The charge conservation gives

$$q_1(t) + q_2(t) = q_1(t+\tau) + q_2(t+\tau)$$

Some manipulation gives

$$\frac{V_2(z)}{V_1(z)} = z^{-1/2}\frac{C_1 + C_2}{\left(1+\frac{1}{A}\right)C_1 + \frac{C_2}{A}} = z^{-1/2}\left(1+\frac{C_2}{C_1}\right)\frac{1}{1+\frac{1}{A}\left(1+\frac{C_2}{C_1}\right)} \tag{4.6}$$

We can from this equation see that is A is infinity we will return to the same answer as in a). Further, the circuit is insensitive to offset in the operational amplifier and we can get a design specification of the DC-gain of operational amplifier to fulfill a certain specification of the whole system.

d) Find the settling time constants, i.e. the speed of the circuit, for both clock phases. Neglect the influence of the switches.

All the parasitics of the circuit are shown in Figure 4.2.
For clock phase t, $t+2\tau$, $t+4\tau$ and so on
The feedback factor is equal to 1 since the amplifiers output is connected direct to the negative input => $\beta_1 = 1$
This gives the speed $w_{-3dB} = w_u$

For clock phase $t+\tau$, $t+3\tau$, $t+5\tau$ and so on

$$\beta_2 = \frac{\frac{1}{C_{pe}+C_2}}{\frac{1}{C_1}+\frac{1}{C_{pe}+C_2}} = \frac{C_1}{C_1 + C_{pe} + C_2} \tag{4.7}$$

The second clock phase is the one that are slowing down the system. The speed is equal to

$$w_{-3db} = \beta_2 \omega_u = \frac{C_1}{C_1 + C_{pe} + C_2} \omega_u \tag{4.8}$$

5. CMOS Building blocks

a) In an active RC filter we need to have an operational amplifier with the following specification

Table 1: OPamp specification

Performance parameters	Values
A_0	80dB
f_u	100MHz
C_L	5pF
SR	80V/μs
OR	[0.3 - 2.3]V
CMR	[0.1 - 2.0]V
V_{dd}	3.3V
P_{diss}	<10mW

How would you like to design the operational amplifier?

Draw the block diagram of the operational amplifier and make a specification of each block in your design, like the one above and the name of the type of building block and the type of the input transistors.

b) The same task a the one above but here we like to have an operational transconductance amplifier that will be used in a SC-filter.

These two exercise have very many solutions. The key point is to understand the difference between a operational amplifier and a operational transconductance amplifier. A operational amplifier has small output resistance and it has the possibility to drive load with low resistance. One solution can look like in Figure 5.1

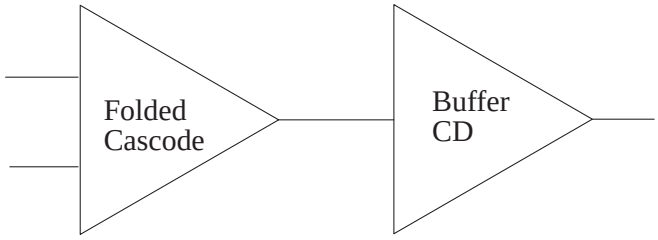


Figure 5.1 A block diagram of an operational amplifier

The Folded cascode amplifier has pmos input transistors to fulfill the CMR and the following specification:
$A_0 = 82dB$, $f_u = 120MHz$, $SR = 80V/\mu s$, $CMR = [0.1 - 2.0]$, $P_{diss} = 7mW$ and $OR = [0.5 - 3.1]$
The buffer is a common drain amplifier with nmos transistors. The specification is:
$A_0 = -1.9dB$, $f_u = 200MHz$, $SR = 80V/\mu s$, $OR = [0.3 - 2.3]$, $P_{diss} = 3mW$ the CMR is not possible to define.

The operational transconductance amplifier has high output resistance and thereby it can only drive load large resistance.
Here we only uses a Folded cascode amplifier and no buffer at the output. The Folded cascode amplifier will have to following specification:
$A_0 = 80dB$, $f_u = 100MHz$, $SR = 80V/\mu s$, $CMR = [0.1 - 2.0]$, $P_{diss} = 10mW$ and $OR = [0.3 - 2.3]$

c) Derive the quotient between the output and input resistance of the current mirror shown in the figure.

The ESSS is shown in Figure 5.2

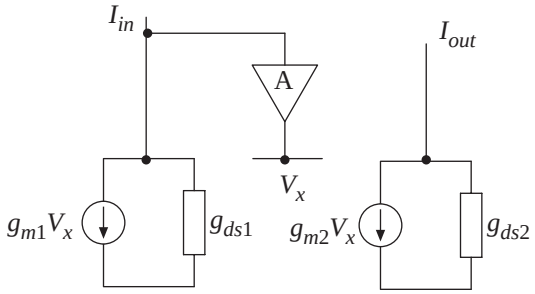


Figure 5.2 The ESSS of the current mirror.

The input resistance is calculated by adding a voltage source V_{in} at the input.

$$i_{in} = g_{ds1}V_{in} + g_{m1}AV_{in} \tag{5.1}$$

The resistance is then

$$r_{in} = \frac{V_{in}}{i_{in}} = \frac{1}{g_{ds1} + Ag_{m1}} \approx \frac{1}{Ag_{m1}} \tag{5.2}$$

The output resistance is given by

$$r_{out} = \left.\frac{V_{out}}{i_{out}}\right|_{i_{in}=0} = \frac{1}{g_{ds2}} \tag{5.3}$$

The ratio is

$$\frac{r_{out}}{r_{in}} = \frac{Ag_{m1}}{g_{ds2}} \tag{5.4}$$

d) Derive the PSRR from the positive supply of the circuit shown inthe figure b. Do not forget to take the bulk-effect into account. No parasitics need to taken into account. Sketch the magnitude of the transfer function with respect to the frequency.

The PSRR is defined as the gain of the circuit from the input to the output divided by the gain from the positive power supply to the output.

The ESSS is shown in Figure 5.3

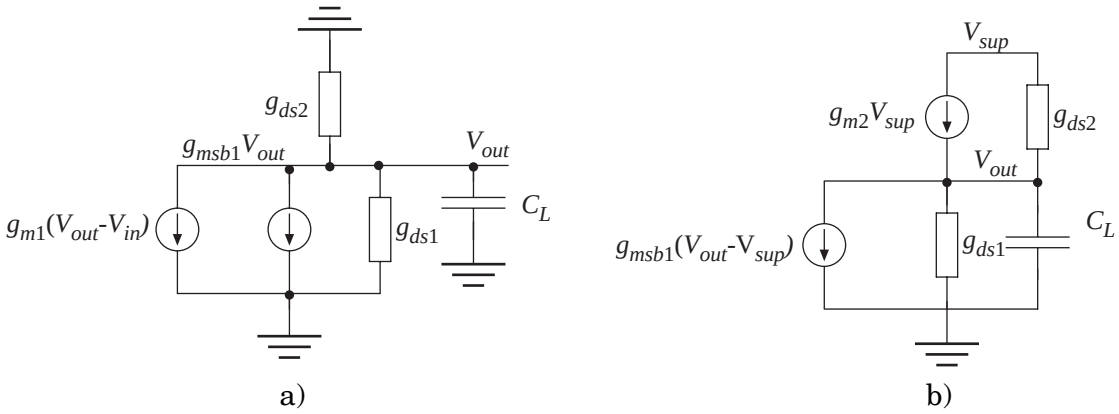


Figure 5.3 The ESSS of the Common Drain circuit from a) the input, b) the positive power supply.

The gain from input to output is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m1} + g_{msb1} + g_{ds1} + g_{ds2} + sC_L} \tag{5.5}$$

and from the power supply to the output is following equation can be solved

$$g_{m2}V_{sup} + (V_{sup} - V_{out})(g_{ds2} + g_{mbs1}) - V_{out}(g_{ds1} + sC_L) = 0 \tag{5.6}$$

where V_{sup} is the power supply variations. The transfer function is given by

$$\frac{V_{out}}{V_{sup}} = \frac{g_{m2} + g_{ds2} + g_{mbs1}}{g_{msb1} + g_{ds1} + g_{ds2} + sC_L} \tag{5.7}$$

The PSRR of the circuit is

$$\frac{\dfrac{V_{out}}{V_{in}}}{\dfrac{V_{out}}{V_{sup}}} = \frac{g_{m1}(g_{msb1} + g_{ds2} + g_{ds1} + sC_L)}{(g_{m2} + g_{ds2} + g_{mbs1})(g_{m1} + g_{msb1} + g_{ds1} + g_{ds2} + sC_L)} = \tag{5.8}$$

$$\frac{g_{m1}(g_{msb1} + g_{ds2} + g_{ds1})}{(g_{m2} + g_{ds2} + g_{mbs1})(g_{m1} + g_{msb1} + g_{ds1} + g_{ds2})} \left(\frac{1 + \dfrac{s}{\dfrac{g_{msb1} + g_{ds2} + g_{ds1}}{C_L}}}{1 + \dfrac{s}{\dfrac{g_{m1} + g_{msb1} + g_{ds1} + g_{ds2}}{C_L}}} \right) \tag{5.9}$$

The graph of the transfer function will start at a value lower than 1, i.e,

$$\frac{g_{m1}(g_{msb1} + g_{ds2} + g_{ds1})}{(g_{m2} + g_{ds2} + g_{mbs1})(g_{m1} + g_{msb1} + g_{ds1} + g_{ds2})} \tag{5.10}$$

and then start to increase since the zero is located a lower frequency than the pole. The curve will then start to decrease until it reaches the value

$$\frac{g_{m1}}{g_{m2} + g_{ds2}} \tag{5.11}$$