Written Test
TSTE80,
Analog and Discrete-time Integrated Circuits

Date	August 22, 2002
Time:	8 - 12
Max. no of points:	70; 40 from written test, 15 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

NOTE: Exercise 6 is only for those that have taken the course before 2002, and have not handed in more than one assignment during the course.

Exercise

1. Large signal modelling

a) Sketch the output voltage for the circuit shown in Figure 1.1. The input voltage is in the interval of *gnd* and V_{DD}. (3p)

b) Derive the minimum and maximum voltage at the input so that the transistor operates in the saturation region. Express these voltages as a function of the other voltages in the circuit but not the current through the transistor. To reduce the computation time in this exercise, ignore the channel-length modulation. (5p)

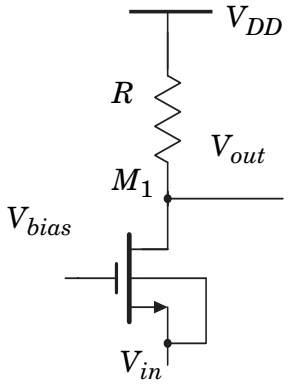

Figure 1.1 A simple gain stage.

2. Basic building block

a) Derive the minimum voltages at nodes V_x, V_y, and V_{out} of the circuit shown in Figure 2.1 so that each transistor operate in the saturation region. Express the voltages in relevant design parameters, such as I_{bias}, α,... (3p)

The amplifier is laid out close to a digital clock network which injects noise through the substrate to the analog parts.

b) Derive the equivalent output noise spectrum from the substrate to the output node. Assume that the substrate noise at the bulk of transistors M_1 and M_2 are uncorrelated and has constant spectral density, S_{sub}. Transistor M_3 is totally shielded from the substrate noise source. Neglect the influence of thermal and flicker noise of the transistors. (5p)

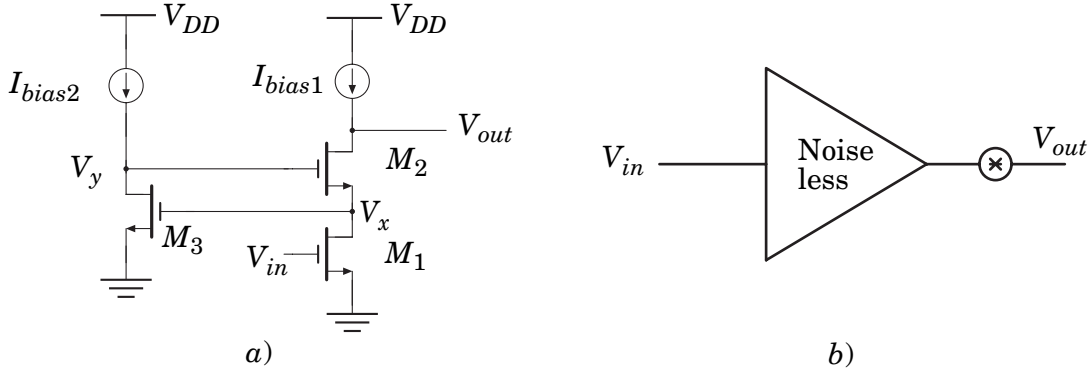

Figure 2.1 a) A CMOS circuit. b) The equivalent output noise model of the circuit.

3. An operational amplifier in a context

a) Derive the DC gain and the poles of the circuit shown in Figure 3.1. Assume that $C_1R_1 > 1/p_1$. Motivate all your approximations carefully. The gain of the amplifier is given by: (6p)

$$A(s) = \frac{A_0}{1 + \frac{s}{p_1}}$$

In an active-RC leapfrog filters the quality of the integrators sets the performance of the filter. Using poor integrators in a filter yields a large deviation compared to the magnitude response from the reference LC-filter. One performance metric of an integrator is its Q-value which is defined as

$$Q = \frac{Im\{H(j\omega)\}}{Re\{H(j\omega)\}} = -\tan\phi(j\omega)$$

where $H(j\omega)$ is the integrators transfer function. In our filter we need to have a Q-factor of at least 100 for the frequency interval of 100kHz to 2MHz.

b) What is the smallest value of the unity-gain frequency of the amplifier to meet a Q-value of at least 100 for the integrator? Assume that the amplifier has very large DC gain. (2p)

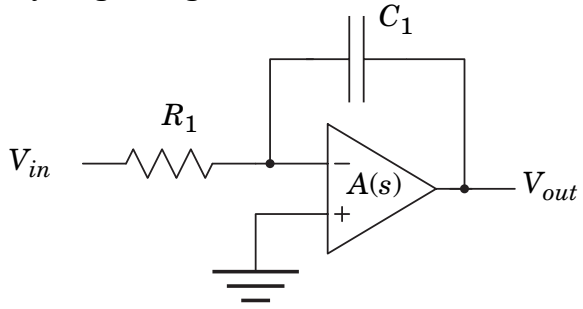

Figure 3.1 An operational amplifier in a context.

4. An SC circuit

A switched capacitor circuit in clock cycle 1 is shown in Figure 4.1.

a) Derive the transfer function for the clock cycle 1 of the switched capacitor circuit shown in Figure 4.1, i.e., $V_{out}(z)/V_{in}(z)$. Assume that the OTA is ideal except that it suffers from an offset voltage, V_{os}. (6p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (2p)

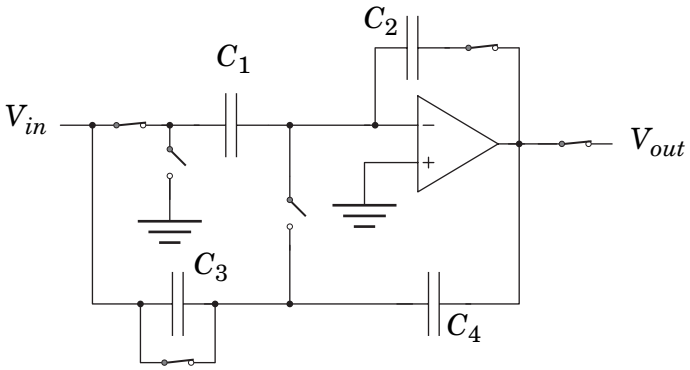

Figure 4.1 A switched capacitor circuit.

5. A mixture of questions

a) In a transconductance-C filter we need to match two capacitors of the values, 100pF and 150pF, respectively. What do you have to do to achieve accurate matching? Sketch a "floor plan" of the capacitor-array to achieve accurate matching between the capacitors. (3p)

b) A differential gain stage as the one shown in Figure 5.1 is to be implemented on silicon. In what types of processes (p-substrate and n-well, n-substrate and p-well, twin well process) is it possible to implement this amplifier? (2p)

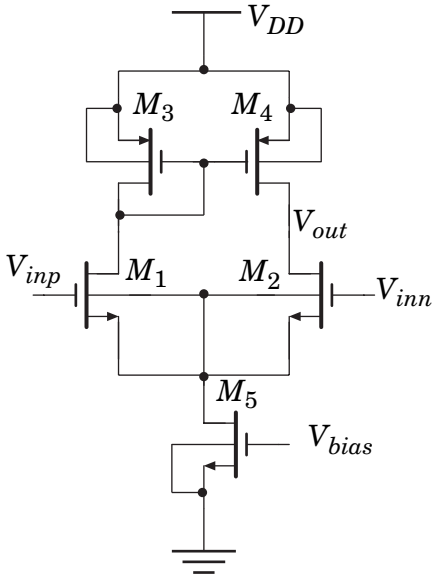

Figure 5.1 A differential gain stage.

c) Derive the power supply rejection ratio from the positive power supply of the amplifier shown in Figure 5.2. Neglect the influence of the capacitive parasitics. (3p)

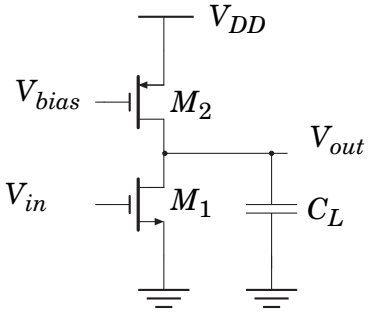

Figure 5.2 A basic building block.

6. Extra exercise

NOTE: This exercise is only for the students that have taken the course before 2002 and not handed in three assignments during the course.

Assume that C_c is smaller than C_L and $W_6 > W_2$.

a) Draw the small signal scheme for the amplifier in Figure 6.1. Do not forget the most important parasitics. (2p)

b) Derive the gain, poles, and zeros of the amplifier. Motivate all the approximations you are doing. (4p)

c) Determine two ways to increase the unity-gain frequency of the amplifier. What will happen to the phase margin, common-mode range, and the DC voltage at node x? (4p)

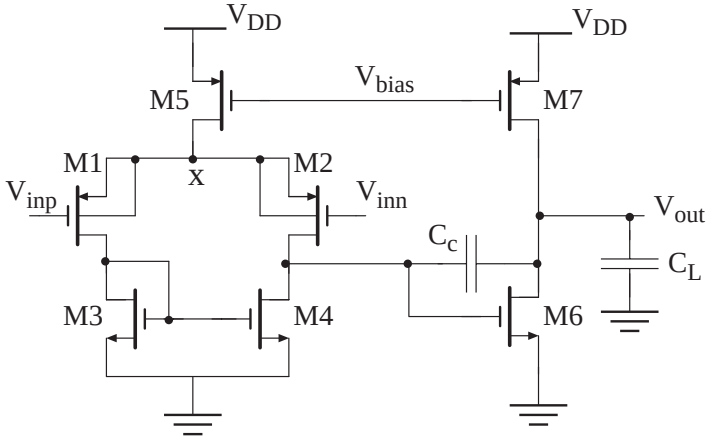

Figure 6.1 Operational transconductance amplifier

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$