# Written Test
# TSTE80,
# Analog and Discrete-time Integrated Circuits

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| Date | August 16, 2001 |
| Time: | 14 - 18 |
| Place: | Garnisonen |
| Max. no of points: | 70;<br>50 from written test,<br>15 for project, and 5 the assignment. |
| Grades: | 30 for 3, 42 for 4, and 56 for 5. |
| Allowed material: | All types of calculators except Lap Tops. All types of tables and handbooks. Written material and downloaded web-material except old exams.<br>No textbooks are allowed. |
| Examiner: | Lars Wanhammar. |
| Responsible teacher: | Robert Hägglund.<br>Tel.: 013 - 28 16 76 (3). |
| Correct (?) solutions: | Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor. |

# Good Luck!

# Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

# Exercise

**1. Basic CMOS building block**

a) Assume that $V_{b3}$ is connected to ground. Determine the gain, poles, and zeros of the circuit shown in Figure 1.1. The only parasitic capacitance to consider is $C_{gs}$ of M3. The load capacitance is much larger than all parasitics. (4p)

b) Derive an expression for the possible input swing of the circuit shown in Figure 1.1. Use relevant design parameters such as W, L, ... (2p)

c) Now assume that M3 is biased in the triode region. What will happen to the gain of the circuit when $V_{b3}$ is varied? Why do we do build this type of circuit? (4p)

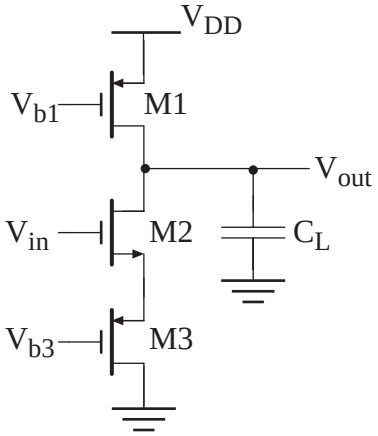


***Figure 1.1*** CMOS building blocks

## 2. Operational amplifier

Assume that $C_c$ is smaller than $C_L$ and $W_6 > W_2$.

a) Draw the small signal scheme for the amplifier in Figure 2.1. Do not forget the most important parasitics. (2p)

b) Derive the gain, poles, and zeros of the amplifier. Motivate all the approximations you are doing. (4p)

c) Determine two ways to increase the unity-gain frequency of the amplifier. What will happen to the phase margin, common-mode range, and the DC voltage at node x? (4p)

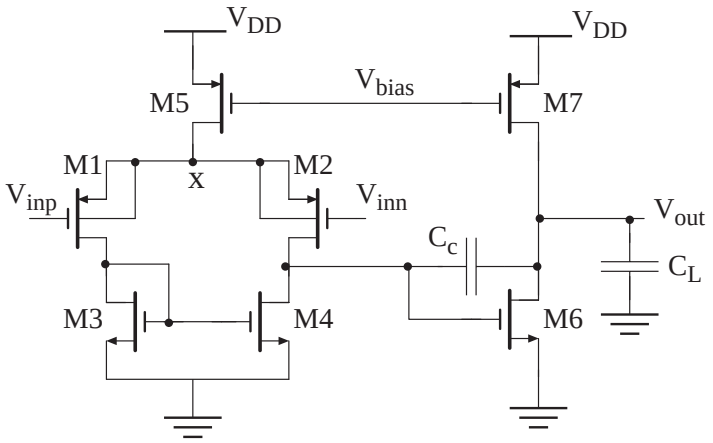


***Figure 2.1*** Operational transconductance amplifier

## 3. Noise in CMOS circuits

A good model for the thermal noise in a transistor is to add a noise source in parallel with the transistor as shown in Figure 3.1. The noise in the drain is given by

$$I_d^2(f) = 4kT\left(\frac{2}{3}\right)g_m$$

**Use this model in this exercise**!

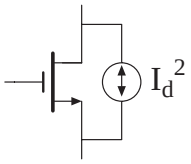


***Figure 3.1*** Thermal noise model for a MOS transistor

a) Derive the total thermal output noise power of the circuit shown in Figure 3.2. All parasitics are much smaller than $C_L$. The spectral density function for a parallel current source for the resistor is given by $I_R^2(f) = 4kT/R$ (4p)

b) Describe two ways to decrease the thermal output noise power of the circuit shown in Figure 3.2 by changing relevant design parameters. What will happen to the gain and the unity-gain frequency? (2p)

c) Add a large capacitor $C_1 \gg C_L$ in parallel with the resistor. Furthermore assume that $1/R \ll g_{out}$. What will happen to the output noise power? (4p)

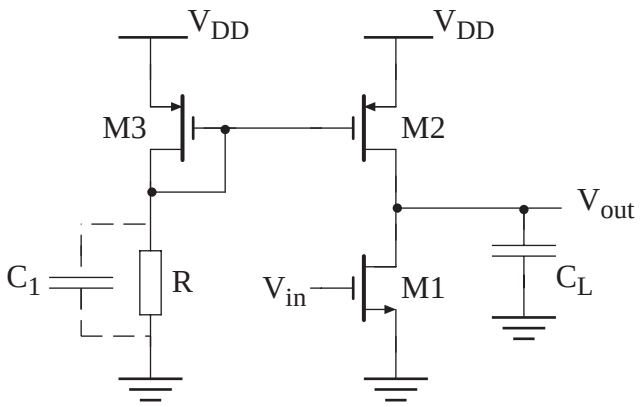


***Figure 3.2*** A noisy common source gain stage

## 4. Switched capacitor

The operational transconductance amplifier suffers from finite gain, $A$, and input offset voltage, $V_{os}$.

a) Derive the transfer function of the switched capacitor circuit shown in Figure 4.1, i.e. $V_2(z)/V_1(z)$. (4p)

b) Is the circuit insensitive to parasitics? Motivate your answer carefully. (2p)

c) Find the settling time constants, i.e. the speed of the circuit, for both clock phases. Neglect the influence of the switches. (4p)

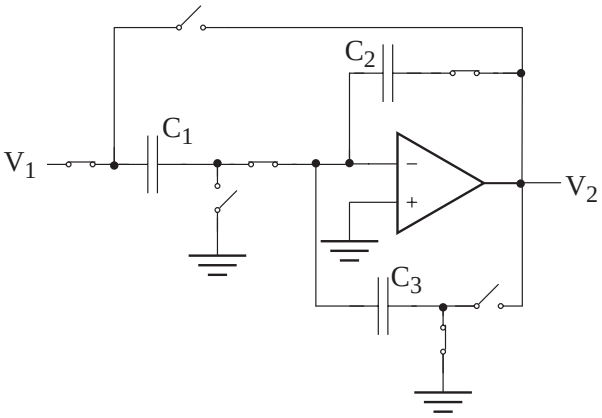


***Figure 4.1*** A switched capacitor circuit

## 5. CMOS Building blocks

a) Determine the common-mode range and the maximum swing of the control signal, $V_{cnrtl}$, of the common-mode feedback circuit shown in Figure 5.1. Use relevant design parameter such as W, L, ... (2p)

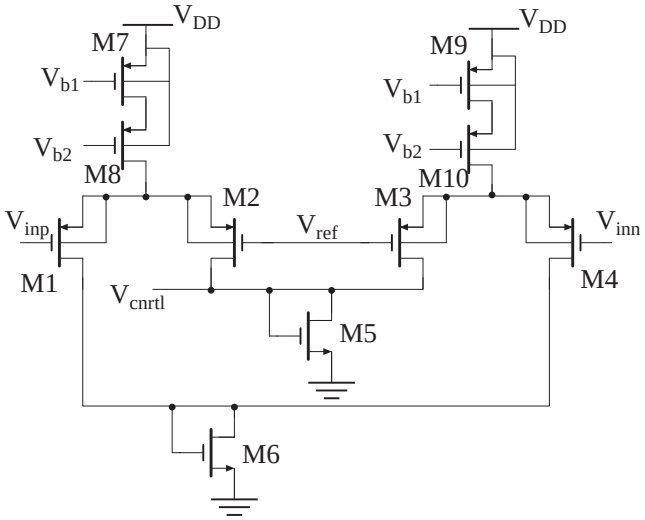


***Figure 5.1*** A common-mode feedback circuit

b) Determine the output resistance of the circuit in Figure 5.2. (3p)

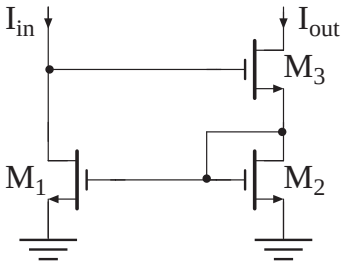


***Figure 5.2*** A current mirror

c) Sketch the output signal of the circuit in Figure 5.3 as a function of the input signal, when the input signal ramps from ground to $V_{DD}$. Determine the input voltages where the operation region of the transistor is changing. Assume $R_L = R_S$. (3p)

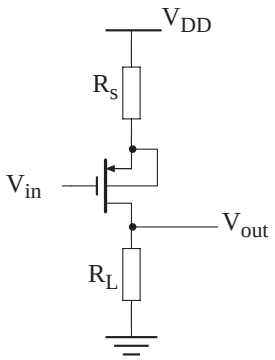


***Figure 5.3*** An analog building block

d) Explain the concept of clock feedthrough. Why is it a problem in SC-circuits? (2p)

# Transistor formulas and noise

## CMOS transistors

### Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

### Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

## Circuit noise

### Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

### Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox} f}$$