Written Test
TSTE80, Analog and Discrete-time Integrated Circuits

Date:	June 9, 2000
Time:	8 - 12
Place:	Garnisonen
Max. no of points:	70; 50 from written test, 15 for project and 5 for oral test.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	No laptops. No text books, such as Johns & Martin "*Analog Integrated Circuit Design*". No dedicated compendia, such as Eriksson "*Aktiva RC-filter och SC-filter*". Pocket calculators are allowed. Written material, tables, downloaded web-material, etc., are allowed.
Examiner:	Lars Wanhammar
Responsible teacher:	J. Jacob Wikner. Tel.: 0705915938
Correct (?) solutions:	Solutions and results will be displayed in July 2000.

Good Luck!

Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no on a brief question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may answer in Swedish, German, or English.

Exercises

1. CMOS Building Blocks

Consider the CMOS building block in Figure 1. This is a gain-boosting circuit and from the name we obviously understand that the gain is increased. The current sources have an infinite output resistance.

a) Express the small-signal gain from the input to the output (V_{in} to V_{out}) as a function of the bias currents, transistor sizes and process parameters. (3p.)

b) Consider the gate-source capacitances on M2 and M3 (assume that they are equally large). Use relevant design parameters to determine at which frequencies the gain-boosting no longer will increase the gain? (7p.)

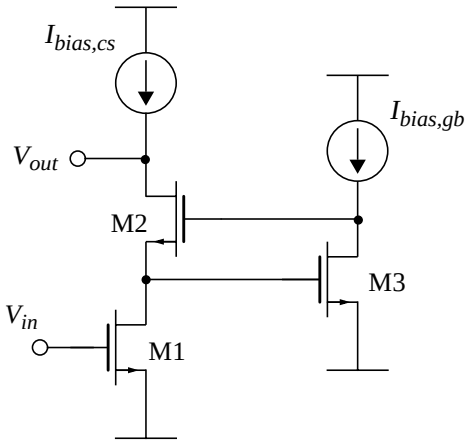

Figure 1 Gain-boosting circuit.

10 points

2. Operational Amplifier

Assume we have a single-stage symmetric OP with CMOS input transistors as illustrated in Figure 2 (a). Further assume that the OP can be connected as the buffer in Figure 2 (b). Notice that there is no external load capacitance. All channel lengths are equal and all bulks are connected to the corresponding sources. Neglect the bulk capacitances (coarse approximation) and assume that $L_{ov} \approx L/8$.

a) Assume that there is a matching error on transistor M2, hence $W_2 = W_1 + \Delta W$. How large input offset voltage would this correspond to? (Do not forget the sign.) (3p.)

b) What is required for linear settling in the configuration in Figure 2 (b)? Motivate your answer and use *relevant* design parameters! (5p.)

c) What is the highest input common-mode voltage that guarantees that all transistors are in their saturation region? (2p.)

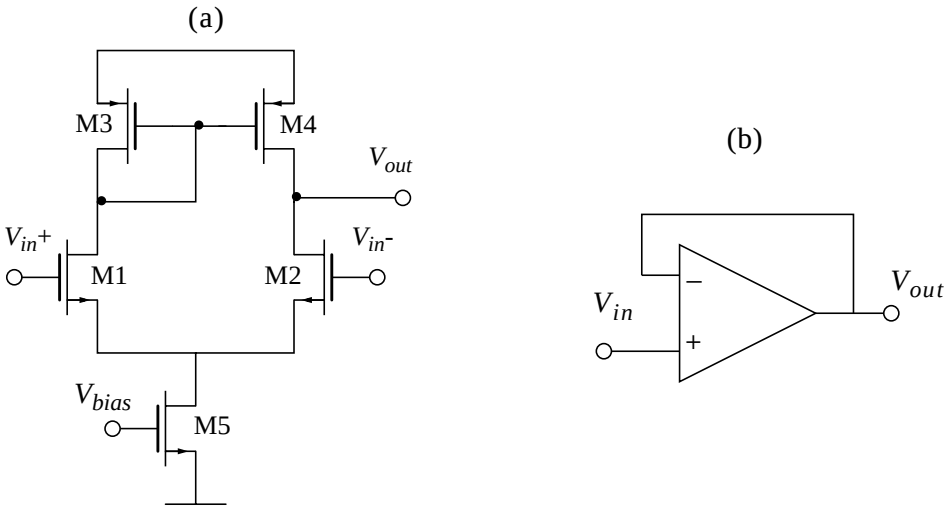

Figure 2 (a) CMOS operational amplifier and (b) in a buffer configuration.

10 points

3. Noise

Consider the common-source circuit in Figure 3. Only consider thermal noise from each transistor but also the noise sources on the bulks of the transistors. Further we have that the bulk noise sources have a noise spectral density given by $S_{bni}(f) = S_0$. The circuit has a pure capacitive load.

a) Derive the total output noise power. (4p.)

b) Derive the total equivalent input-referred noise. Hence, assume no internal noise and only one noise source at the input transistor. (2p.)

c) Use relevant circuit parameters to motivate how you should minimize the output noise power and how this affects the gain and bandwidth of the circuit. (4p.)

10 points

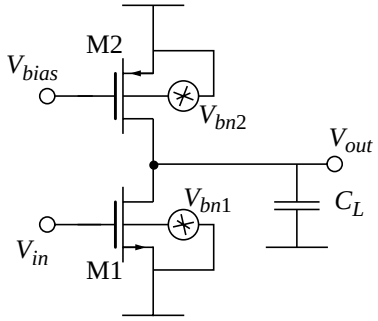

Figure 3 Noisy common-source circuit.

4. Switched Capacitor

Consider the switched-capacitor circuit in Figure 4. Assume that the operational transconductance amplifier suffers from an input offset voltage and that it has a transfer function given by

$$A(s) = \frac{A_0}{1 + s/p_1} = \frac{g_m/g_{out}}{1 + \dfrac{s}{g_{out}/C_{out}}}$$

where g_{out} is the output conductance, g_m is the transconductance and C_{out} is the capacitance associated with the output of the amplifier. This capacitance may very well vary between the different clock phases.

a) Find the transfer function of the SC circuit and assume that the clock period is long. Sketch the ideal output signal (infinite gain and no input offset voltage) and the non-ideal output signal, hence how does the finite DC gain and input offset voltage affect the result? (4p.)

b) How do the switches affect the speed and stability of the circuit? (2p.)

c) Find the settling time constant for each clock phase. Do not forget parasitics and OTA output impedance or load capacitance. Neglect the influence of the switches. (4p.)

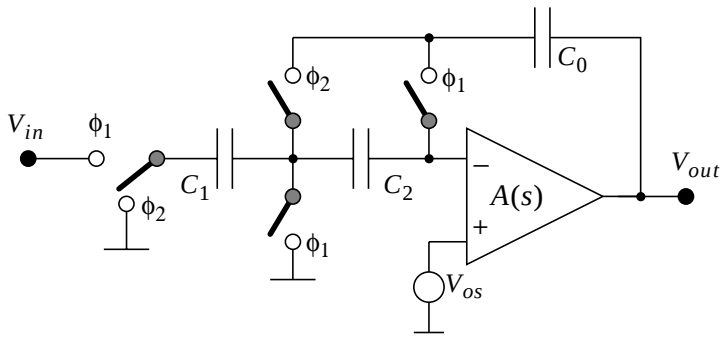

Figure 4 Switched-capacitor circuit.

10 points

5. Surprise – Switched-current circuit

Consider the switched-current circuit in Figure 5. Transistors M1, M3, and M4 are all equally large. Transistor M2 has half the width of M1. ϕ_2 is the inverse clock phase of ϕ_1. The switch controlled by ϕ_3 is used to clear the system. During the first clock period it is opened (not leading current), otherwise it is closed.

a) Find the transfer function of the circuit. (3p.)

b) What are the advantages of using switched-current over switched-capacitor? What are the disadvantages? (3p.)

c) Assume ideal switches (and switching schemes) in a switched-current circuit, such as the one in Figure 5. Discuss the limiting factors on performance and how they appear? (4p.)

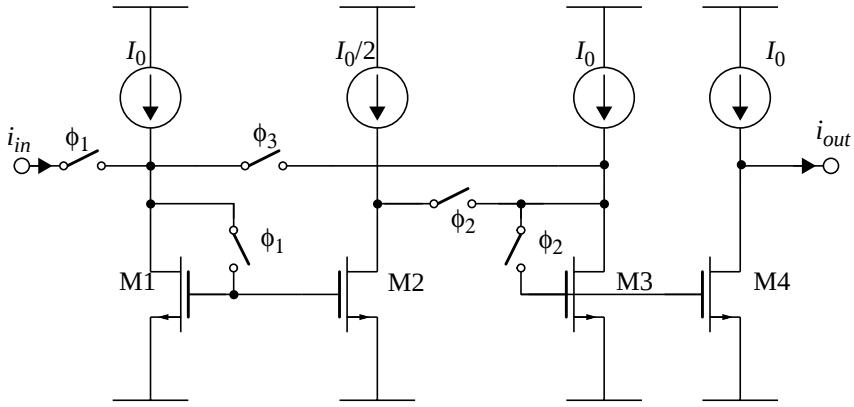

Figure 5 Switched-current circuit.

10 points

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_G - V_T - V_D)$$

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MOS transistor noise

Thermal noise

The thermal noise spectral density at the gate is $\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$

Flicker noise

The flicker noise spectral density at the gate is $\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox} f}$

Parasitics

In the saturation region, the parasitic capacitances on the MOS transistor are approximately given by

$$C_{gs} \approx \frac{2}{3} \cdot W \cdot \left(L + \frac{3}{2} \cdot L_{ov}\right) \cdot C_{ox}, \; C_{gd} \approx WL_{ov} \cdot C_{ox}$$

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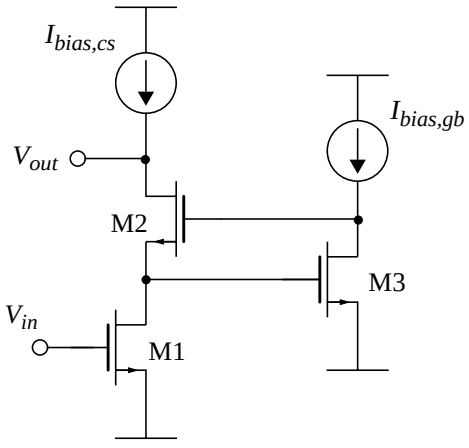

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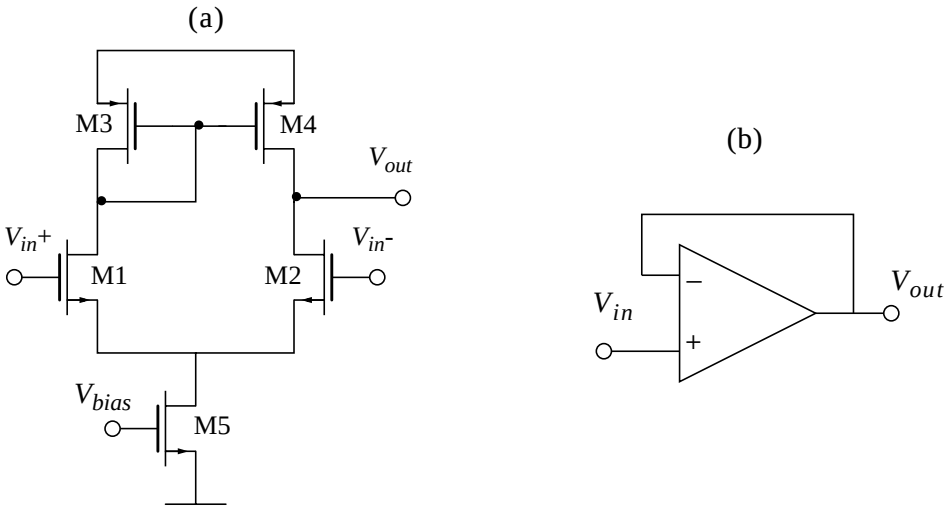

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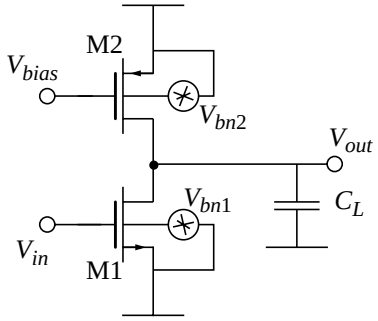

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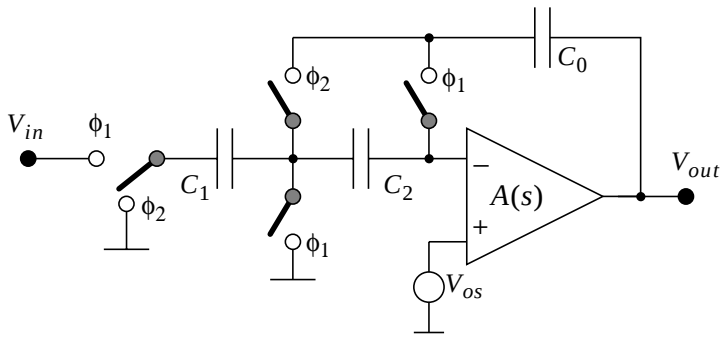

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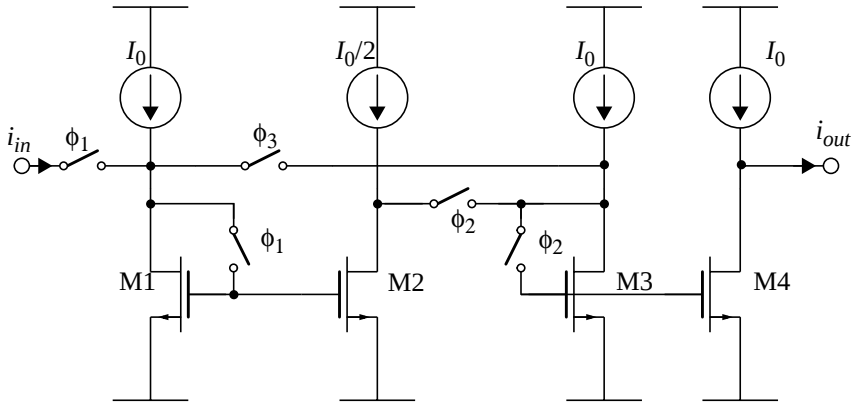

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