Written Test
TSTE80, Analog and Discrete-time Integrated Circuits

Date	May 29, 1999
Time:	9.00 - 13.00 A.M.
Place:	GARN
Max. no of points:	100; 80 from written test, 15 for project, and 5 for oral test.
Grades:	36 for 3, 52 for 4, and 68 for 5.
Allowed material:	Anyone and everyone, but no text books as for example Johns & Martin *"Analog Integrated Circuit Design"*. Pocket calculators are of course allowed.
Examiner:	Lars Wanhammar.
Responsible teacher:	Johan Erlands. Tel.: 070-331 53 76
Correct (?) solutions:	Solutions will not be displayed before June 7. They will be announced in House B, entrance 29, 2nd floor, and published on the Internet.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no on a short question. You always have to answer with figures, formulas, etc., otherwise no points will be given.

Basically, there are few numerical answers to be given in this test.

You may write in Swedish, German, or English.

The points you achieve on the test will be displayed when a majority of all groups have finished and presented their project reports, however not before June 7.

Questions

1. Basic CMOS.

Consider the circuit in Figure 1.1.

a) Which parasitic capacitances dominate on the transistor? How large are they approximately?

b) Derive the transistor's operation regions as a function of the input voltage (and other vital parameters) as the input voltage, V_{in}, varies from 0 to Vdd.

c) In the same way, estimate the transconductance g_m of the transistor as function of the input voltage.

d) Why should we in analog circuits try to keep the transistors in their saturation region?

8 points

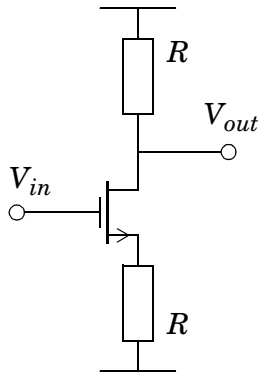

Figure 1.1 NMOS transistor with load. Supply voltages are 0 and Vdd.

2. Basic CMOS Circuits I.

Consider the circuit configuration in Figure 2.1. Ignore the body effects. The load capacitance, C_L, is the dominant capacitive load in the circuit. The circuit is tuned to have a proper operating point.

a) Describe briefly the properties and usage of transistor M1, M2, and M3, respectively.

b) How is the gain changed when V_{bias2} is changed?

c) Explain and show two ways to increase the dc gain by a factor two. Also explain what then happens to the unity-gain frequency and bandwidth.

8 points

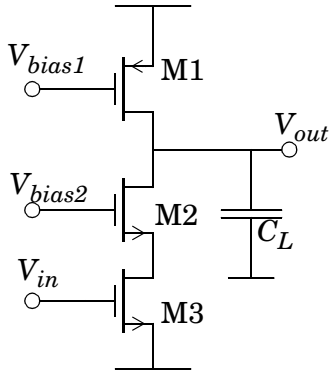

Figure 2.1 CMOS circuit. The supply voltages are 0 and V_{dd}.

3. Basic CMOS Circuits II.

Consider the special circuit in Figure 3.1 below.

a) What happens to the dc gain from V_{in} to V_{out} if I_{bias1} is doubled?

b) What happens to the dc gain if I_{bias2} is doubled?

c) Which are the minimum output and input voltages that guarantee that all transistors are in their saturation region?

d) What is this circuit configuration called?

8 points

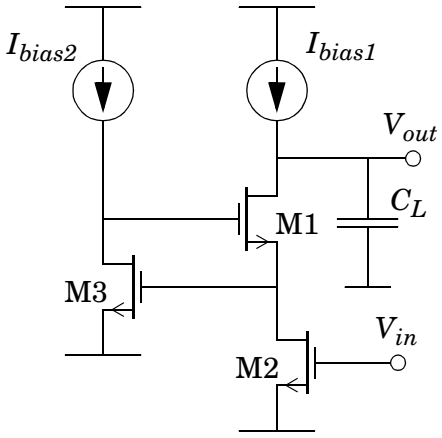

Figure 3.1 CMOS circuit.

4. Noise.

Consider the circuit in Figure 4.1. Neglect the effects of source to bulk voltage variations. The load capacitance, C_L, is the dominant capacitance.

a) Describe (not only the formula) the two most dominating noise sources in common analog CMOS circuits for telecommunications.

b) Assume that the input noise (transistor M1) is only given by thermal noise. Derive the *total output noise power* on node V_{out}.

c) How is the SNR affected when you change the bias current through the circuit?

8 points

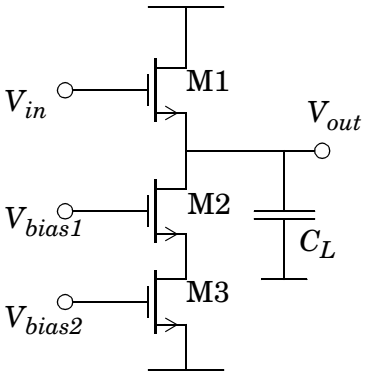

Figure 4.1 CMOS circuit.

5. Amplifiers and Operational Amplifiers.

a) With a macromodel, describe the ideal operational amplifier. What is the input and output impedance? What would be the macromodel for a common CMOS operational amplifier?

b) Assume a single-pole system:

$$V_{out}(s) = \frac{A_0}{1 + s/p_1} \cdot V_{in}(s) \qquad (5.1)$$

Describe the relationship between bandwidth, dc gain, unity-gain frequency, and phase margin.

c) Derive the bandwidth of the circuit in Figure 5.1. The opamp transfer function is given by Eq. (5.1).

8 points

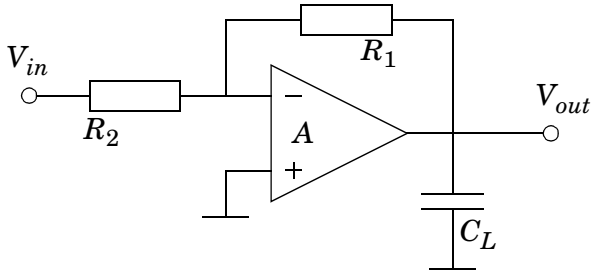

Figure 5.1 Operational amplifier used in a feedback configuration.

6. Transconductance Elements.

a) With a macromodel, describe the ideal transconductor. What is the input and output impedance?

b) Realize the system function below with transconductors and capacitors.

$$H(s) = A \cdot \frac{(s - 0.5)}{(s + 0.8)(s + 0.3)} \tag{6.1}$$

c) Show two different ways to handle the integration capacitance of a fully-differential transconductance-C integrator.

8 points

7. Continuous-Time Filters.

a) Compare a Gm-C filter with an active-RC filter fulfilling the same filter specification. Consider the power dissipaton, chip area, accuracy, speed, and complexity.

b) Scale the filter and find the new resistance values of the RC-filter in Figure 7.1. The scaling factors should be chosen so that the maximum *(over all frequencies)* absolute voltage gain from the input node to each opamp output node is 1. Also explain why you should scale the filter and how the scaling affects transfer function and performance. Initially, all resistances have the value $R_i = 1\Omega$ and the capacitance has the value $C_2 = 1\,\mathrm{F}$.

8 points

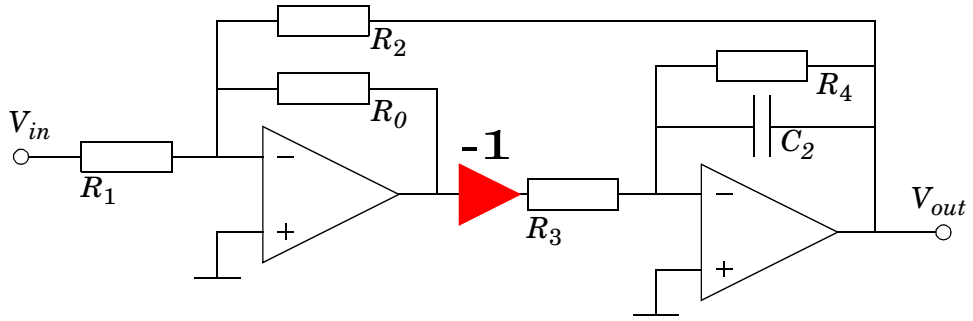

Figure 7.1 Active-RC filter implementation. Note the ideal inverter.

8. Switched-Capacitor Circuits.

Consider the SC circuit in Figure 8.1.

a) Derive the transfer function from inputs to the output of the circuit. What kind of circuit is this?

b) What happens with the transfer function if the operational amplifier has a finite gain? Simply, derive the transfer function if the amplitude is A.

c) Is the circuit insensitive to parasitics? Explain!

8 points

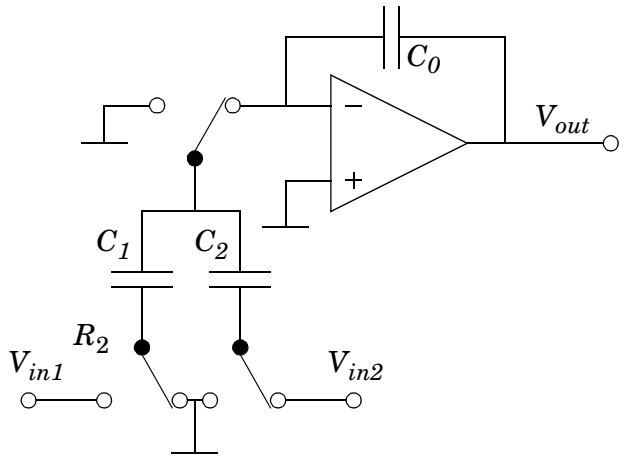

Figure 8.1 Switched capacitor circuit.

9. Switched-Capacitor Filters.

a) Describe the difference between the bilinear transform and the lossless discrete integrator transform. Advantages and disadvantages please.

b) Realize the transfer function in Eq. (9.1) below with SC circuits and using the *system function approach* or *biquad sections*. Describe the advantages and disadvantages of these different techniques. Be precise with the notation of clock phases.

$$H(z) = \frac{z}{(z-0.2)\cdot(z-0.3)} \tag{9.1}$$

Note. Somewhat tricky question. But if you show some effort there will be some points.

8 points

10. Data Converters.

a) What is DNL and INL? Show the definitions. What do these measures describe?

b) What is the difference between dynamic and static errors?

c) If you want to reach an SNR of 110dB for a 14-bit oversampled converter. How many times do you have to oversample assuming you have ideal filters?

8 points

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off: $V_{GS} < V_T$ $\quad I_D \approx 0$

Linear: $V_{GS} - V_T > V_{DS} > 0$ $\quad I_D \approx \frac{\mu_0 C_{ox}}{2}\left(\frac{W}{L}\right)(2(V_{GS} - V_T) - V_{DS})V_{DS}$

Saturation: $0 < V_{GS} - V_T < V_{DS}$ $\quad I_D \approx \frac{\mu_0 C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS})$

Small-signal parameters

Linear region: $g_m \approx (\mu_0 C_{ox})\left(\frac{W}{L}\right)V_{DS}$ $\quad g_{ds} \approx (\mu_0 C_{ox})\left(\frac{W}{L}\right)(V_G - V_T - V_D)$

Saturation region: $g_m = \frac{dI_D}{dV_{GS}} = \sqrt{\mu_0 C_{ox}(W/L)I_D}$ $\quad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is $\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is $\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$