Written Test TSTE08 and TSTE80,
Analog and Discrete-time Integrated Circuits

Date:	August 21, 2008
Time:	14-18
Place:	TER2
Max.no. of points:	25
Grades:	10p for 3, 15p for 4, and 20p for 5.
Allowed material:	All types of calcuclators except laptops. All types of official tables and handbooks. Textbooks: Johns & Martin: Analog Integrated Circuit Design. Razavi: Design of Analog CMOS Integrated Circuits. Sedra&Smith: Microelectronic Circuits. Dictionaries.
Examiner:	Sune Söderkvist
Responsible teacher:	Sune Söderkvist. Tel.: 281355.
Corrrect (?) solutions:	Solutions and results will be displayed in House B, entrance 25-27, ground floor. Solutions also will be on the webb home page.

Graded exams are returned on examinator's office times, tuesdays and fridays at 11.00-13.00, during week no. 36 - 38.

Students instructions

- The CMOS transistor operation regions, small-signal parameters, and noise characteristics are found on the last page of this exam.
- Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas etc., otherwise no or fewer points will be given.
- You may write down your answers in Swedish or English.

Good Luck!

Exercise 1.

Th circuit in **Figure 1** shows an inverter, which shall generate the output voltage $V_{out} = 0.03$ V when the input voltage is $V_{in} = 3$ V. The current through the transistors should be 20 nA. $V_{DD} = 3$ V and $V_B = 1$ V.

Determine the widths of the gates W_1 and W_2 for transistors **M1** and **M2** meeting specifications above.

Parameter values for the transistors are:

	N-channel	P-channel
L	1 μm	1 μm
V_t	0.5 V	0.6 V
$\mu_0 C_{ox}$	20 nA/V^2	6 nA/V^2
λ	0.03 V^{-1}	0.05 V^{-1}

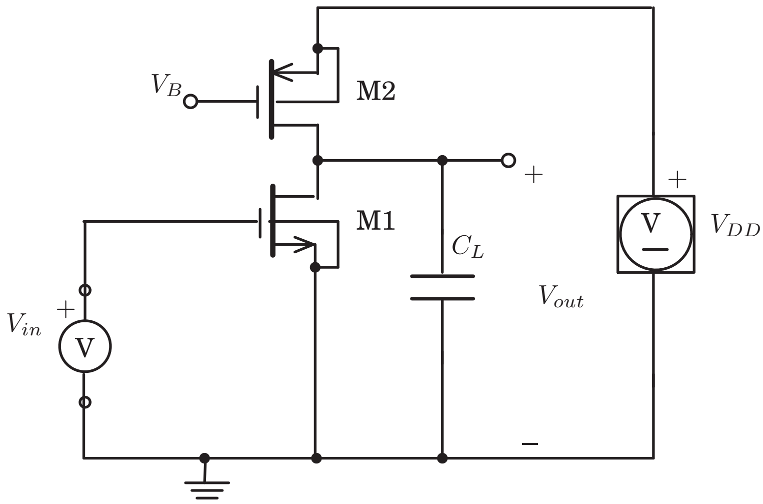


Figure 1: Inverter.

Exercise 2.

Figure 2a shows another type of CMOS-inverter, compared to the one we used in previous example. Now we will study the small-signal properties of this inverter. **Figur 2b** shows a beginning of a small signal equivalent.

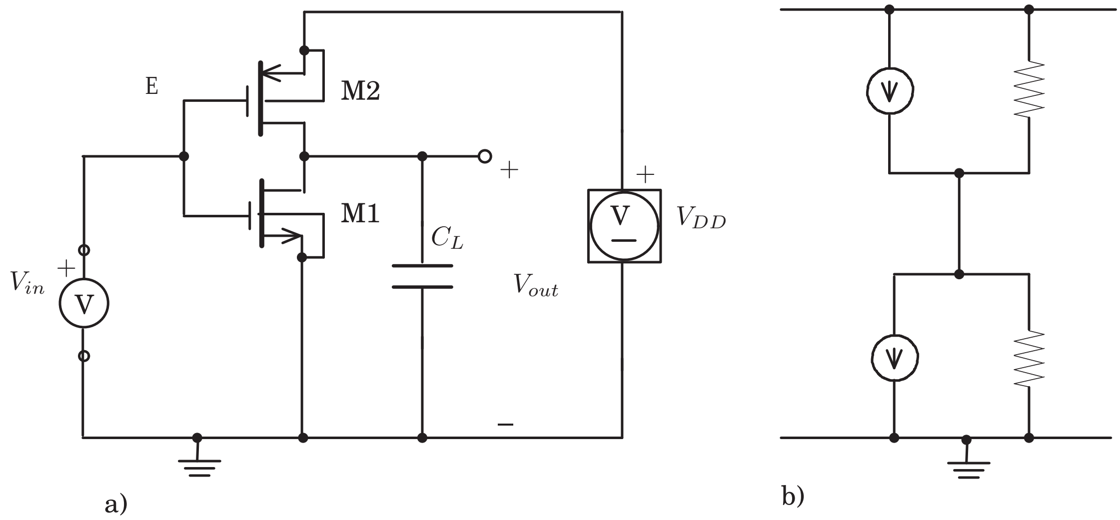
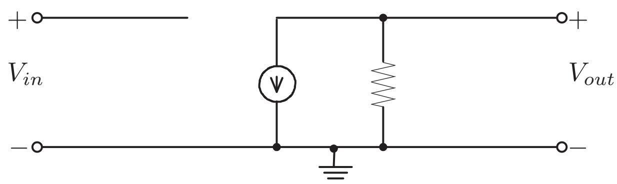


Figure 2: a) CMOS-inverter. b) Beginning of a small signal equivalent.

a) First, complete the small-signal equivalent in **Figure 2b**. Mark out drains (D1, D2), gates (G1, G2) and sources (S1, S2) of both transistors, introduce notations for different circuit elements and introduce all voltages of interest V_{in}, V_{gs1}, V_{sg2} etc. to complete the small signal equivalent. All capacitanses except C_L can be neglected. (V_{DD} is an ideal voltage source.) (2p)

b) Simplify the complete small signal equivalent from a), to receive the shape below. Then determine the transfer function V_{out}/V_{in} expressed in g_{m1}, g_{m2}, g_{ds1} and g_{ds2}. (2p)



c) Determine DC gain and ”unity-gain frequency” ω_u for this gain stage. (1p)

Exercise 3.

Now we will study a differential gain stage feeded by a square-shape pulse on V_{INP} and a inverted square-shape pulse on V_{INN}. **Figure 3 a** shows the first phase, which starts by V_{INP} instantaneously going from 0 to E (which is the height of the square-shape pulse). Simultaneously V_{INN} goes from E to 0. **Figure 3 b** shows the second phase, starting with V_{INP} instantaneously going from E to 0, and simultaneously V_{INN} goes from 0 to E.

The value of E is $E > V_{tn}$. Transistors **M1** and **M3** are identical as well as **M2** and **M4**. I_0 is an independent current source giving the DC current I_0.

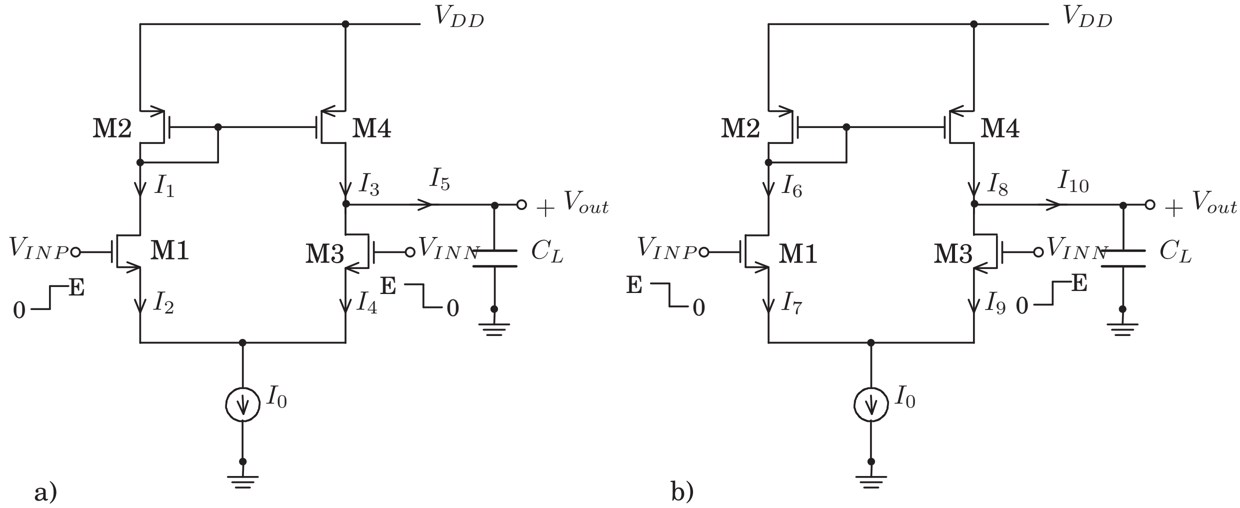


Figure 3: Differential gain stage.

a) Describe how the differential gain stage works in both phases by giving values of the currents I_1, I_2, ... , I_{10} in figures. Motivate shortley the value of each current. (4p)

b) From definition of SR, determine Slew-Rate (SR) for the otput voltage V_{out}. (1p)

Exercise 4.

Here we will study how the termal noise from the transistor **M1** in **Figure 4** affects the output voltage. Thus, your problem is to derive the spectral density R_{out} on the node V_{out} caused by the thermal noise of transistor **M1**. Also, determine corresponding noise power $P_{out,noise}$ on the output.
Hint: First, draw a small signal equivalent and derive the transfer function V_{out}/V_{in}. Then neglect g_{ds} compared to g_m.

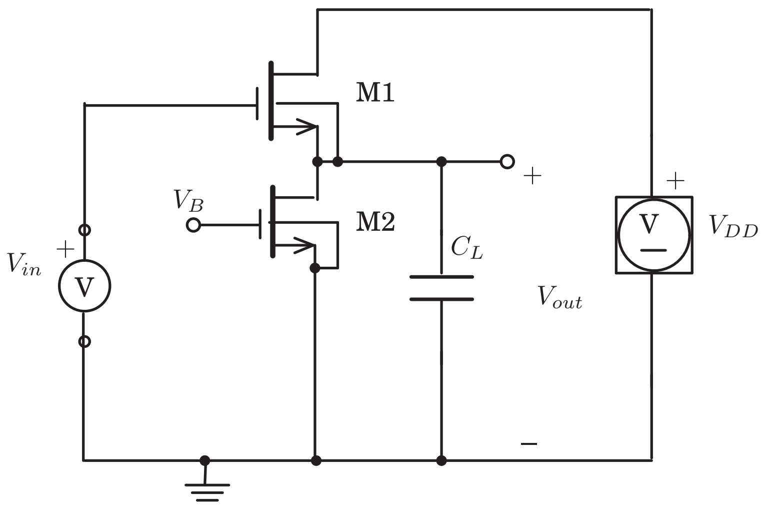


Figure 4: CMOS circuit.

Exercise 5.

a) The relationship between the output voltage v_2 and the input voltage v_1 for the SC-circuit in **Figure 5** can, at $kT = t + \tau$ and $T = 2\tau$, be written as following difference equation

$$v_2(kT) = bv_2(kT - T) + av_1(kT - T)$$

Determine the constansts a and b expressed in C_1 and C_2. What is the function of the circuit?
Assume that the OP-amp. is ideal. (2p)

b) Now, assume that the OP-amp. has a finite gain A and do the same calculus as in a).

I.e. determine the constants a and b expressed in C_1, C_2 and A. The current at the input of the OP-amp. can be neglected. (2p)

c) Explain why the SC-circuit in **Figure 5** is insensitiv for parasitics. Assume that the OP-amp. is ideal. (1p)

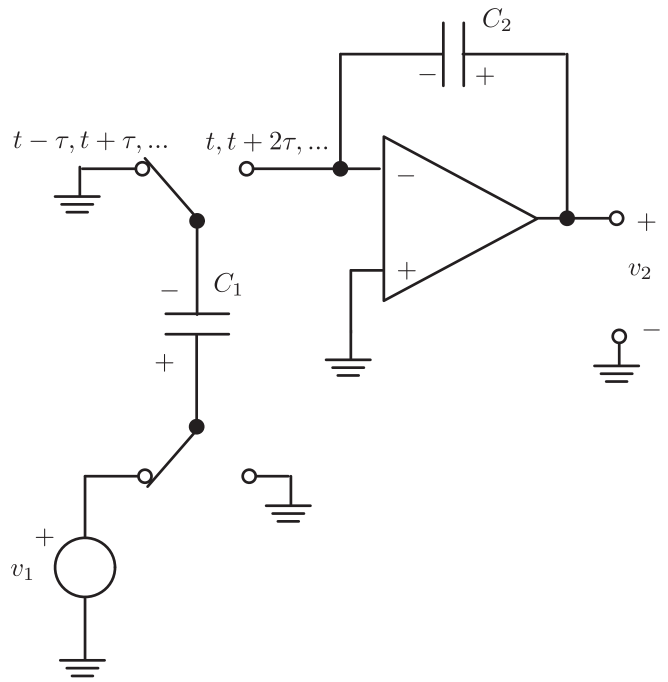


Figure 5: SC-circuit.

Transistor formulas and noise

1 CMOS transistors

Current and threshold voltage formulas and operating regions for an NMOS transistor

Cut-off:	$V_{GS} < V_t$	$I_D \approx 0$
Linear:	$V_{GS} - V_t > V_{DS} > 0$	$I_D = \alpha(2(V_{GS} - V_t) - V_{DS})V_{DS}$
Saturation:	$0 < V_{GS} - V_t < V_{DS}$	$I_D = \alpha(V_{GS} - V_t)^2(1 + \lambda(V_{DS} - V_{eff}))$
	$V_{DSsat} = V_{eff} = V_{GS} - V_t$	
All regions:	$V_t = V_{t,0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})$	

Small-signal parameters

Linear:	$g_m \approx 2\alpha V_{DS}$	$g_{ds} \approx 2\alpha(V_{GS} - V_t - V_{DS})$
Saturation:	$g_m \approx 2\sqrt{\alpha I_D}$	$g_{ds} \approx \lambda I_D$

Constants: $\alpha = \frac{1}{2}\mu_{0n}C_{ox}\frac{W}{L}$ $\quad \lambda = \sqrt{\frac{K_s\epsilon_0}{2qN_A\phi_0}} \cdot \frac{1}{L}$ $\quad \gamma = \frac{\sqrt{2qN_AK_s\epsilon_0}}{C_{ox}}$

2 Circuit noise

Thermal noise in CMOS transistors
The thermal noise spectral density at the gate of a CMOS transistor is

$$V^2(f) = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Thermal noise in resistors
The thermal noise spectral density of a resistor is modeled as a parallel noise current source

$$I^2(f) = \frac{4kT}{R}$$

Flicker noise in CMOS transistors
The flicker noise spectral density at the gate of a CMOS transistor is

$$V^2(f) = \frac{K}{WLC_{ox}f}$$