Written Test TSTE08 and TSTE80, Analog and Discrete-time Integrated Circuits

Date:	June 05, 2008
Time:	14-18
Place:	T2
Max.no. of points:	25
Grades:	10p for 3, 15p for 4, and 20p for 5.
Allowed material:	All types of calcuclators except laptops. All types of official tables and handbooks. Textbooks: Johns & Martin: Analog Integrated Circuit Design. Razavi: Design of Analog CMOS Integrated Circuits. Sedra&Smith: Microelectronic Circuits. Dictionaries.
Examiner:	Sune Söderkvist
Responsible teacher:	Sune Söderkvist. Tel.: 281355.
Corrrect (?) solutions:	Solutions and results will be displayed in House B, entrance 25-27, ground floor. Solutions will also be shown at the webb home page.

Graded exams are returned at 11.00-13.00 o'clock: tuesday June 17, friday August 15 and tuesday August 19.

Students instructions

- The CMOS transistor operation regions, small-signal parameters, and noise characteristics are found on the last page of this exam.
- Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas etc., otherwise no or fewer points will be given.
- You may write down your answers in Swedish or English.

Good Luck!

Exercise 1.

The circuit in **Figure 1** is a commonly used structure when designing analog circuits. Transistor **M1** is assumed to be biased in saturation. Also assume that the W/L ratio of transistor **M2** is K times larger than that of transistor **M1**. The channel-length modulation can be neglected.

a) Derive the output voltage V_{out} as a function of the factor K, i.e. $V_{out} = f(K)$ when also **M2** is saturated. Express V_{out} in terms of the current I_0 and transistor design parameters, but not voltages. (3p)

b) Determine for which value of K transistor **M2** switches from operating in the saturation region to the linear region. (2p)

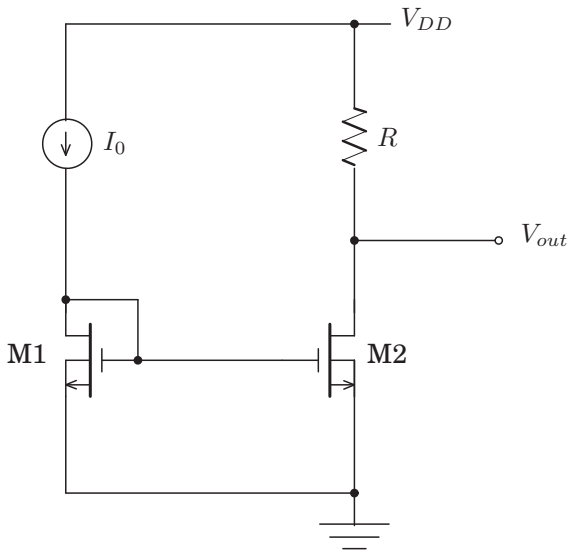

Figure 1: A commonly used analog circuit.

Exercise 2.

Figure 2 shows a common-source amplifier, where **M1** acts like a current source giving the DC current I_D and **M2** is a cascode transistor, which decreases the output resistance and also reduces the effect of the Miller capacitance from input to output. All transistors are biased to operate in the saturation region. Assume that the transistors small-signal parameters are g_{m1}, g_{ds1}, g_{m2}, g_{ds2} and g_{m3}, g_{ds3} respectively. The body effects can be neglected.

a) Sketch a small-signal equivalent circuit and determine an exact expression for the transfer function $H(s) = V_{out}(s)/V_{in}(s)$. All capacitors but C_L can be neglected. (3p)

b) Now assume that $g_{mi} >> g_{dsj}$, $i = 1, 2, 3$ and $j = 1, 2, 3$, to get an approximation of $H(s) = V_{out}(s)/V_{in}(s)$. From this approximative expression, determine the DC gain, the 3-dB cut-off frequency, and the unity-gain frequency. (1p)

c) Express the DC gain in terms of the design parameters W_i, and L_i for the transistors Mi, $i = 1, 2, 3$, and answer following questions (motivate):

How is the DC gain changed: If the current I_D is increased by a factor 4? If the channel-width of transistor $M3$ is increased by a factor 4? Assume that all transistors remain saturated. (1p)

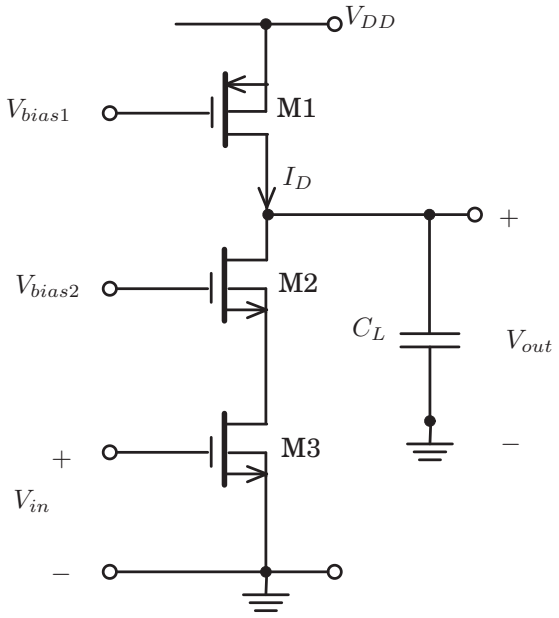

Figure 2: Common source stage with cascode.

Exercise 3.

A switched-capacitor circuit in clock phase 1 is shown in **Figure 3**. The value of V_{in} changes only at time t, $t + 2\tau$, $t + 4\tau$, and so on, i.e., $V_{in}(t) = V_{in}(t + \tau)$.

a) Express the output voltage, $V_{out}(z)$, as a function of the input voltage, $V_{in}(z)$, for clock phase 1. Assume that the operational amplifier is ideal. (4p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (1p)

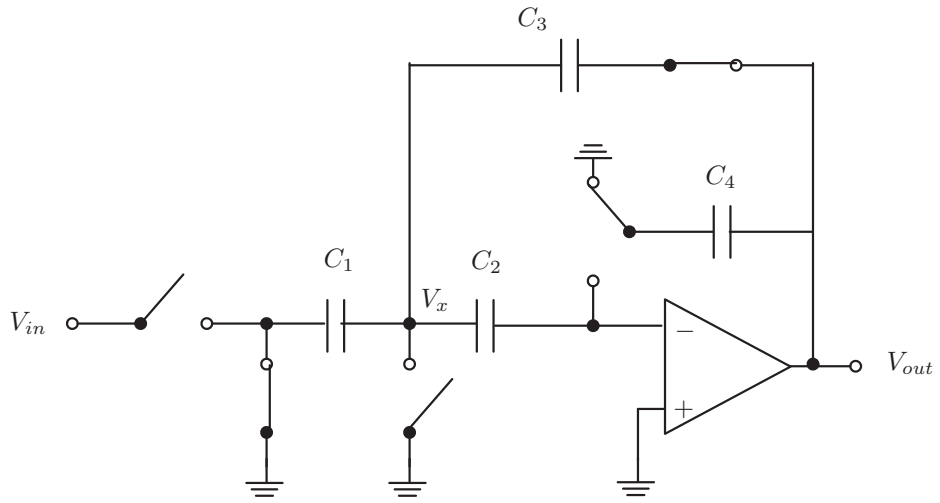

Figure 3: A switched-capacitor circuit in clock phase 1.

Hint: After some work you should find $V_x(t)$ to be zero for all t.

Exercise 4.

Derive the input and output ranges of the amplifier shown in **Figure 4** where all transistors are operating in the saturation region. Furthermore, the transistors in the gain-stage are matched, i.e. **M1** and **M2** are identical, as well as **M3** and **M4**, **M5** and **M8**, and also **M6** and **M7**.
Express the input and output ranges in relevant design parameters; i.e. I_0, α_i and V_{ti}.

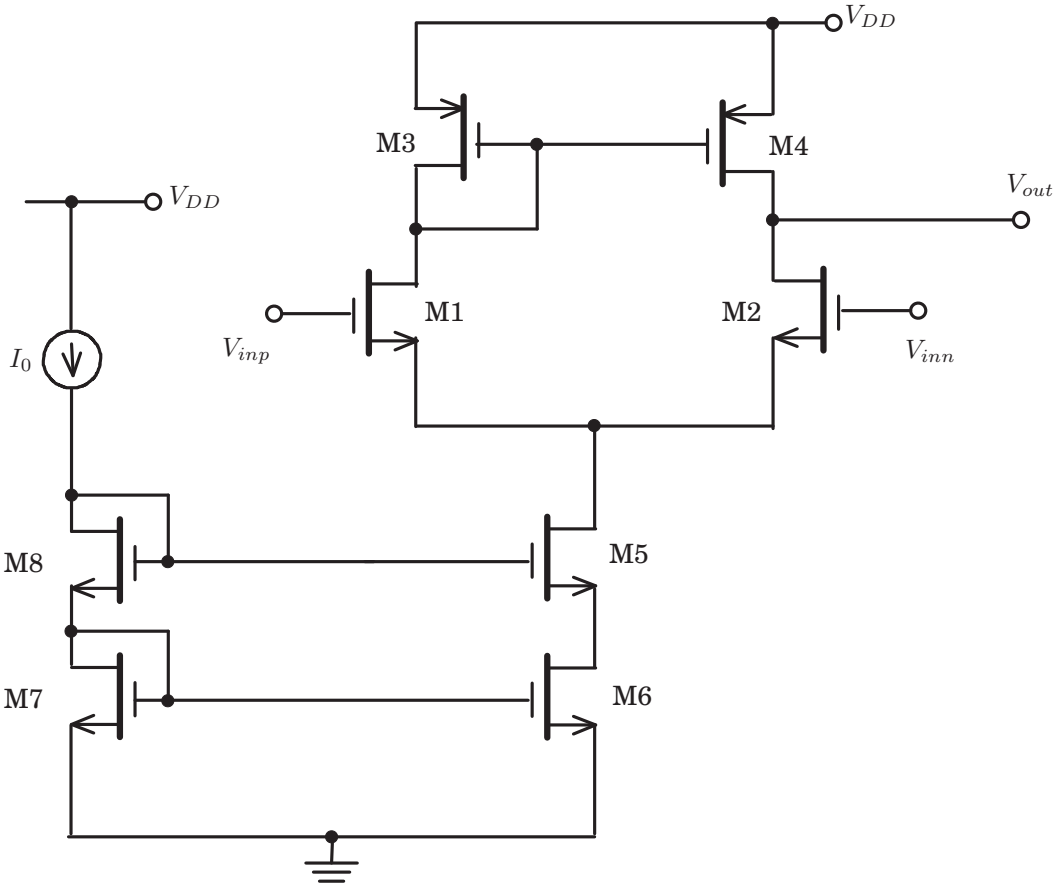

Figure 4: Differential gain-stage.

Exercise 5.

In this exercise we will study the **thermal noise** and the **substrate noise** from the two transistors in the common-souce stage in **Figure 5**. The **substrate noise** is represented by noisy voltage sources V_{sni} with spectral density $R_{sni}(f)$, $i = 1, 2$ in the circuit. Assume that substrate noise is white noise with spectral density $R_{sn}(f) = R_0$. The **thermal noise** you should know, from the course, how to represent. The transistors have small signal parameters g_{m1}, g_{bs1}, g_{ds1} and g_{m2}, g_{bs2}, g_{ds2} respectively.

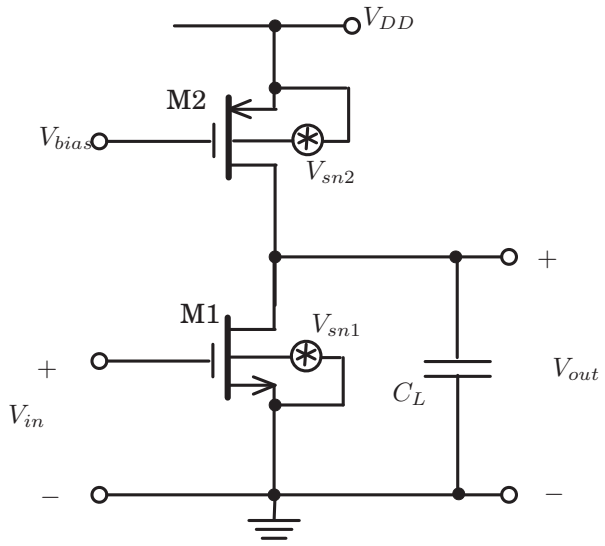

Figure 5: A noisy common-source amplifier.

Your task is to determine an expression for the spectral density R_{out} of the output noise, assuming that the noise from the transistors are uncorrelated. Also assume that thermal noise and substrate noise are uncorrelated. (5p)

Transistor formulas and noise

1 CMOS transistors

Current and threshold voltage formulas and operating regions for an NMOS transistor

Cut-off:	$V_{GS} < V_t$	$I_D \approx 0$
Linear:	$V_{GS} - V_t > V_{DS} > 0$	$I_D = \alpha(2(V_{GS} - V_t) - V_{DS})V_{DS}$
Saturation:	$0 < V_{GS} - V_t < V_{DS}$	$I_D = \alpha(V_{GS} - V_t)^2(1 + \lambda(V_{DS} - V_{eff}))$
	$V_{DSsat} = V_{eff} = V_{GS} - V_t$	
All regions:	$V_t = V_{t,0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})$	

Small-signal parameters

Linear:	$g_m \approx 2\alpha V_{DS}$	$g_{ds} \approx 2\alpha(V_{GS} - V_t - V_{DS})$
Saturation:	$g_m \approx 2\sqrt{\alpha I_D}$	$g_{ds} \approx \lambda I_D$

Constants: $\alpha = \frac{1}{2}\mu_{0n}C_{ox}\frac{W}{L}$ $\lambda = \sqrt{\frac{K_s\epsilon_0}{2qN_A\phi_0}} \cdot \frac{1}{L}$ $\gamma = \frac{\sqrt{2qN_AK_s\epsilon_0}}{C_{ox}}$

2 Circuit noise

Thermal noise in CMOS transistors
The thermal noise spectral density at the gate of a CMOS transistor is

$$R(f) = V^2(f) = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Thermal noise in resistors
The thermal noise spectral density of a resistor is modeled as a parallel noise current source

$$R(f) = I^2(f) = \frac{4kT}{R}$$

Flicker noise in CMOS transistors
The flicker noise spectral density at the gate of a CMOS transistor is

$$R(f) = V^2(f) = \frac{K}{WLC_{ox}f}$$

Noise at the output:

$$R_{out}(f) = \sum_k |H_k(f)|^2 R_{in,k}(f)$$

$$P_{out,noise} = \int_0^\infty R_{out}(f)df$$