TSTE08, Analog and Discrete-time Integrated Circuits, 2011-03-16
Written exam, TENA

Date and time	2011-03-16, 14.00 - 18.00
Location(s)	TER3 (32 copies printed)
Responsible teacher	J Jacob Wikner, jacwi50, +46-70-5915938
Aid	Any written and printed material, including books and old exams. Note! No pocket calculators, no laptops, no iPods, no telephones, no internet connection.
Instructions	A maximum of 25 points can be obtained from the written exam. Three points can be obtained from quizzes. In total: 10 points are required to pass, 15 for a grade four, and 20 for a grade five. ˣ *Hint! **Be strategic** when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...* Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **'hidden"in the text** and therefore: read the instructions carefully! ˣ *Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available by 2011-03-31 (hopefully...)

Outline

1. NOISE (5 P)

✗ *We'll take a simple one this year ...*

Consider the circuit in Figure 1.1. The input voltage, v_{in}, is connected to the PMOS and the current mirror sets the bias current through the active device. Only consider the thermal noise of the transistors.

1) Derive a compact expression of the **total output noise power** for the circuit**!**

2) Derive the **input-referred noise spectral density!**

3) Express and sketch **how the total output noise power depends on the bias current,** I_0 ! Should the current be **minimized or maximized** for minimum noise?

4) How should you **set the mirror ratio** for maintained gain but lower noise?

Make valid assumptions and motivate them well!

✗ ***Finding a compact expressions implies in this context: 'Minimize the number of parameters in your expression."***

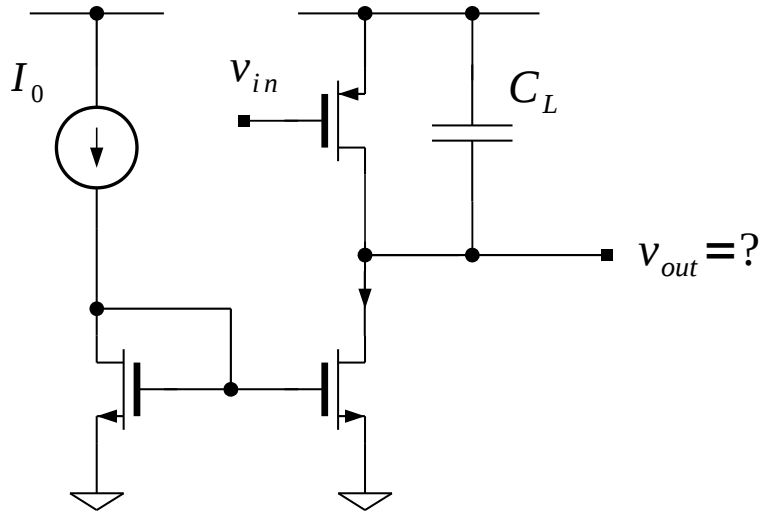

Figure 1.1: Phew! Three transistors...

✗ *Tip! Use symmetries to speed up your conclusions.*

✗ *Don't forget that you have to consider the **total noise power** at the output. Hint: use the noise brickwall bandwidth:* $p_1/4$ *(see for example Johns Martin).*

Solutions

1) Derive a compact expression of the **total output noise power** for the circuit**!**

We have three transistors in the design, all of them are noisy and only thermal noise is to be considered, i.e., the noise models on the gates and between drain and source are

$$v_{ng1}^2(f)=4kT\gamma/g_{mn0} \text{ and } i_{nds1}^2(f)=4kT\gamma\cdot g_{mn0} \quad (1.1)$$

First, since question (4) is there, let the current mirror have an arbitrary mirror ratio, say K.

> *x In fact, the exercise does not give you any details on the current mirror ratio.*

First -- some educational aspects:

Anyway, the noise in the primary branch of the current mirror has to be mirrored to the other side, and that would be dictated by the mirror ratio. The noise source on the gate of the primary side transistor can be "moved" to the gate of the other transistor, but with the K factor squared. In this particular case, I am going to use the current model (above). Notice for the current mirror, we have $I_{out}=K\cdot I_0$ which obviously implies $I_{out}^2=K^2\cdot I_0^2$. The same holds for the noise current then:

$$i_{nds0,out}^2(f)=K^2\cdot i_{nds0}^2(f)=K^2\cdot 4kT\gamma\cdot g_{mn0} \quad (1.2)$$

We know that the current ratio is K, which means that

$$g_{mn0}=\frac{2I_0}{V_{eff}}=\frac{2(I_{out}/K)}{V_{eff}}=\frac{1}{K}\cdot\frac{2I_0}{V_{eff}}=\frac{g_{mn1}}{K} \quad (1.3)$$

Combining these gives us

$$i_{nds0,out}^2(f)=K\cdot 4kT\gamma\cdot g_{mn1} \quad (1.4)$$

So related to the secondary side transistor, the noise is K times larger/smaller than its own current. Let us finally combine this with the g_{mn1} noise:

$$i_{nds,out}^2(f)=i_{nds0,out}^2(f)+i_{nds1,out}^2(f)=(K+1)\cdot 4kT\gamma\cdot g_{mn1} \quad (1.5)$$

Now, let us bring this back to the gate of that secondary side transistor:

$$v_{ng1}^2(f)=\frac{i_{nds,out}^2(f)}{g_{mn1}^2}=(K+1)\cdot\frac{4kT\gamma}{g_{mn1}} \quad (1.6)$$

So, the noise source voltage on the left-hand side can be brought over and multiplied K times and **then referring to the right-hand side transconductance**.

Back to solutions procedure ... due to the symmetry we see two (or three) common source stages. Two are for the NMOS and one is for the PMOS. (Due to the mirror ratio, one of the NMOS will be amplified K times, but let us leave that for now). So we have:

$$v_{tot}^2(f)=v_{np}^2(f)\cdot\left|\frac{g_{mp}/g_{out}}{1+\frac{s}{g_{out}/C_L}}\right|^2+v_{nn1}^2(f)\cdot\left|\frac{g_{mn1}/g_{out}}{1+\frac{s}{g_{out}/C_L}}\right|^2+v_{nn0}^2(f)\cdot\left|\frac{g_{mn1}/g_{out}}{1+\frac{s}{g_{out}/C_L}}\right|^2 \tag{1.7}$$

Then we only care about the total noise power, and we remove the s-stuff in the denominator and multiply with $p_1/4=g_{out}/4C_L$ instead.

$$P_{tot}=v_{tot}^2(f)\cdot p_1/4=v_{np}^2(f)\cdot\frac{g_{mp}^2}{4\,g_{out}C_L}+v_{nn1}^2(f)\cdot\frac{g_{mn1}^2}{4\,g_{out}C_L}+v_{nn0}^2(f)\cdot\frac{g_{mn1}^2}{4\,g_{out}C_L} \tag{1.8}$$

Then we add the noise expressions

$$P_{tot}=\frac{4kT\gamma}{g_{mp}}\cdot\frac{g_{mp}^2}{4\,g_{out}C_L}+\frac{4kT\gamma}{g_{mn1}}\cdot\frac{g_{mn1}^2}{4\,g_{out}C_L}+\frac{4kT\gamma}{g_{mn0}}\cdot\frac{g_{mn1}^2}{4\,g_{out}C_L} \tag{1.9}$$

and clean up a bit

$$P_{tot}=\frac{kT\gamma}{C_L}\cdot\frac{g_{mp}}{g_{out}}+\frac{kT\gamma}{C_L}\cdot\frac{g_{mn1}}{g_{out}}+\frac{kT\gamma}{C_L}\cdot\frac{g_{mn1}^2/g_{mn0}}{g_{out}} \tag{1.10}$$

Then break out some gain stuff ...

$$P_{tot}=\frac{kT\gamma}{C_L}\cdot\frac{g_{mp}}{g_{out}}\cdot\left(1+\frac{g_{mn1}}{g_{mp}}+\frac{g_{mn1}^2/g_{mn0}}{g_{mp}}\right) \tag{1.11}$$

Then we know that $g_{mn1}=g_{mn0}\cdot K$, so we get:

$$P_{tot}=\frac{kT\gamma}{C_L}\cdot\frac{g_{mp}}{g_{out}}\cdot\left(1+\frac{g_{mn1}}{g_{mp}}+\frac{K\cdot g_{mn1}}{g_{mp}}\right)=\frac{kT\gamma}{C_L}\cdot\frac{g_{mp}}{g_{out}}\cdot\left(1+(1+K)\cdot\frac{g_{mn1}}{g_{mp}}\right) \tag{1.12}$$

The input-referred noise spectral density can be found by dividing the output spectral density with the transfer function (absolute-squared) from input to output. We get:

$$v_{tot}^2(f)=\frac{v_{np}^2(f)\cdot\left|\frac{g_{mp}/g_{out}}{1+\frac{s}{g_{out}/C_L}}\right|^2+v_{nn1}^2(f)\cdot\left|\frac{g_{mn1}/g_{out}}{1+\frac{s}{g_{out}/C_L}}\right|^2+v_{nn0}^2(f)\cdot\left|\frac{g_{mn1}/g_{out}}{1+\frac{s}{g_{out}/C_L}}\right|^2}{\left|\frac{g_{mp}/g_{out}}{1+\frac{s}{g_{out}/C_L}}\right|^2} \tag{1.13}$$

This gives

$$v_{tot}^2(f)=v_{np}^2(f)+v_{nn1}^2(f)\cdot\left|g_{mn1}/g_{mp}\right|^2+v_{nn0}^2(f)\cdot\left|g_{mn1}/g_{mp}\right|^2 \tag{1.14}$$

and with the values inserted

$$v_{tot}^2(f)=4kT\gamma/g_{mp}+4kT\gamma/g_{mn1}\cdot\left|g_{mn1}/g_{mp}\right|^2+4kT\gamma/g_{mn0}\cdot\left|g_{mn1}/g_{mp}\right|^2 \tag{1.15}$$

This equals

$$v_{tot}^2(f)=\frac{4kT\gamma}{g_{mp}}\cdot\left(1+\frac{g_{mn1}}{g_{mp}}+\frac{g_{mn1}^2}{g_{mn0}\cdot g_{mp}}\right)=\frac{4kT\gamma}{g_{mp}}\cdot\left(1+(K+1)\cdot\frac{g_{mn1}}{g_{mp}}\right) \tag{1.16}$$

So that was the simple part ... Let's look at the other two:

> ✗ *The exercise emphasizes on minimizing the number of parameters. This can be done on the expressions above, according to e.g.* $g_{out}\sim\lambda\cdot I_D$ *, etc., etc. That is however not spelled out in the solutions above as we will touch upon this below too.*

3) Express and sketch **how the total output noise power depends on the bias current,** I_0 ! Should the current be **minimized or maximized** for minimum noise?

The total noise is

$$P_{tot}=\frac{kT\gamma}{C_L}\cdot\frac{g_{mp}}{g_{out}}\cdot\left(1+(1+K)\cdot\frac{g_{mn1}}{g_{mp}}\right) \tag{1.17}$$

We have to do some kind of educated guess here. Let's **keep the** V_{effp} **constant** on the input transistor such that gain is maintained (and swing). This means

$$P_{tot}=\frac{kT\gamma}{C_L}\cdot\frac{1}{\lambda\cdot V_{effp}}\cdot\left(1+(1+K)\cdot\frac{g_{mn1}\cdot V_{effp}}{2K\cdot I_0}\right) \tag{1.18}$$

What about g_{mn1} then? Well, same thing here - we probably want to maintain gain and swing when changing our I_0 . This gives us:

$$P_{tot}=\frac{kT\gamma}{C_L}\cdot\frac{1}{\lambda\cdot V_{effp}}\cdot\left(1+(1+K)\cdot\frac{2KI_0\cdot V_{effp}}{2K\cdot I_0\cdot V_{effn}}\right)=\frac{kT\gamma}{C_L}\cdot\frac{1}{\lambda\cdot V_{effp}}\cdot\left(1+(1+K)\cdot\frac{V_{effp}}{V_{effn}}\right) \tag{1.19}$$

which means that I_0 **does not have any influence**.

Another option is to say that V_{effx} is a parameter that can be changed. We can use the expression above again. Since $I_0\sim\alpha\cdot V_{effx}^2$ we see that inside the paranthesis it does not make any difference. But outside the paranthesis it does ... We see that V_{effp} increases if we increase the current. This would thus reduce the P_{tot} . We should therefore **increase the current to minimize noise** (i.e., we should have **lower gain** as we have said several times in the lectures).

4) How should you **set the mirror ratio** for maintained gain but lower noise?

Well, this is more or less the same question as the one above, but with a slight twist (maintained gain). The gain cannot be touched and thus V_{effp} should be held constant and we can then rewrite the terms a bit to extract what terms are playing any role.

$$P_{tot}=\frac{kT\gamma}{C_L}\cdot\frac{g_{mp}}{g_{out}}\cdot\left(1+(1+K)\cdot\frac{g_{mn1}}{g_{mp}}\right)=\frac{kT\gamma}{C_L}\cdot\left(A_0+(1+K)\cdot\frac{g_{mn1}}{g_{out}}\right) \tag{1.20}$$

So the term we have to focus on is

$$\frac{kT\gamma}{C_L}\cdot(1+K)\cdot\frac{g_{mn1}}{g_{out}} \text{ and in essence } (1+K)\cdot\frac{g_{mn1}}{g_{out}} \tag{1.21}$$

Also here, we see the ”gain”from the NMOS hidden in the expression and we can write this as:

$$(1+K)\cdot\frac{1}{\lambda\cdot V_{effn}} \tag{1.22}$$

Notice that the V_{effn} does not depend on the mirror ratio. It is set by the primary side of the mirror. **The mirror ratio should be minimized.**

2. OP/OTA, STABILITY (5 P)

OK, so a question on stability in amplifiers, etc. Consider the configuration in Figure 2.1, which consists of a current mirror and two other transistors. One can see that this is a simplified version of a current-mirror OTA. You can safely assume that all transistors operate in their saturation regions. Obviously it is a kind of two-stage amplifier (?) and you would have a parasitic capacitance, C_p, as indicated in the figure.

Assume the following: (1) $C_{gs} \approx C_{ox} W L/2$ is the dominating capacitor of a single NMOS transistor and for simplicity (2) $g_{mp} = 4 \cdot g_{mn}$.

Express the total DC gain as a function of the mirror ratio, K.

For which values of C_L does the circuit have a 45-degree phase margin (and more)? Sketch and express how this relates to the mirror ratio, K.

Make valid assumptions and motivate them well!

- *Minimize the number of parameters in your expressions.*

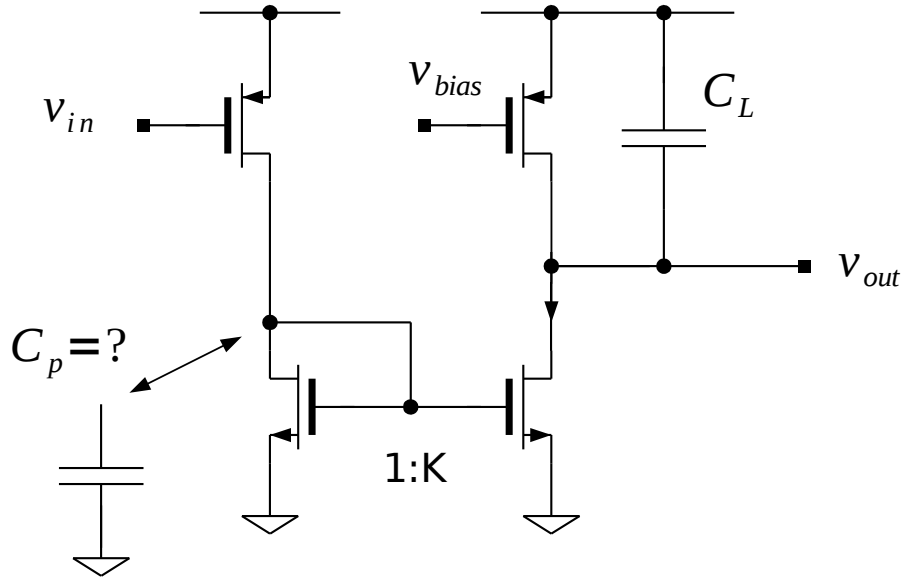

Figure 2.1: Transistors in a gain configuration.

- *Once again! Any (reasonable) try to answer the question can give you credits!*
- *And once again! Do not forget to present your results properly!*
- $\tan^{-1}(\text{large number}) \approx 90$ *degrees,* $\tan^{-1}(1) = 45$ *degrees.*

Solutions

The DC gain transfer function is:

$$\frac{v_2}{v_1}\approx\left(\frac{g_{mp}}{g_{mn}}\right)\cdot\left(\frac{K\cdot g_{mn}}{g_{out}}\right)=K\cdot\left(\frac{g_{mp}}{g_{out}}\right)=K\cdot\frac{I_0/V_{effp}}{\lambda\cdot K I_0}=\frac{1}{\lambda V_{effp}} \tag{2.1}$$

For future calculations, we have to assume that V_{effp} is small such that A_0 is high.

It is independent on the K. Let us include some capacitors:

$$A(s)\approx\frac{g_{mp}/g_{mn}}{1+\frac{s}{g_{mn}/C_p}}\cdot\frac{K\cdot g_{mn}/g_{out}}{1+\frac{s}{g_{out}/C_L}}=\frac{K g_{mp}/g_{out}}{\left(1+\frac{s}{\underbrace{g_{mn}/C_p}_{p_p}}\right)\cdot\left(1+\frac{s}{\underbrace{g_{out}/C_L}_{p_L}}\right)} \tag{2.2}$$

As the tips and tricks claims: assume the poles are well separated which would give us two cases: $p_p\gg p_L$ and $p_L\gg p_p$. We also know that for a general two-pole system we have

$$\phi_m\approx 180-\operatorname{atan}\frac{p_1}{\omega_{ug}}-\operatorname{atan}\frac{p_2}{\omega_{ug}} \tag{2.3}$$

If the poles are well separated this boils down to, since the dominant pole is much lower than unity gain frequency):

$$\phi_m\approx 90-\operatorname{atan}\frac{p_x}{\omega_{ug}}$$ (p_x is the nondominant pole) (2.4)

and further on, if we are targeting 45 degrees, we see that

$$\phi_m\approx 90-\operatorname{atan}\frac{p_x}{\omega_{ug}}=45\Rightarrow\operatorname{atan}\frac{p_x}{\omega_{ug}}=45\Rightarrow\frac{p_x}{\omega_{ug}}=1\Rightarrow p_x=\omega_{ug} \tag{2.5}$$

Further on, the unity-gain frequency is

$$\omega_{ug}\approx A_0\cdot p_y$$ (p_y is the dominant pole). (2.6)

This means that

$$p_x=A_0\cdot p_y=K\cdot\left(\frac{g_{mp}}{g_{out}}\right)\cdot p_y \tag{2.7}$$

First case, $p_p\gg p_L$, i.e., $p_y=p_L$ and $p_x=p_p$.

$$\frac{g_{mn}}{C_p}=K\cdot\left(\frac{g_{mp}}{g_{out}}\right)\cdot\left(\frac{g_{out}}{C_L}\right)\Rightarrow\frac{g_{mn}}{C_p}=\frac{K\cdot g_{mp}}{C_L}\Rightarrow\frac{C_L}{C_p}=\frac{K\cdot g_{mp}}{g_{mn}}=4K \tag{2.8}$$

Then some magic touch on the C_p:

$$C_p = (1+K)\cdot C_{gs} \tag{2.9}$$

which gives us

$$C_L = \frac{K\cdot g_{mp}}{g_{mn}}\cdot C_p = 4K\cdot(1+K)C_{gs} \tag{2.10}$$

And in the strictest sense we should write:

$$C_L > 4K\cdot(1+K)C_{gs} \approx 4K^2\cdot C_{gs} \tag{2.11}$$

Second case, $p_L \gg p_p$, i.e., $p_y = p_p$ and $p_x = p_L$.

$$\frac{g_{out}}{C_L} = K\cdot\frac{g_{mp}}{g_{out}}\cdot\frac{g_{mn}}{C_p} \Rightarrow \frac{C_L}{C_p} = \frac{K}{4}\cdot\frac{g_{mp}^2}{g_{out}^2} \tag{2.12}$$

which gives us

$$C_L = \frac{K}{4}\cdot\frac{g_{mp}^2}{g_{out}^2}\cdot(1+K)C_{gs} \tag{2.13}$$

What to do with the last one? Well, remember that the DC gain was constant from the first question? The DC gain was actually independent on the K mirror ratio and equal to:

$$A_0 = K\cdot\left(\frac{g_{mp}}{g_{out}}\right) \tag{2.14}$$

we can therefore use this as a constant and rewrite as

$$C_L = \frac{K^2}{4}\cdot\frac{g_{mp}^2}{g_{out}^2}\cdot\frac{(1+K)C_{gs}}{K} = A_0^2\cdot\frac{1+K}{K}\cdot C_{gs} = A_0^2\cdot C_{gs}\cdot\left(1+\frac{1}{K}\right) \tag{2.15}$$

or in a stricter sense:

$$C_L < A_0^2\cdot C_{gs}\cdot\left(1+\frac{1}{K}\right) \tag{2.16}$$

Notice the ranges on C_L!

3. SWITCHED CAPACITOR CIRCUITS, ETC. (5 P)

Consider the circuit in Figure 3.1. It has an ideal operational amplifier, two capacitors and some four switches that operate in nonoverlapping phases, ϕ_1 and ϕ_2.

1) Find the transfer function of this circuit by doing a proper charge redistribution analysis.

2) Given your results explain what kind of transfer function it describes is! This is a special circuit and therefore state the important parameters that are so typically associated with this one.

3) Is it parasitic insensitive? **Motivate well and show steps!**

4) Help yourself (and me...) by sketching the output voltage in the time domain (provide some example input signal).

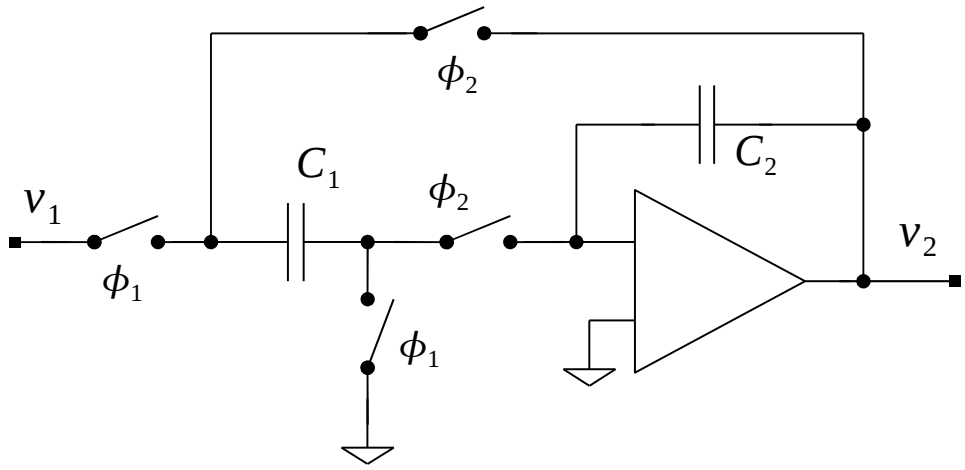

Figure 3.1: Some kind of SC-stuff

✗ *Do not forget to present your calculations properly!*

Solutions

Charge redistribution

1) Find the transfer function of this circuit by doing a proper charge redistribution analysis.

At ϕ_1 :

$$q_1(\phi_1)=C_1\cdot(v_1(\phi_1)-0)=C_1\cdot v_1(\phi_1) \text{ and}$$
$$q_2(\phi_1)=C_2\cdot(v_2(\phi_1)-0)=C_2\cdot v_2(\phi_1) \quad (3.1)$$

At ϕ_2 :

$$q_1(\phi_2)=C_1\cdot(v_2(\phi_2)-0)=C_1\cdot v_2(\phi_2) \text{ and}$$
$$q_2(\phi_2)=C_2\cdot(v_2(\phi_2)-0)=C_2\cdot v_2(\phi_2) \quad (3.2)$$

Charge preservation (we have two formulas):

$$q_2(\phi_1)=q_2(\phi_2)\Rightarrow v_2(\phi_1)=v_2(\phi_2) \quad (3.3)$$

and

$$q_1(\phi_2)+q_2(\phi_2)=q_1(\phi_1)+q_2(\phi_2) \quad (3.4)$$

Let's start to use some "hormal"indexes and replace with the capacitor-times-voltage expressions:

$$\begin{aligned} C_1\cdot v_2(n+0.5)+C_2\cdot v_2(n+0.5)&=C_1\cdot v_1(n)+C_2\cdot v_2(n)\Rightarrow \\ (C_1+C_2)\cdot v_2(n+0.5)-C_2\cdot v_2(n)&=C_1\cdot v_1(n) \end{aligned} \quad (3.5)$$

And we know that

$$v_2(n)=v_2(n-0.5) \quad (3.6)$$

so we get

$$(C_1+C_2)\cdot v_2(n+0.5)-C_2\cdot v_2(n-0.5)=C_1\cdot v_1(n) \quad (3.7)$$

Which kind of enables us to go for the z-transform:

$$(C_1+C_2)\cdot V_2(z)\cdot z^{0.5}-C_2\cdot V_2(z)\cdot z^{-0.5}=C_1\cdot V_1(z) \text{ or}$$
$$(C_1+C_2)\cdot V_2(z)-C_2\cdot V_2(z)\cdot z^{-1}=C_1\cdot V_1(z)\cdot z^{-0.5} \quad (3.8)$$

We can now form the transfer function:

$$H(z)=\frac{V_2(z)}{V_1(z)}=\frac{C_1\cdot z^{-0.5}}{(C_1+C_2)-C_2\cdot z^{-1}}=\frac{C_1}{C_1+C_2}\cdot\frac{z^{0.5}}{z-\frac{C_2}{C_1+C_2}} \tag{3.9}$$

2) Given your results explain what kind of transfer function it describes is! This is a special circuit and therefore state the important parameters that are so typically associated with this one.

A good old low-pass filter it is... and bandwidth is given by ... what? Well, make life easy for you and do that replacement we did in one of the lectures:

$$z=e^{j\omega T}\approx 1+j\,\omega T=1+sT \tag{3.10}$$

The denominator becomes

$$1+sT-\frac{C_2}{C_1+C_2}=sT-\frac{C_1}{C_1+C_2} \tag{3.11}$$

This would imply a pole at (cf. $1+s/p_1$)

$$p_1=\frac{C_1}{T\cdot(C_1+C_2)} \text{ or } f_{3\text{dB}}=f_{sample}\cdot\frac{C_1}{2\pi\cdot(C_1+C_2)} \tag{3.12}$$

The DC gain of the circuit is found for $z=1$ (!!!) and is equal to

$$H(1)=\frac{C_1}{C_1+C_2}\cdot\frac{1}{1-\frac{C_2}{C_1+C_2}}=1 \tag{3.13}$$

3) Is it parasitic insensitive? **Motivate well and show steps!**

It is parasitic insensitive.

The C_2 is definitely not affected, it is fixed and one plate is virtually grounded, the other is connected to OTA output. The C_1 has one of its plates connected to either ground or virtual ground, so that is safe. The other side is either connected to ideal input voltage or to ideal OTA output, thus these ideal sources will restore the charge accordingly.

4) Help yourself (and me...) by sketching the output voltage in the time domain (provide some example input signal).

As long as you captured the fact that output is half a clock delayed and that the output is sampled and held during the whole period.

4. DATA CONVERTERS (ADCS)

The noise analysis in question one was so simple this time ... let us extend to cover also data converters.

You want to design an uniformly sampling and uniformly quantizating N-bit flash ADC. The conversion range is 1 V. The reference levels for the comparators are given by a resistor string containing a total resistance of

$$R_{tot}=2^N\cdot\Delta R \tag{4.1}$$

where ΔR is a unit resistance. Assume that all resistors in the resistive divider are noisy. The thermal noise voltage spectral density for any resistance, R, is given by

$$v_{nR}^2(f)=4kTR \tag{4.2}$$

and can be assumed to be white, i.e., a Gaussian distribution.

Assume that, magically, the bandwidth of the resistive divider equals the sample frequency of the converter, f_s, for all reference nodes.

1) What is the (theoretical) **quantization noise power** of the converter provided the sample frequency is f_s, the input signal bandwidth is $f_{BW}=4\cdot f_s$, and the decimation filters receiving the ADC output have an ideal bandwidth of $f_s/2$.

2) In the text above we have put two requirements on the ADC to be able to do the type of calculations we do in 1). What is missing?

3) How large can ΔR be **without having any impact on performance** (assume a 6-sigma limit on the thermal noise)? Express this in terms of number of bits, N, and sample frequency, f_s.

- *Notice that you need to work with some probability theory - the noise has a Gaussian distribution, hence the comment on 6 sigma above.*
- *Are you really comparing right things with eachother? Apples and pears - as we say in Swedish.*

Solutions

1) What is the (theoretical) **quantization noise power** of the converter provided the sample frequency is f_s, the input signal bandwidth is $f_{BW}=4\cdot f_s$, and the decimation filters receiving the ADC output have an ideal bandwidth of $f_s/2$.

Most of the jibberish above plays no role for the quantization noise - the quote on decimation filters does. But frequency is set to f_s/2, i.e., whole band is passed through. The quantization noise is therefore the good old:

$$P_q=\frac{\Delta^2}{12}\approx\frac{1}{12}\cdot\left(\frac{1}{2^N}\right)^2=\frac{1/3}{2^{2N+2}} \tag{4.3}$$

2) In the text above we have put two requirements on the ADC to be able to do the type of calculations we do in 1). What is missing?

The signal needs to be uncorrelated with the signal and this is done when N is high enough and the signal is large enough.

3) How large can ΔR be **without having any impact on performance** (assume a 6-sigma limit on the thermal noise)? Express this in terms of number of bits, N, and sample frequency, f_s.

We have 2^N resistors in our resistor chain generating a total noise current of

$$v_{rn}^2(f)=4kTR_{tot} \tag{4.4}$$

From an AC point of view, the worst case noise is found on the center tap of the resistor ladder. From an AC point of view, we have to fold the transistor ladder (Vrefpos and Vrefneg connected to ground). Then the noise is the overlaying AC source.

From point k on the ladder, the transfer function will be:

$$V_k=V_n\cdot\frac{k\cdot\Delta R\times(2^N-k)\cdot\Delta R}{k\cdot\Delta R+(2^N-k)\cdot\Delta R}\cdot\frac{1}{R_{tot}}=V_n\cdot\frac{k\cdot(2^N-k)\cdot\Delta R}{2^N}\cdot\frac{1}{2^N\cdot\Delta R}=V_n\cdot\frac{k\cdot(2^N-k)}{2^{2N}} \tag{4.5}$$

This expression will take its maximum value at $k=2^{N-1}$ and we get

$$V_{2^{N/2}}=V_n\cdot\frac{2^{N-1}\cdot(2^N-2^{N-1})}{2^{2N}}=V_n\cdot\frac{2^{N-1}\cdot(2^{2N-1}-2^N)}{2^{2N}}=V_n\cdot\left(\frac{1}{2}-\frac{1}{2^N}\right)\approx\frac{V_n}{2} \tag{4.6}$$

So, from a noise perspective, we need to use the superfunction:

$$v_{max}^2(f)=\frac{v_{rn}^2(f)}{4} \tag{4.7}$$

The total noise voltage found on the ladder was given previously and it gives us:

$$v_{max}^2(f)=\frac{4\,k\,T\,R_{tot}}{4}=k\,T\,R_{tot} \tag{4.8}$$

The total noise power is given by the bandwidth and we get:

$$P_{tot}=v_{max}^2(f)\cdot\frac{p_1}{4}=v_{max}^2(f)\cdot\frac{2\pi f_1}{4}=v_{max}^2(f)\cdot\frac{\pi f_s}{2}=kT\,R_{tot}\cdot\frac{\pi f_s}{2} \tag{4.9}$$

Which we can write as

$$P_{tot}=k\,T\,\Delta R\cdot\pi f_s\cdot 2^{N-1} \tag{4.10}$$

The rms value of the noise voltage becomes

$$v_{nrms}=\sqrt{k\,T\,\Delta R\cdot\pi f_s\cdot 2^{N-1}} \tag{4.11}$$

This must be compared to the LSB voltage and we need to consider the 6-sigma specification. To avoid a bit error in the center tap, we must guarantee that the noise does not become higher than half and LSB, since otherwise the comparator of the next level would detect the level and give you a bit error. This statement gives us:

$$v_{nrms}\cdot 6<\frac{v_{LSB}}{2}\Rightarrow\sqrt{k\,T\,\Delta R\cdot\pi f_s\cdot 2^{N-1}}<\frac{1}{12\cdot 2^N}\Rightarrow k\,T\,\Delta R\cdot\pi f_s\cdot 2^{N-1}<\frac{1}{144\cdot 2^{2N}} \tag{4.12}$$

We can now solve this for ΔR:

$$\Delta R<\frac{1}{72\pi\cdot 2^{3N}\cdot k\,T\cdot f_s} \tag{4.13}$$

For the fun of it - let's pick some numbers: $N=12$, $f_s=100$ MHz. This would give us a resistance of 0.15 Ohm(!). This means that you must limit the bandwidth of the ladder significantly to avoid small resistors.

On the other hand - a 12-bit flash converter wouldn't really be realistic anyway. But this exercise indicates how the resistor scales.

5. FILTERS, OPAMPS, ETC.

Implement the following transfer function

$$H(s)=\frac{V_2(s)}{V_1(s)}=\frac{K\cdot\omega_0^2}{s^2+\frac{\omega_0}{Q}s+\omega_0^2} \tag{5.1}$$

using the leapfrog approach (see Figure 5.1 for an outline and suggested starting point for your work). All the three parameters K, ω_0, and Q, are positive numbers. We can set the DC gain of the filter to unity and the cut-off frequency to be 10 MHz. We can set the quality factor to $1/\sqrt{2}$.

1) Realize the filter using active RC components! Use a minimum number of single-ended operational amplifiers. Use Figure 5.1 as a guidance.

2) Suggest different R and C values, i.e., find the R and C that give you the K, ω_0, and Q values.

3) Assume the filter is implemented using OTAs rather than OPs. How should you in that case select the values on R and C?

4) In general - in a modern, 45-nm CMOS process and a filter of this type, how large would you set the components?

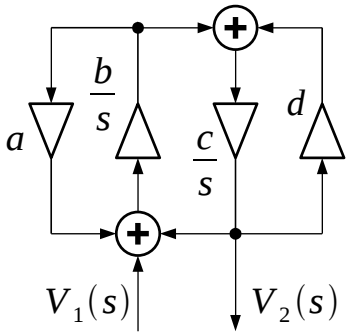

Figure 5.1: Second-order leapfrog approach...

- *Hint! We have been looking at odd-order structures (mainly third-order) in our leapfrog filters. Strip the existing Leapfrog diagram and see what happens if you only save two integrators.*
- *Do not forget the option to invert nodes if needed ...*
- *Subquestions 2, 3, and 4 are more or less the same question...*

Solutions

So - first of all - this could have been a straight-forward plug-in-the-numbers exercise. But ... Well, let's start by looking at the " **(see Figure 5.1 for an outline and suggested starting point for your work)** "If I were you I should have reacted here and understood that there was something behind this... Anyway, look at the tips:

> x *Hint! We have been looking at odd-order structures (mainly third-order) in our leapfrog filters. Strip the existing Leapfrog diagram and see what happens if you only save two integrators.*

Option 1

Let's look at the figure: Introduce a helping node, $R_0 I_0(s)$ to the graph and start:

$$V_2(s)=\frac{c}{s}\cdot\left(d\cdot V_2(s)+R_0 I_0(s)\right) \text{ and } R_0 I_0(s)=\frac{b}{s}\cdot\left(a\cdot R_0 I_0(s)+V_1(s)+V_2(s)\right) \tag{5.2}$$

We should now solve this w.r.t. V_2 and V_1. The first equation claims:

$$V_2(s)\frac{s}{c}-d\cdot V_2(s)=R_0 I_0(s)\Rightarrow V_2(s)=\frac{R_0 I_0(s)}{\frac{s}{c}-d} \tag{5.3}$$

and the second one gives us:

$$R_0 I_0(s)\cdot\frac{s}{b}-a\cdot R_0 I_0(s)=V_1(s)+V_2(s)\Rightarrow R_0 I_0(s)=\frac{V_1(s)+V_2(s)}{\frac{s}{b}-a} \tag{5.4}$$

Combining these two gives us:

$$V_2(s)=\frac{R_0 I_0(s)}{\frac{s}{c}-d}=\frac{V_1(s)+V_2(s)}{\left(\frac{s}{b}-a\right)\cdot\left(\frac{s}{c}-d\right)}\Rightarrow\frac{V_2(s)}{V_1(s)}=\frac{1}{\left(\frac{s}{b}-a\right)\cdot\left(\frac{s}{c}-d\right)-1} \tag{5.5}$$

Or perhaps

$$\frac{V_2(s)}{V_1(s)}=\frac{bc}{(s-ab)\cdot(s-cd)-bc}=\frac{bc}{s^2-(ab+cd)s+bc\cdot(ad-1)} \tag{5.6}$$

Now, we need to align these parameters with the data given in the exercise.

$$bc=K\cdot\omega_0^2,\ -(ab+cd)=\frac{\omega_0}{Q},\ bc(ad-1)=\omega_0^2 \tag{5.7}$$

The exercise also states $K=1$, which quickly gives us $ad=2$ and $d=2/a$. Further on, we obviously get $c=\omega_0^2/b$.Thus we have

$$\frac{V_2(s)}{V_1(s)}=\frac{\omega_0^2}{s^2-(ab+2\omega_0^2/ab)s+\omega_0^2} \tag{5.8}$$

So,

$$ab+2\frac{\omega_0^2}{ab}=\frac{-\omega_0}{Q}\Rightarrow(ab)^2+\frac{\omega_0}{Q}\cdot(ab)+2\omega_0^2=0 \tag{5.9}$$

gives

$$(ab)^2+\frac{\omega_0}{Q}\cdot(ab)+2\omega_0^2=0 \tag{5.10}$$

Solve this for (ab) to get:

$$(ab)=\frac{-\omega_0}{2Q}\pm\sqrt{\frac{\omega_0^2}{4Q^2}-2\omega_0^2}=-\frac{\omega_0}{2\sqrt{2}}\pm\omega_0\cdot\sqrt{\frac{1}{2}-2}=-\frac{\omega_0}{2\sqrt{2}}\left(1\pm2\cdot\sqrt{-3}\right) \tag{5.11}$$

Oops - getting bad feelings ... brrr. Negative number gives me a complex number, not good... How do we implement a complex number? That has to be done with a resonator. This means we are looking at an LC tank in the schematics. Should we change the schematics or what? Aaarghgh!? Well, look at the hints:

> *x Do not forget the option to invert nodes if needed ...*

So, somewhere you need to plug in those inverters... Happy hunting. I'll omit those steps in the solutions.

A hint is to insert it close to the V_2 node in one of feedback paths... and also think of how the input is fed to the network ... is that really the correct way of doing it? Shouldn't it be scaled somehow?

Option 2

Another options is to start from the real basics instead and partially ignore the picture of the exercise. Look at a second-order LC ladder network. Assume generator and load resistors to be equal, $R_0=R_L$. Set up the equations

$$I_0=\frac{(V_1-V_x)}{R_0},\ V_x=\frac{(I_0-I_2)}{sC},\ I_2=\frac{(V_x-V_2)}{sL},\ I_2=\frac{V_2}{R_0} \tag{5.12}$$

Create the state space variables

$$RI_0=(V_1-V_x)\cdot\frac{R}{R_0},\ V_x=\frac{(RI_0-RI_2)}{sRC},\ RI_2=(V_x-V_2)\cdot\frac{R}{sL},\ RI_2=V_2\cdot\frac{R}{R_0} \tag{5.13}$$

And hook them up according to the leapfrog scheme. Eliminate the inversions, move the adder of the input signal. Eliminate some more inverters. Then notice that we have some additional inversion in one of the outer branches. How to handle that one, hmm, hmm.

In Figure 5.2 below, the purple guys are the integrators. The white ones are the amplifiers, and I haven't added the values (them you can find in the equation above).

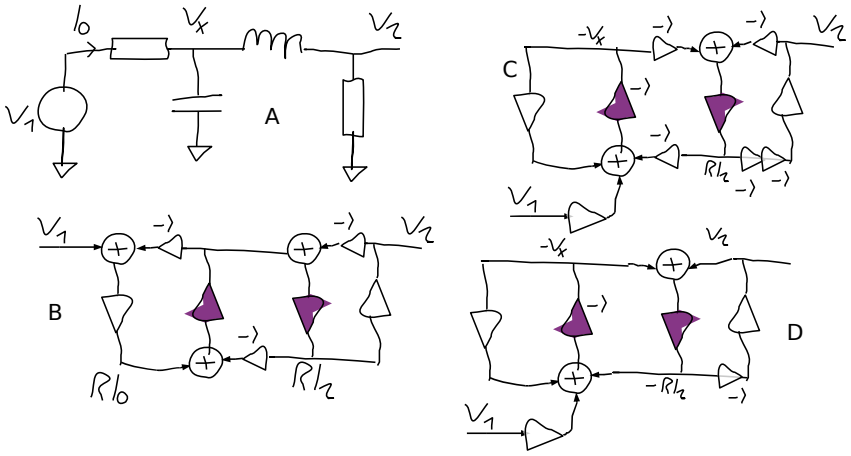

Figure 5.2: Tjoho!

Well, we can introduce two "dummy"inverters for the rightmost integrator (Figure 5.3 A). We can now pick an intermediate node (Figure 5.3 B). Further, we can translate V_2 and picked it from another node (Figure 5.3 C). We can actually remove it too (Figure 5.3 D) as the inverter later on will give us an option to scale the feedback path. Additional scaling can be done at the input to the whole filter!

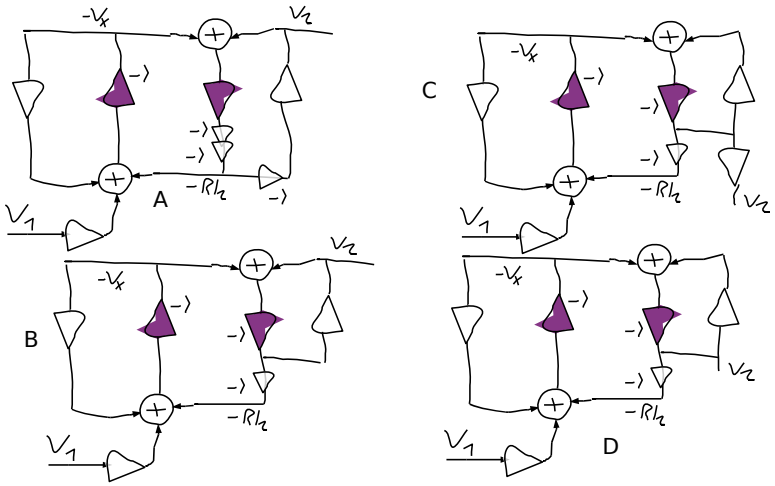

Figure 5.3: Yippie!

Then start to insert the integrators and you would get something like Figure 5.4. Except for my horrible sketch, but belive me, it is quite similar to whatever leapfrog RC integrator implementation that we have used in the course.

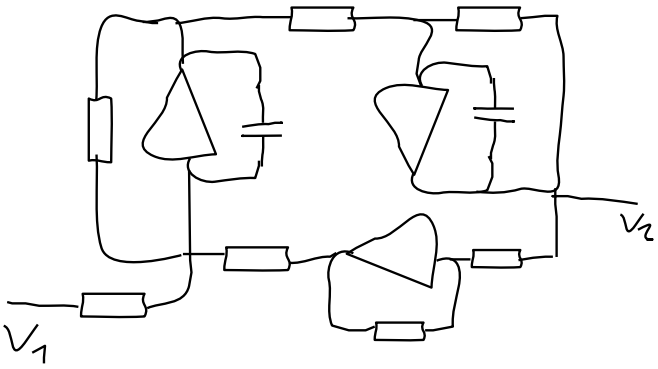

Figure 5.4: RC thing-ie.

Notice that this more ore less directly could be derived from the existing diagrams you find in your hand-outs.

The equations here would be (starting with the left-most integrator):

$$V_x = -\left(\frac{1}{s R_1 C_1}\cdot V_1 + \frac{1}{s R_2 C_1}\cdot V_x - \frac{R_4/R_5}{s R_3 C_1}\cdot V_2\right)$$ which turns into

$$-V_x\left(1+\frac{1}{s R_2 C_1}\right) = \frac{1}{s R_1 C_1}\cdot V_1 - \frac{R_4/R_5}{s R_3 C_1}\cdot V_2$$ which we can rewrite (5.14)

$$-V_x\cdot\frac{s R_2 C_1+1}{s R_2 C_1} = \frac{V_1}{s R_1 C_1} - \frac{R_4/R_5}{s R_3 C_1}\cdot V_2 \Rightarrow -V_x\cdot\left(s R_2 C_1+1\right) = \frac{R_2}{R_1}\cdot V_1 - \frac{R_2\cdot R_4}{R_3\cdot R_5}\cdot V_2$$

Here it would make sense to introduce some help variables, for example $\tau_1 = R_2 C_1$. For the other integrator, we get:

$$V_2 = -\left(\frac{1}{s R_6 C_2}\cdot V_x + \frac{1}{s R_7 C_2}\cdot V_2\right) \Rightarrow V_x = -V_2\cdot\frac{1+\frac{1}{s R_7 C_2}}{\frac{1}{s R_6 C_2}} = -V_2\cdot\left(s R_7 C_2+1\right)\cdot\frac{R_6}{R_7} \quad (5.15)$$

Now they can be combined:

$$V_2\cdot\left(\left(s R_7 C_2+1\right)\cdot\frac{R_6}{R_7}\cdot\left(s R_2 C_1+1\right) + \frac{R_2\cdot R_4}{R_3\cdot R_5}\right) = \frac{R_2}{R_1}\cdot V_1 \quad (5.16)$$

or

$$\frac{V_2}{V_1}=\frac{R_2/R_1}{\left(sR_7C_2+1\right)\cdot\frac{R_6}{R_7}\cdot\left(sR_2C_1+1\right)+\frac{R_2\cdot R_4}{R_3\cdot R_5}} \tag{5.17}$$

which is equal to

$$\frac{V_2}{V_1}=\frac{R_2/R_1}{s^2R_6R_2C_1C_2+\frac{R_6}{R_7}+s\left(R_6C_2+R_2C_1\frac{R_6}{R_7}\right)+\frac{R_2\cdot R_4}{R_3\cdot R_5}} \tag{5.18}$$

and eventually

$$\frac{V_2}{V_1}=\frac{\frac{R_2}{R_1}\cdot\frac{1}{R_6R_2C_1C_2}}{s^2+s\cdot\frac{R_6C_2+R_2C_1\frac{R_6}{R_7}}{R_6R_2C_1C_2}+\frac{\frac{R_2\cdot R_4}{R_3\cdot R_5}+\frac{R_6}{R_7}}{R_6R_2C_1C_2}} \tag{5.19}$$

2) Go for the engineer style. ("A lazy engineer is a good engineer"). Set all resistors equal: $R_0=R_1=R_2=R_3=R_4=R_5=R_6=R_7$ then also identify two time constants: $\tau_1=R_2C_1$ and $\tau_2=R_6C_2$. Put them equal too for simplicity, $\tau=\tau_1=\tau_2$ (i.e. capacitors equally large too). What do we get?

$$\frac{V_2}{V_1}=\frac{1/\tau^2}{s^2+s\cdot\frac{2\tau}{\tau^2}+\frac{2}{\tau^2}}=\frac{1/\tau^2}{s^2+s\cdot\frac{2}{\tau}+\frac{2}{\tau^2}} \tag{5.20}$$

Nice... To find the DC gain, set $s=0$. This gives us

$$\frac{V_2}{V_1}=\frac{1}{2} \tag{5.21}$$

which violates the requirement of $K=1$. So, for this purpose, we need to set $R_1=0.5R_2$. Let's check the others and go from the original formula: $\omega_0=\sqrt{2}/\tau$ is clear from the third term in the denominator. And magically, we see that the second term also neatly boils down to ω_0/Q (!)

> *x This is actually not that magical, since you set the two τ equal...*

From the exercise we have $\omega_0=2\pi\cdot 10$ MHz. Say now, we have a 1-pF capacitor, that would give us a resistance of approximately 160 kOhms. So,

$C_1=C_2=1$ pF, and $R_2=R_3=R_4=R_5=R_6=R_7=2R_1=167$ kOhm.

3+4). Set as many components as equal as possible, don't make them larger than say 10 pF, try to avoid large resistor, 160 kOhm is too much, hence use larger capacitors. With 10 pF we get 16 kOhm.

> ✗ *It should be mentioned that scaling would potentially require us to select different values.*