TSTE08, Analog and Discrete-time Integrated Circuits, 2010-08-28
Written exam, TENA

Date and time	2010-08-28, 14.00 - 18.00
Location(s)	TER2 (20 copies printed)
Responsible teacher	J Jacob Wikner, jacwi50, +46-70-5915938
Aid	**Any written and printed material, including books and old exams.** **Note! No pocket calculators, no laptops, no ipods, no telephones, no internet connection.**
Instructions	A maximum of 25 points can be obtained, 10 points are required to pass, 15 for a grade four, and 20 for a grade five. ɤ *Hint!* ***Be strategic*** *when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...* Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully! ɤ *Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available by 2010-09-11 (hopefully...)

Outline

1. CMOS, PERFORMANCE, ETC. (5 P)

Consider the circuit in Figure 1.1 below. An input signal is fed to the gate of the NMOS transistor. The DC output voltage, v_{out} - at the drain of the transistor - is fixed by a very, very, very, very large resistor, R_{set}. There is a capacitive load, C_L, between transistor drain and positive supply. The transistor should operate in its saturation region. Further on, the input voltage is biased at

$$V_{IN}=V_{dd}/4 . \tag{1.1}$$

Now, assume that this single-stage amplifier has a certain slew rate of SR in its bias operating region. Sketch how the following parameters depend on the slew rate when the **capacitance is fixed**:

1) Transconductance g_m,
2) output conductance g_{ds},
3) DC gain $A_0=g_m/g_{ds}$,
4) dominant pole p_1, and
5) unity-gain frequency ω_u.

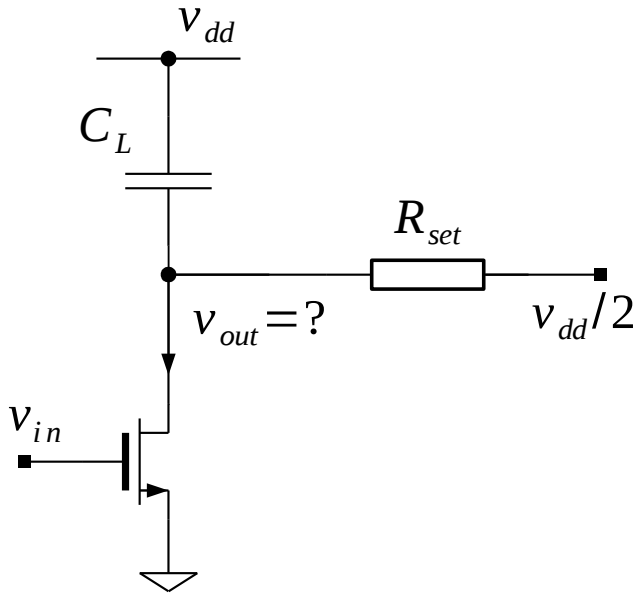

Figure 1.1: Common-something with some kind of load and stuff.

- *This exercise will show that you have understood basic small-signal properties and the relations between them. Make valid assumptions and motivate them well.*
- *Sketch does not mean: draw with infinite accuracy.*

2. GAIN STAGES, SWING, ETC. (5 P)

Consider the circuit in Figure 2.1 which is some kind of circuit. It consists of one PMOS and four NMOS transistors. The input signal is connected to transistor M_0, the output is connected to the drain of M_4 and source of M_3.

1) Find the minimum and maximum **output voltage levels** for which all transistors are operating their saturation region.

2) Derive a compact formula describing the DC gain as function of the two currents through transistors M_2 and M_4.

3) Describe with words (or maths if you like) what happens to the DC gain if input voltage is connected to transistor M_2 rather than M_0?

Make valid assumptions and motivate them well in your solutions!

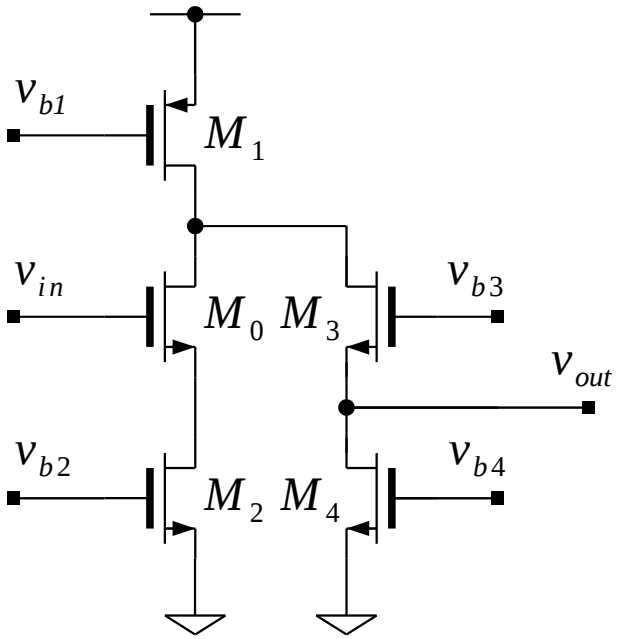

Figure 2.1: Some differential pair of some kind.

- *This exercise will show that you have understood the relation between schematics and small-signal expressions as well as large-signal operation.*
- ***Remember**: You can **always do some suitable assumptions**, as long as you motivate them well!*
- *Don't forget to sanity check your results! Hint: what should the DC gain be for this kind of circuit?*

3. NOISE (5 P)

Consider the circuit in Figure 3.1 which consists of two transistors and some kind of load between them, Z_L:

$$Z_{out} = R_{out} \| C_{out} \tag{3.1}$$

The input voltage, v_{in}, is connected to the two gates and the output voltage, v_{out}, is the voltage across the Z_L. Both transistors operate in their saturation region. Further assume that all transistors (well, the two of them) are noisy. The resistor, R_{out}, can be considered to be noise free.

1) Derive the **total output noise power**

2) Derive the **input-referred noise spectral density**

3) Express and sketch **how the input-referred noise depends on the input DC voltage!**

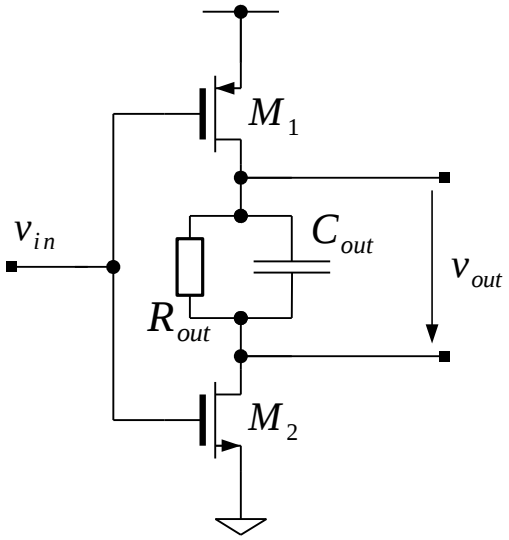

Figure 3.1: Phew! Two transistors...

- *Tip! Use all the symmetries to speed up your conclusions.*
- *Don't forget that you have to consider the **total noise power** at the output. Hint: use the noise brickwall bandwidth: $p_1/4$ (see for exampleJohns Martin).*

4. OP/OTA, FEEDBACK (5 P)

OK, so a question on feedback in amplifiers, etc. Consider the feedback configuration in Figure 4.1. It consists of a CMOS inverter with R_1 and R_2 as feedback components. So a couple of exercises for you:

1) What is the input impedance?

2) For which values on C_{out} is the circuit stable?

3) Assume closed loop gain should be <u>exactly unity</u>. Dimension the R_1 **and** R_2 and **d**o **not** neglect the influence of the limited gain of the transistors.

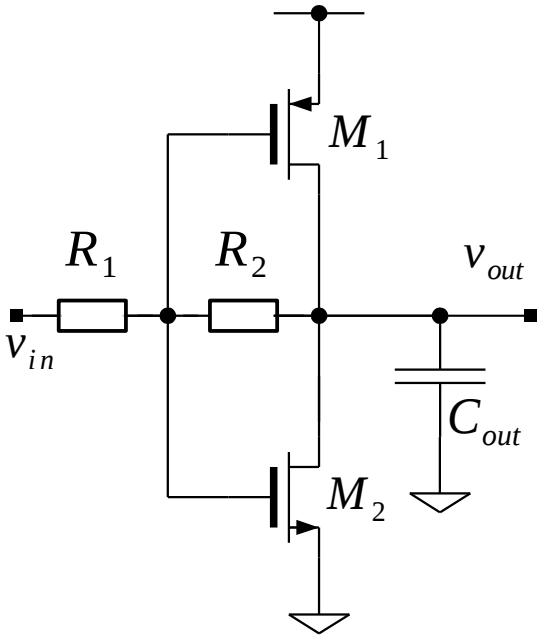

Figure 4.1: Transistors in a closed-loop gain configuration.

- *Once again! Any (reasonable) try to answer the question can give you credits!*
- *And once again! Do not forget to present your results properly!*

5. SWITCHED CAPACITOR CIRCUITS, ETC. (5 P)

ᵡ Well ... Back to basics ...

Consider the circuit in Figure 5.1. It has an amplifier in a buffer configuration, two capacitors and two switches that operate in nonoverlapping phases. Assume the buffer to be ideal.

As a designer, you have quite a few dfifferent design parameters to take into account. Today, let us focus on the switches and the sampling time.

Assume that the switches have an on-resistance of R_{on} and that the off-resistance R_{off} is very, very, very, very, very large. Further on, you have a certain sampling period, i.e., $T=1/f_s$, in your system.

1) What is the **average power consumption** of the circuit as a function of these parameters? Assume the input signal is

$$v_{in}(t)=A\cdot\sin\left(2\pi f_0 t\right), \tag{5.1}$$

where A is an amplitude and f_0 is a frequency significantly lower than the sample frequency.

2) What would the power consumption be **if the switches are ideal**, i.e., $R_{on}=0$?

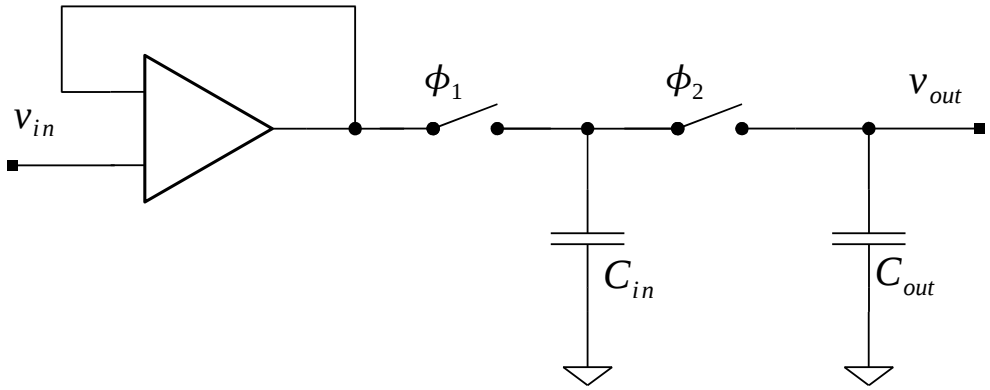

Figure 5.1: Some kind of SC-stuff