Lecture 9, ATIK

Data converters 2

LiU EXPANDING REALITY

What did we do last time?

Data converters

- Fundamentals
- Overview of different types of data converters

A first glance at oversampling

What will we do today?

Recapture the oversamping data converters

- Interpolating/Decimating
- Sigma-delta modulator

DACs

- Designing a current-steering DAC

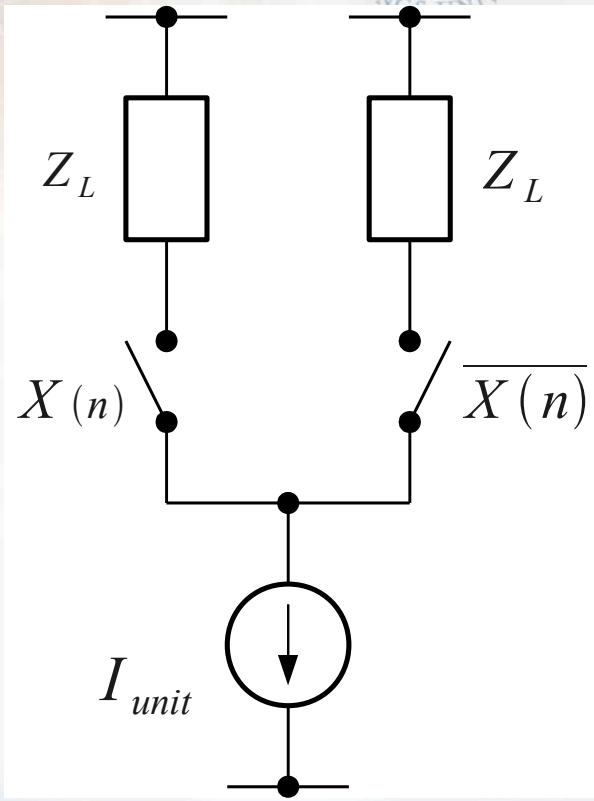
Current-steering DAC

All current directed to the output implies high efficiency

No buffer required, implies high speed

Short design time

Current output and no buffer implies now slow rate limitations



$$I_{out}(X) = X \cdot I_{unit} = \sum x_k \cdot 2^{k-1} \cdot I_{unit}$$

with

$$X = X_0 + \Delta X$$

gives

$$V_{out}(X) = Z_L \cdot I_{out}(X) = X \cdot Z_L \cdot I_{unit} = Z_L \cdot \sum x_k \cdot 2^{k-1} \cdot I_{unit}$$

Current-steering DAC, MOS implementation

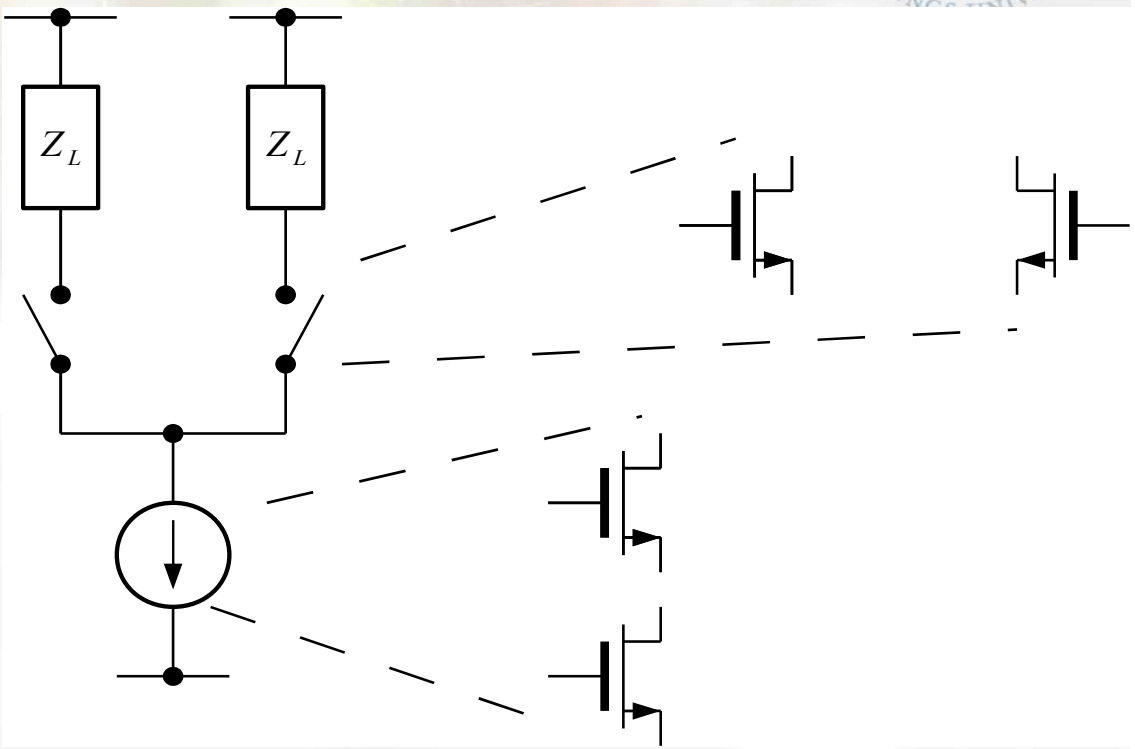
Switches are implemented by NMOS

- Transmission gates normally does not make any impact

Current sources are typically cascoded transistors

- C.f. current mirror

Each weight consists of k unit sources in parallel



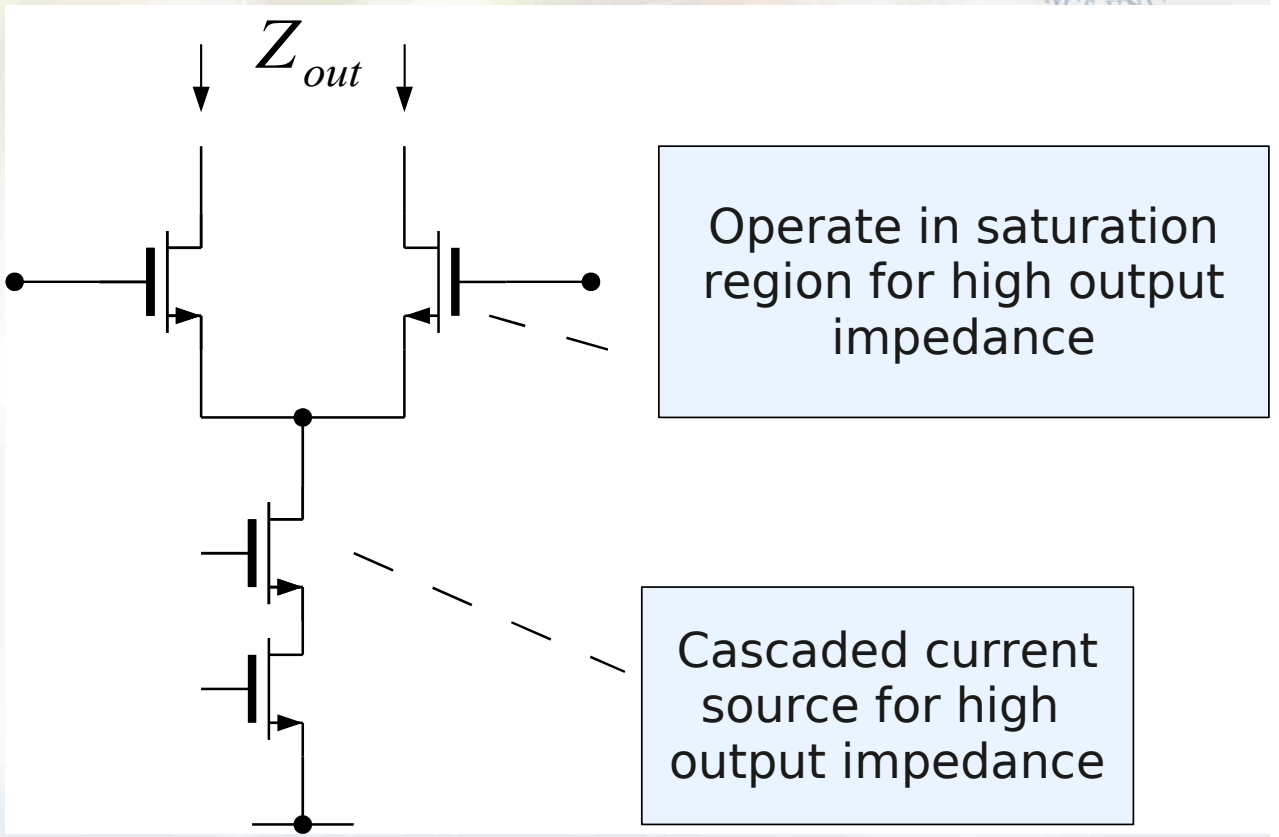
Current-steering DAC, main design tasks

Designing a good differential pair

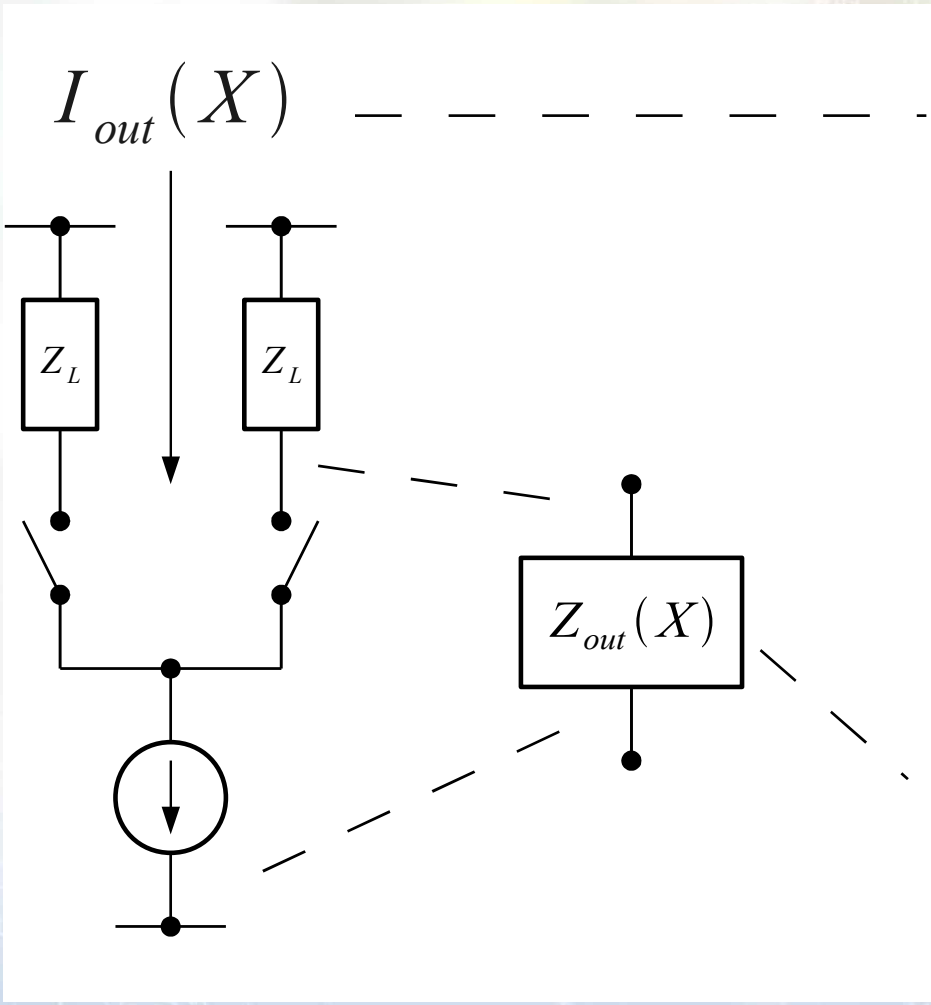
Designing accurate current mirrors

Optimization

Trade-offs



Output impedance



Output currents depend on output impedance (i.e. quality of current source).

Distortion

Output impedance is also dependent on the code.

Output impedance

Form the differential output

$$V_{out}(\Delta X)=\frac{Z_L\cdot I_{unit}\cdot(X_0+\Delta X)}{1+Z_L\cdot Y_{unit}\cdot(X_0+\Delta X)}-\frac{Z_L\cdot I_{unit}\cdot(X_0-\Delta X)}{1+Z_L\cdot Y_{unit}\cdot(X_0-\Delta X)}$$

Scale and introduce helping variables

$$\frac{V_{out}(\Delta X)}{Z_L\cdot I_{unit}\cdot X_0}=\frac{1+\delta x}{1+\eta\cdot(1+\delta x)}-\frac{1-\delta x}{1+\eta\cdot(1-\delta x)}$$

$$\frac{V_{out}(\Delta X)}{Z_L\cdot I_{unit}\cdot X_0}=\frac{2\,\delta x}{(1+\eta\cdot(1+\delta x))\cdot(1+\eta\cdot(1-\delta x))}$$

and approximate

$$\frac{V_{out}(\Delta X)}{Z_L\cdot I_{unit}\cdot X_0}=\frac{2\,\delta x/(1+\eta)^2}{1-\left(\frac{\eta}{1+\eta}\right)^2\cdot\delta x^2}\approx\frac{2\,\delta x}{(1+\eta)^2}\cdot\left(1+\left(\frac{\eta}{1+\eta}\right)^2\cdot\delta x^2\right)$$

Output impedance, linearity requirement

Harmonic distortion is the power ratio between fundamental and distortion term:

$$\mathrm{HD}_3 \sim \frac{1}{8\cdot\left(\frac{\eta}{1+\eta}\right)^4} = \frac{1}{8} + \frac{1}{8\cdot\eta^4} \approx \frac{1}{8\cdot\eta^4} = \frac{1}{8\cdot\left(Z_L\cdot Y_{unit}\cdot X_0\right)^4} = \frac{1}{8}\cdot\left(\frac{Z_{unit}/Z_L}{2^{N-1}}\right)^4$$

For a given output impedance, Z_{unit}:

With more bits, the harmonic distortion gets worse

With a larger load resistance, the distortion gets worse

Example:

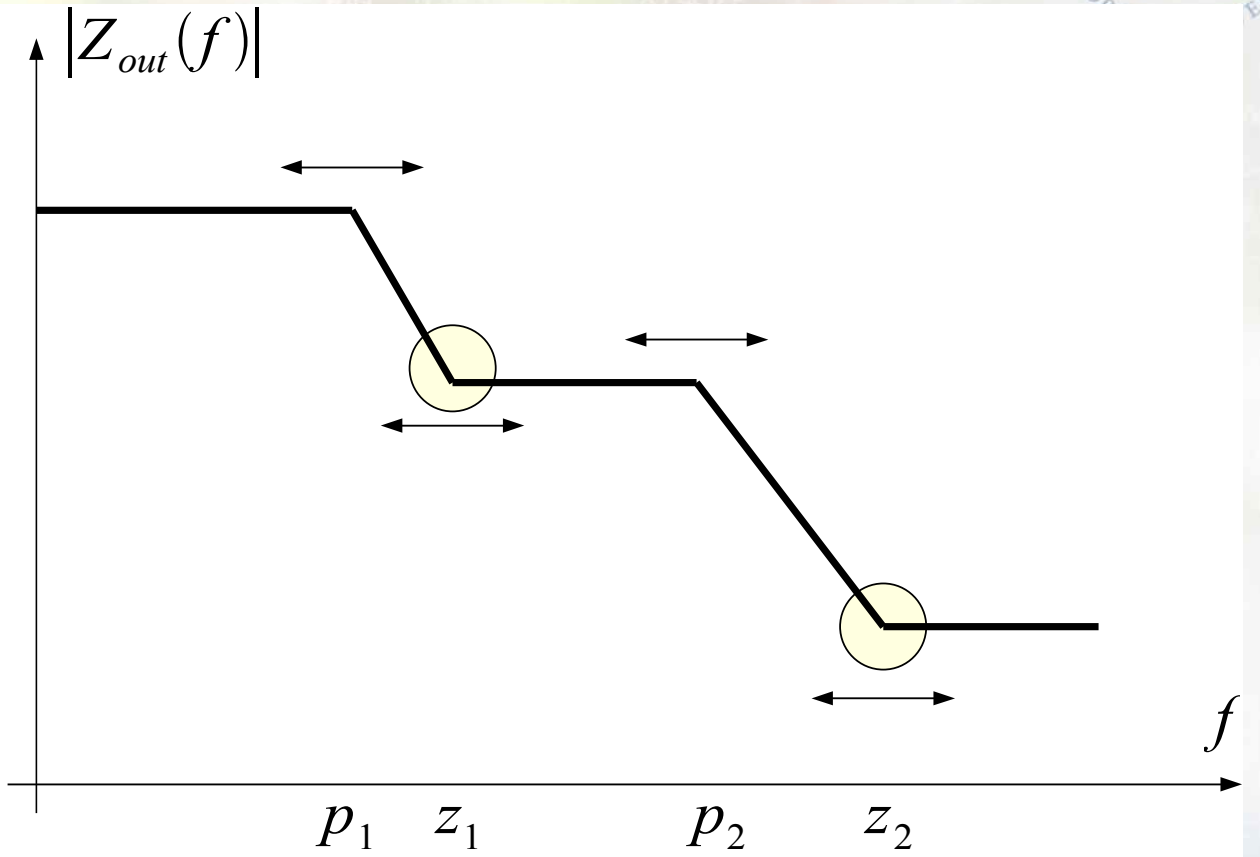
$Z_{unit}=1\,\mathrm{M}\Omega$, $Z_L=50\,\Omega$, $N=10$ gives $\mathrm{HD}_3\approx 55$ dB such that

$$\mathrm{ENOB}=\frac{\mathrm{HD}_3-1.76}{6.02}\approx 9 \text{ bits}$$

Output impedance - what does this mean?

$$R_{out} \approx \frac{g_{mcsc} \cdot g_{mswt}}{g_{src} \cdot g_{csc} \cdot g_{swt}}$$

$$\eta(f) = \frac{Z_{load}(f)}{Z_{out}(f)} \cdot X_0$$



The higher up in frequency, the worse impedance ratio!

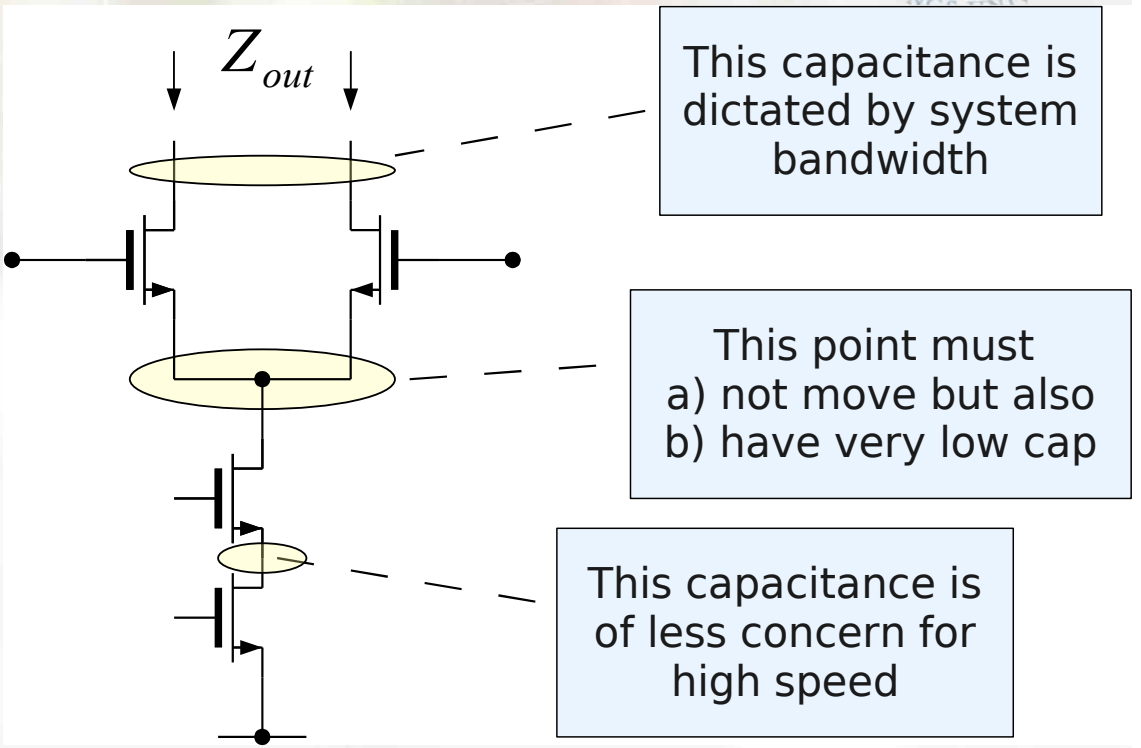
Impact of capacitances

Single-transistor has pole/zero at

$$p_1 = \frac{g_{ds}}{C}, \quad z_1 = \frac{g_m}{C}$$

DC

$$R_{out} = \frac{g_m}{g_P^2} \sim \frac{L_{src} \cdot \sqrt{(W\,L)_{sw}}}{I_{unit}^{1.5}}$$

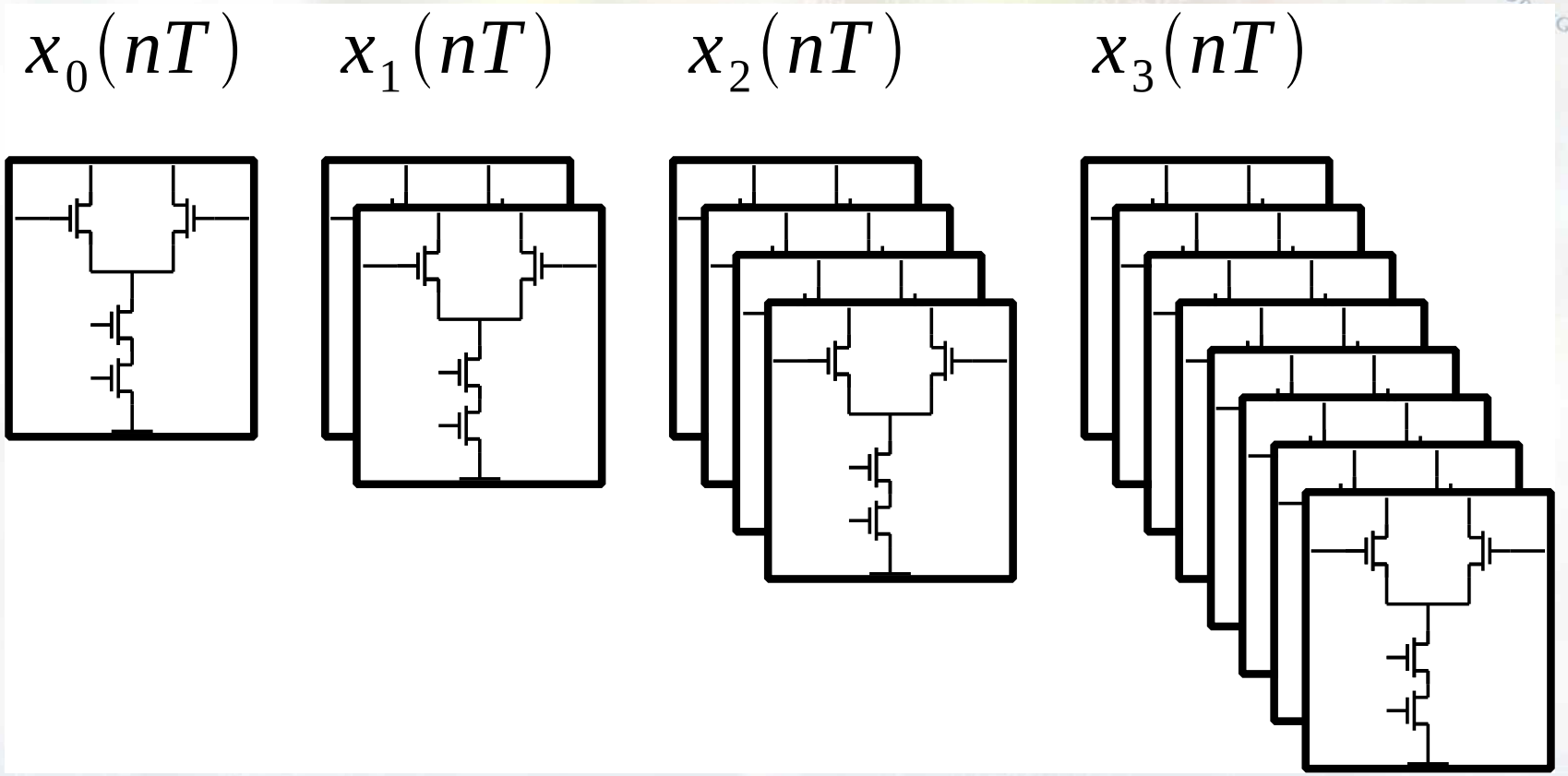


Low current, (very!!!) long source transistor, and large switches.

The latter not feasible due to speed and the fact that the capacitance increases.

Also here we get a requirement on the current and transistors sizes.

Architectural choices, binary

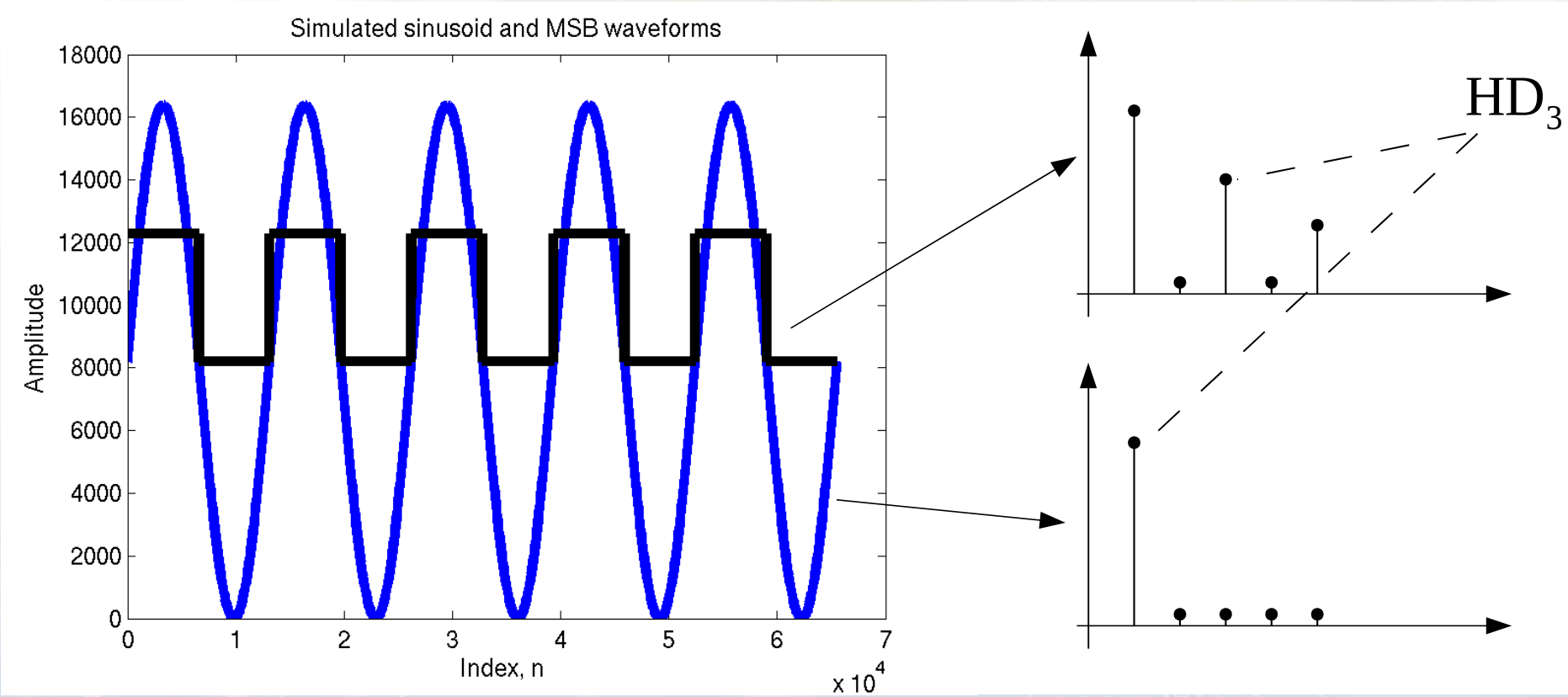


$$I_{out}(X) = X \cdot I_{unit} = \sum x_k \cdot 2^{k-1} \cdot I_{unit}$$

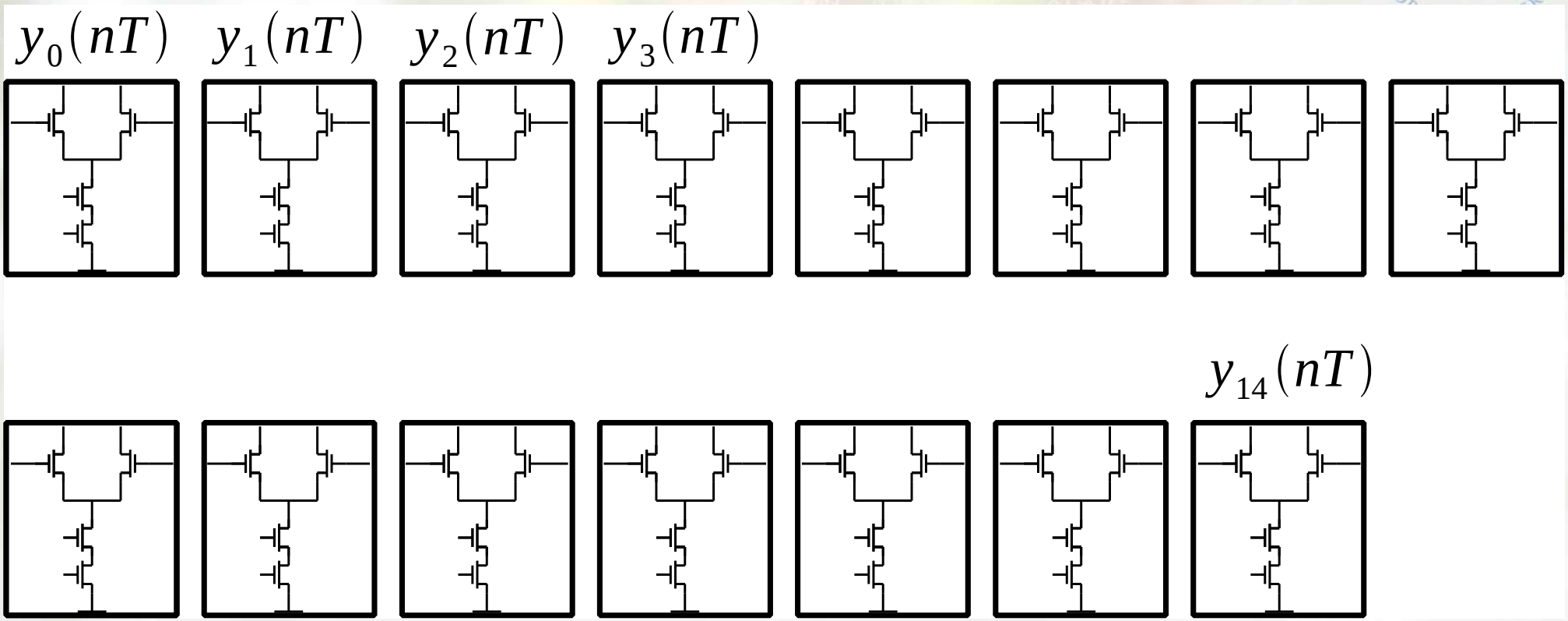
Impact of binary weighted DACs

Mismatch errors will cause differences in weights

Assume errors in the most significant bit (MSB) only in this example.

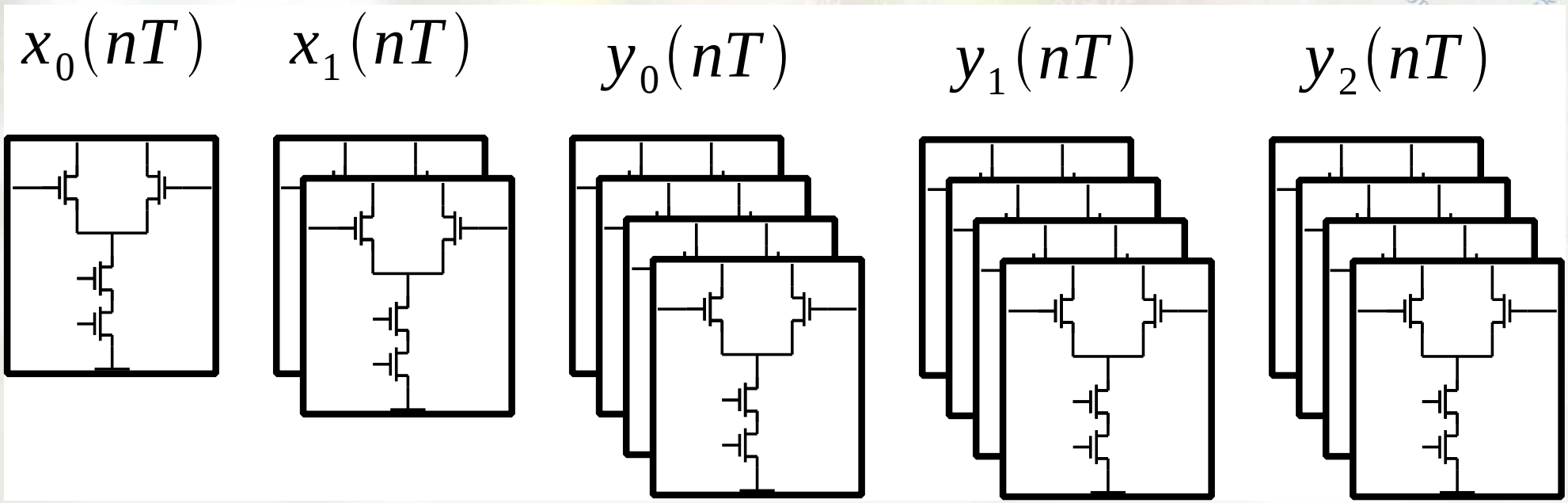


Architectural choices, Unary/Thermometer



$$I_{out}(X) = X \cdot I_{unit} = \sum y_k \cdot 1 \cdot I_{unit}$$

Architectural choices, segmented



$$I_{out}(X) = X \cdot I_{unit} = x_M \cdot \sum y_k \cdot 1 \cdot I_{unit} + \sum x_k \cdot 2^{k-1} \cdot I_{unit}$$

Impact of mismatch 1

Go back to the binary and consider the square-wave error

$$\mathrm{HD}_3 = \frac{P_s}{P_{\epsilon,3}} = \frac{\frac{2^{2N}}{8}\cdot I_{unit}^2}{\frac{2^{N+2}\cdot\sigma_{unit}^2}{9\pi^2}} = 2^N \cdot \frac{9\pi^2}{32}\cdot\frac{I_{unit}^2}{\sigma_{unit}^2} \approx \frac{3\cdot 2^N}{\sigma_{unit}^2 / I_{unit}^2} = \frac{3\cdot 2^N}{\sigma_r^2}$$

All architectures (including quantization noise)

$$\mathrm{SNDR} = \frac{3\cdot 2^{2N-1}}{1+3\cdot\sigma_r^2\cdot 2^{N+1}}$$

There is a trade-off between linearity and noise!

Which is worst for your application?

Impact of mismatch 2

Consider the effective number of bits instead:

$$\text{SNDR} = \frac{3 \cdot 2^{2N-1}}{1 + 6 \cdot \sigma_r^2 \cdot 2^N} \Rightarrow \text{ENOB} = N - \frac{1}{2} \cdot \log_2\left(1 + 6\sigma_r^2 \cdot 2^N\right)$$

such that (assume 3-sigma for higher yield)

$$\sigma_r = \frac{1}{3} \cdot \sqrt{\frac{2^{2(N-\text{ENOB})} - 1}{6 \cdot 2^N}}$$

Assume the target is **12-bit** performance with a nominal **14-bit** DAC:

$$\sigma_r \approx 0.4 \ \%$$

Is this a big number?

Impact of mismatch 3

The random, relative error in current is given by

$$\sigma_r^2 = \sigma^2\left(\frac{\Delta I}{I_{unit}}\right) = \frac{A_\beta^2}{W\,L} + \frac{4\,A_{VT}^2}{V_{eff}^2 \cdot W\,L}$$ giving $$W\,L = \frac{1}{\sigma_r^2}\cdot\left(A_\beta^2 + \frac{4\,A_{VT}^2}{V_{eff}^2}\right)$$

Example values:

$V_{eff} = 0.5$ V, $A_\beta = 2$ % um, $A_{VT} = 7$ mV um, and $\sigma_r \approx 0.4$ %

which gives

$$W\,L \approx 70 \text{ sq um}$$

Impact of mismatch 4

But there are also gradients and intradependencies at hand.

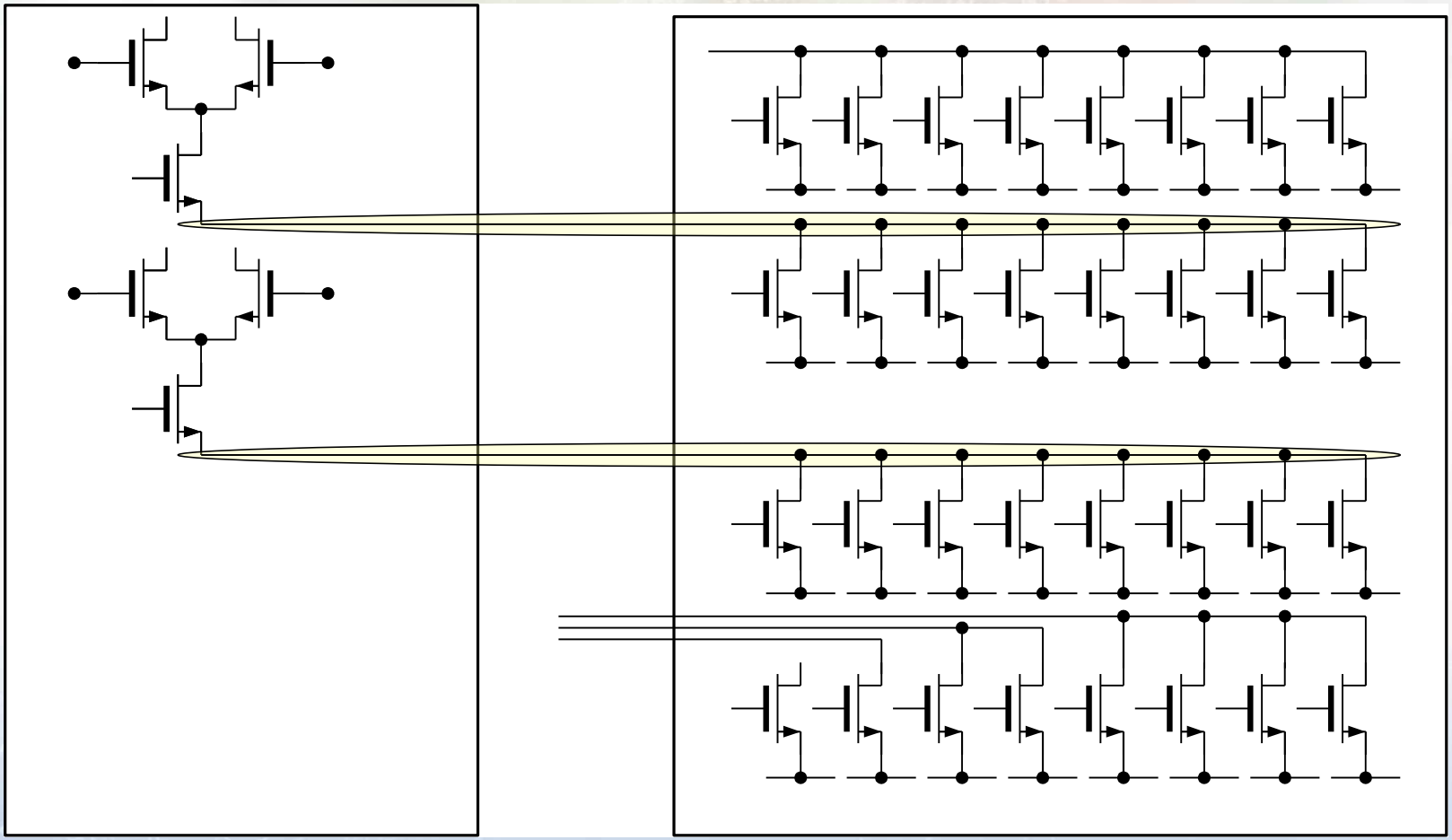
Bad vs better layout:

N/A	0	1	1
2	2	2	2
4	4	4	4
4	4	4	4

4	N/A	2	4
1	4	0	2
2	4	4	1
4	2	4	4

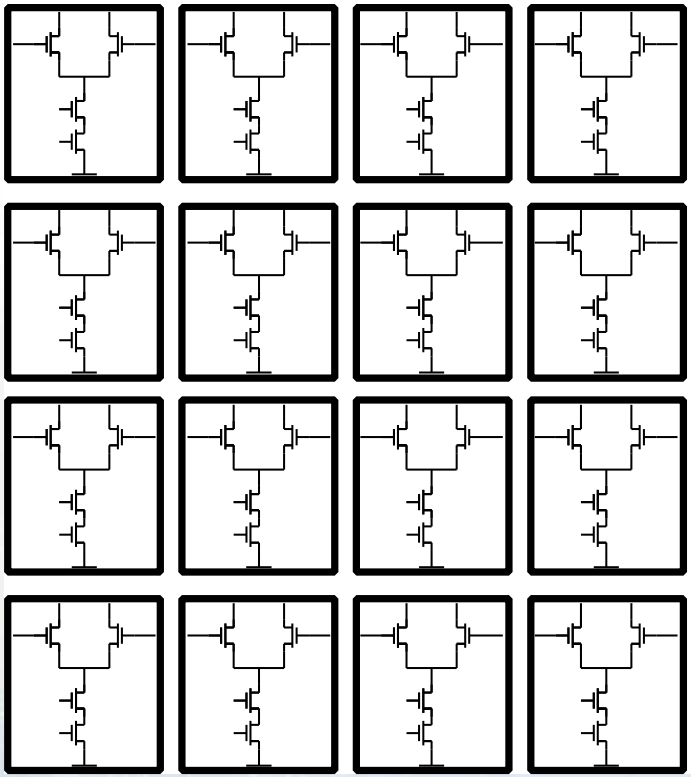
Minimizing the cap in the sensitive node 1

Swatch array

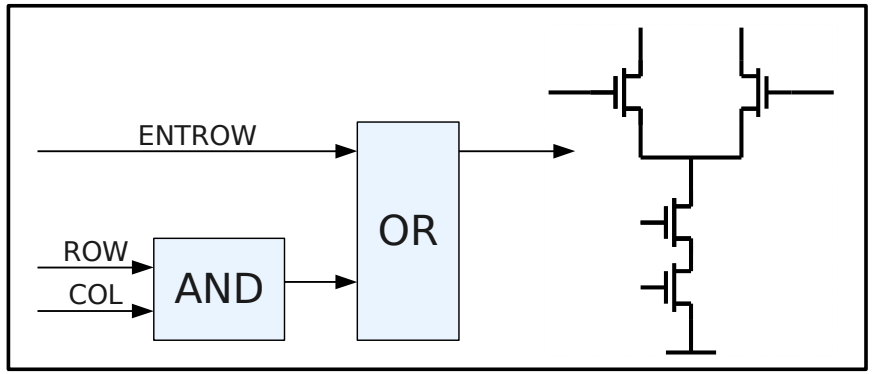


Minimizing the cap in the sensitive node 2

Encoded array structure

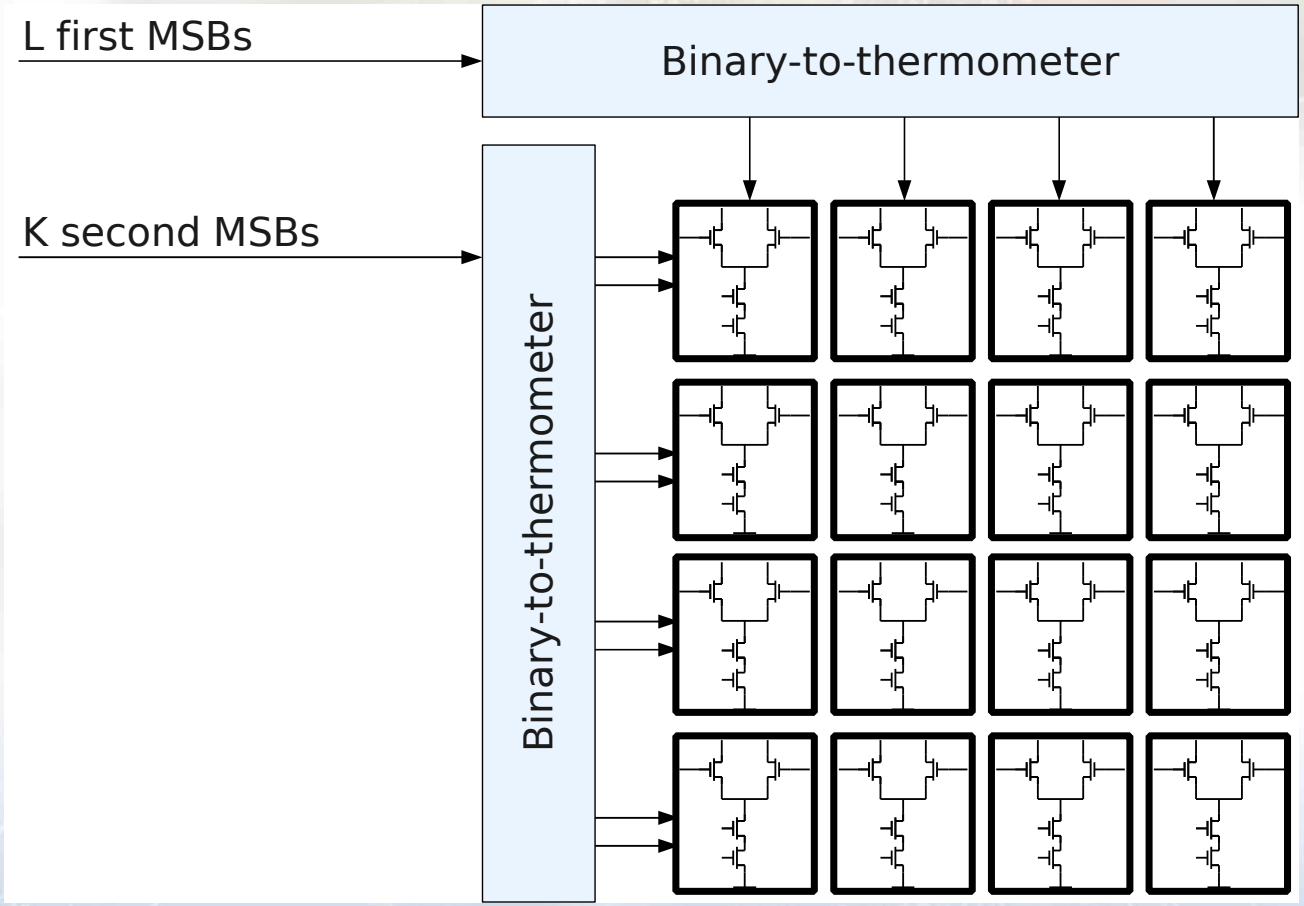


Switch is turned on if entire row is selected or if row and column are selected.

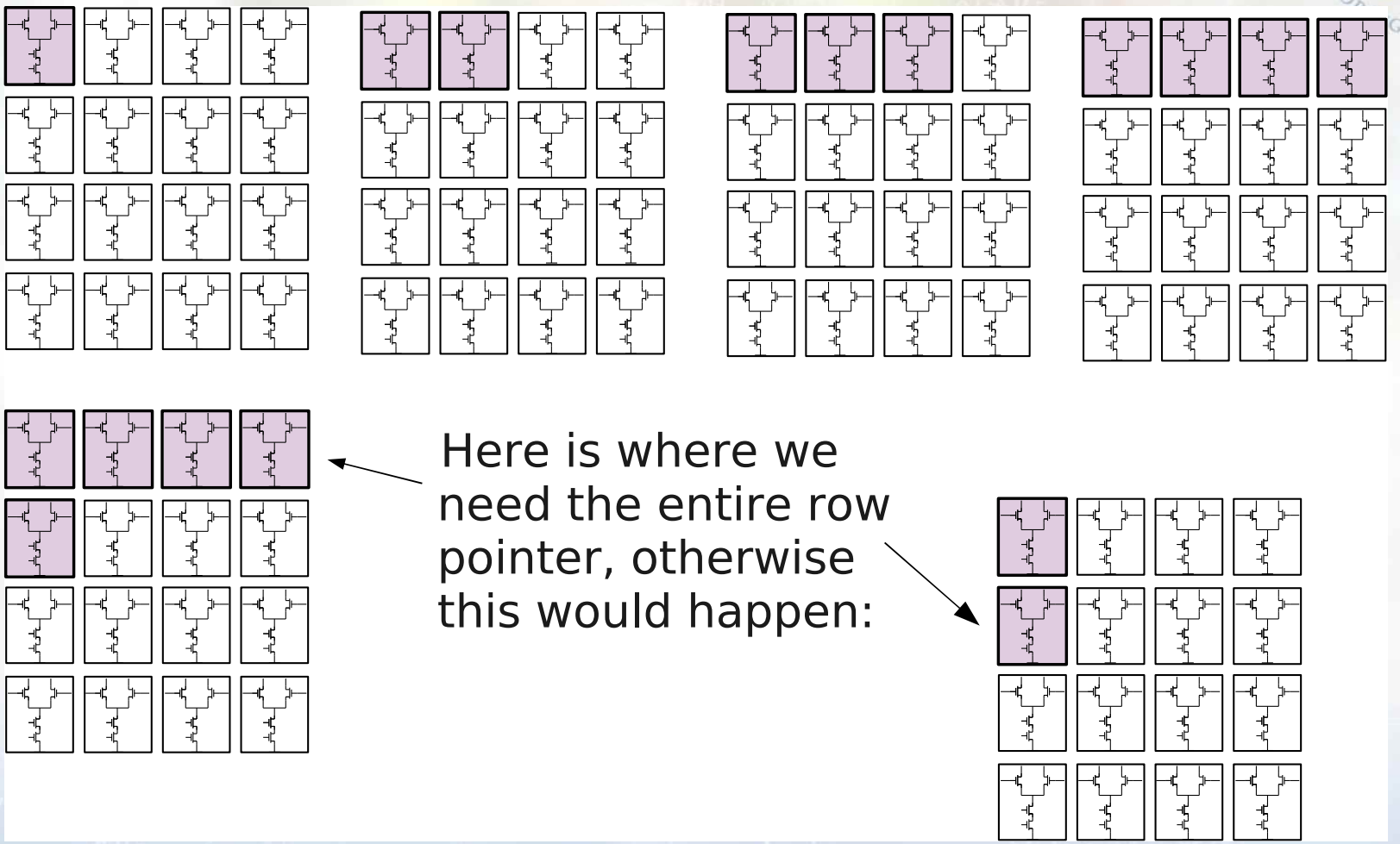


Minimizing the cap in the sensitive node 2

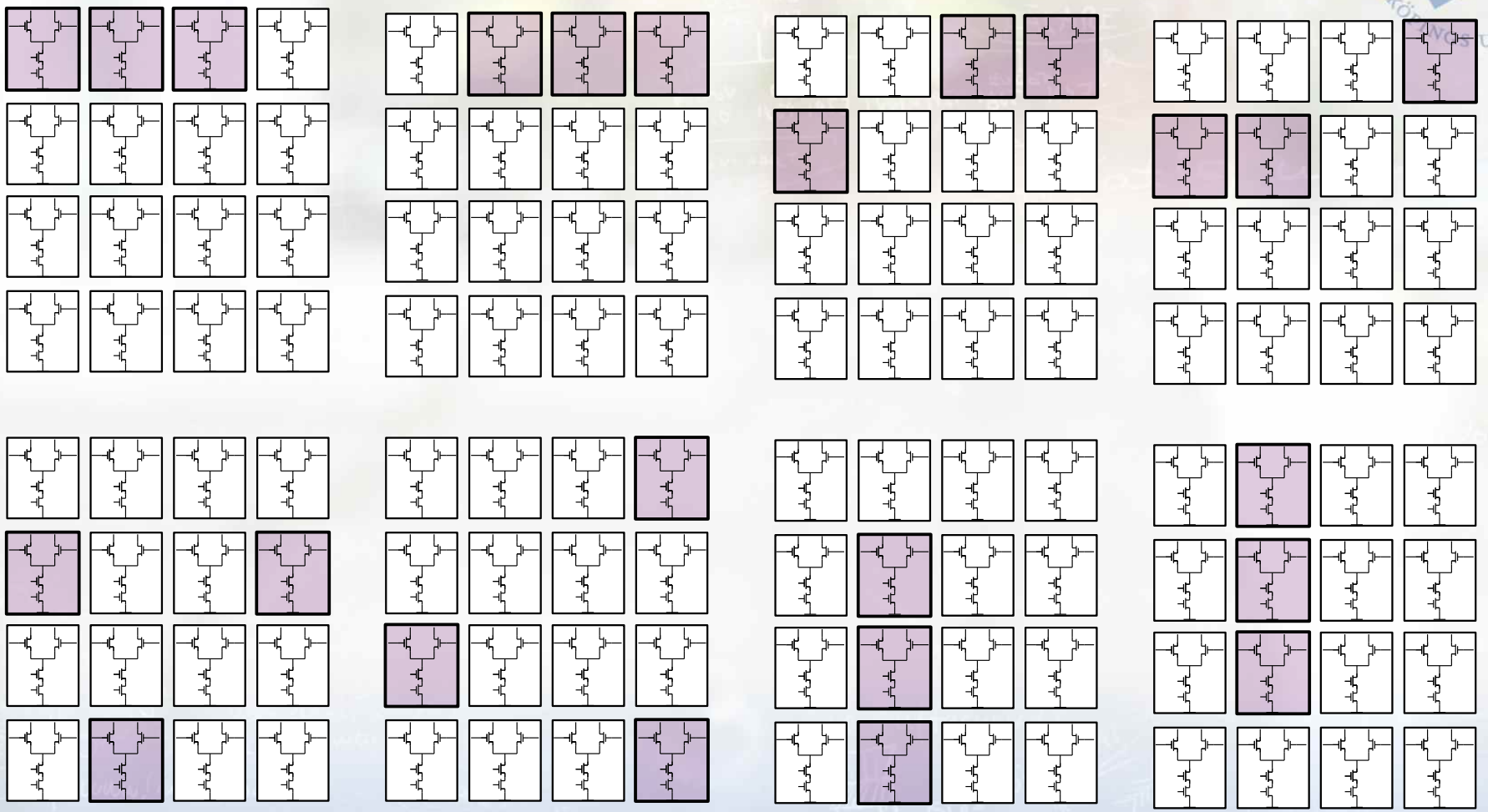
Array, cont'd



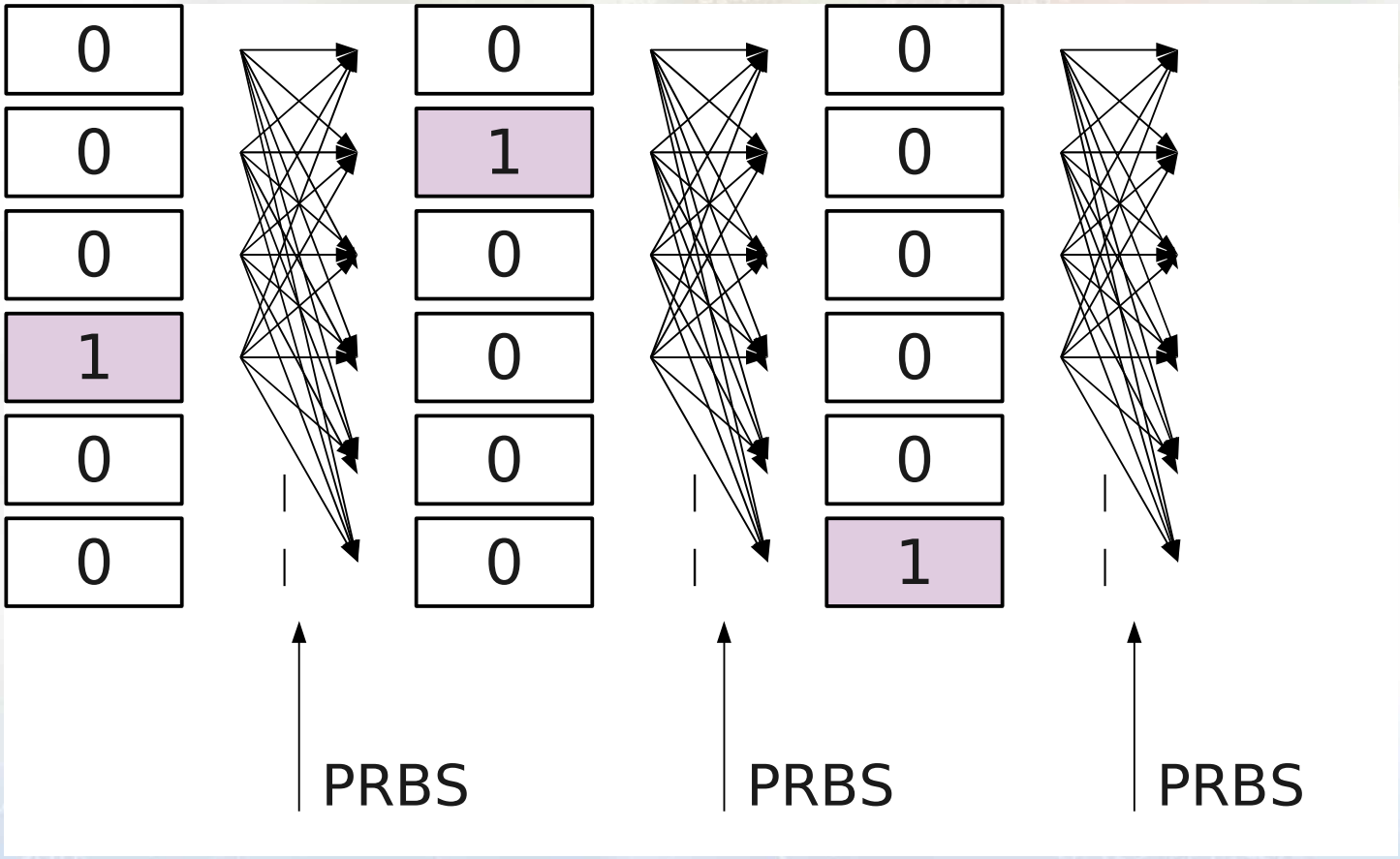
Array-based architecture



Array-based architecture

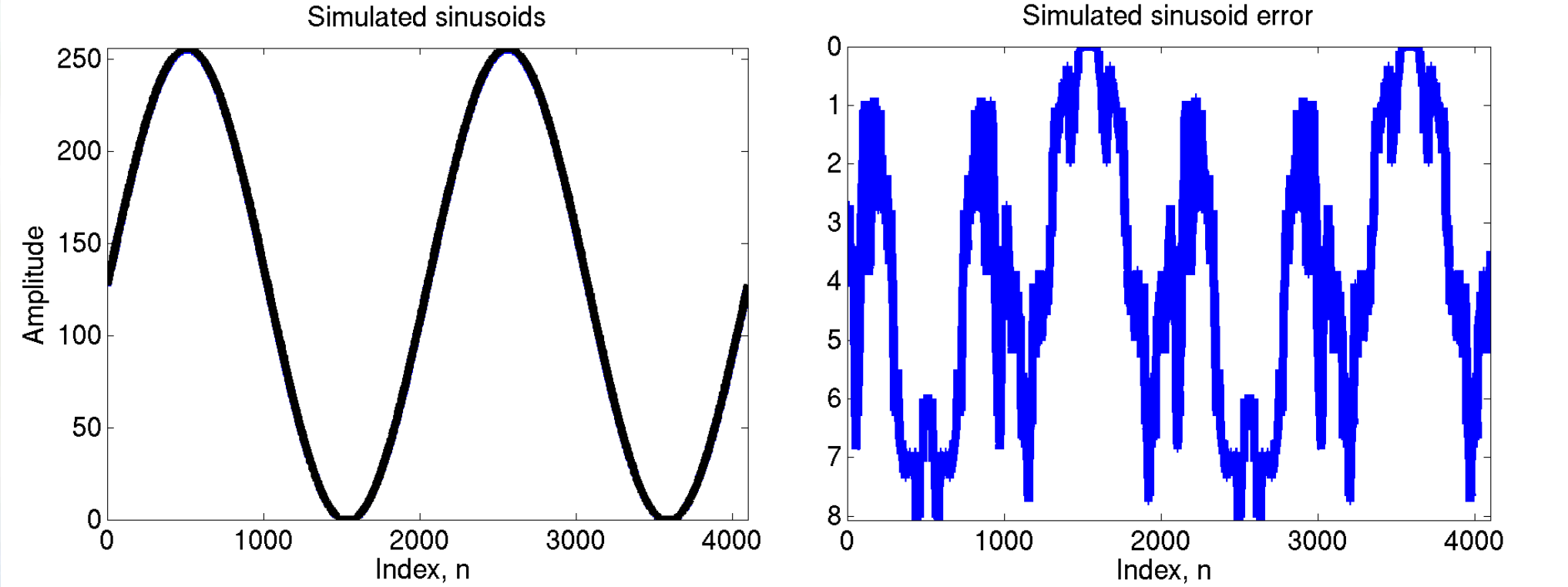


Redundancy implies we can scramble!



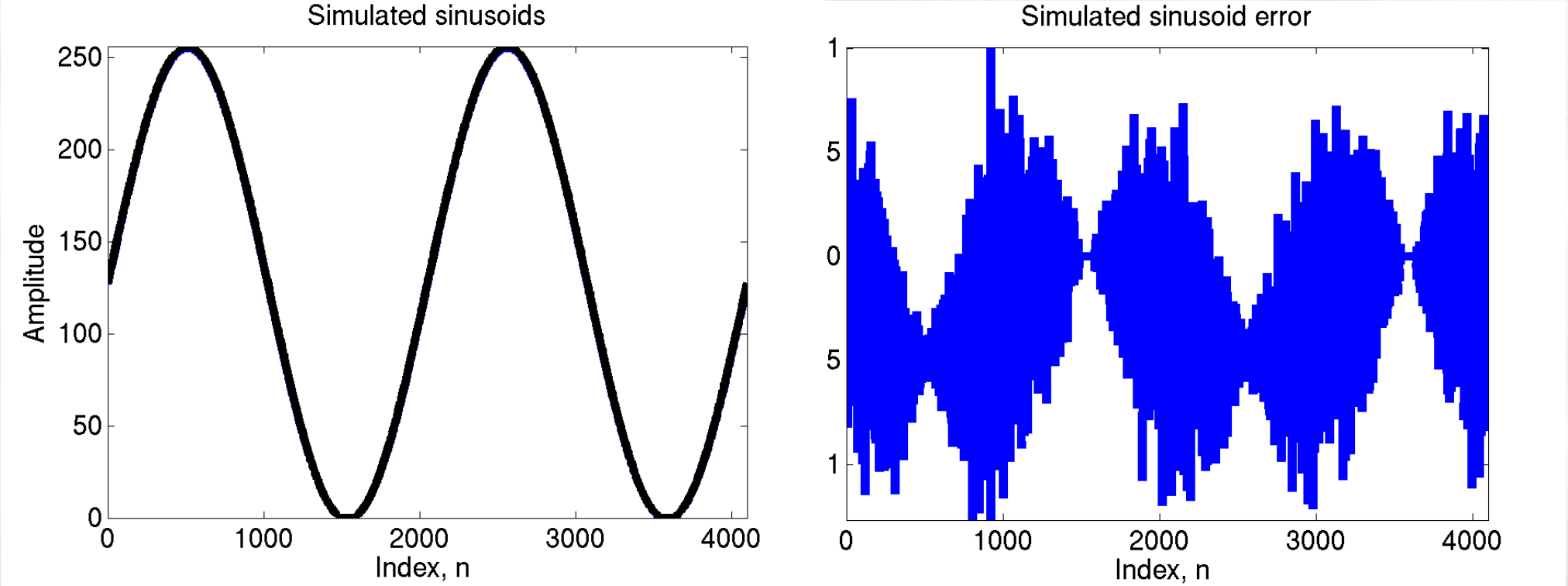
No scrambled structure

The error is strongly signal-dependent (c.f. low number of bits)



Scrambled structure

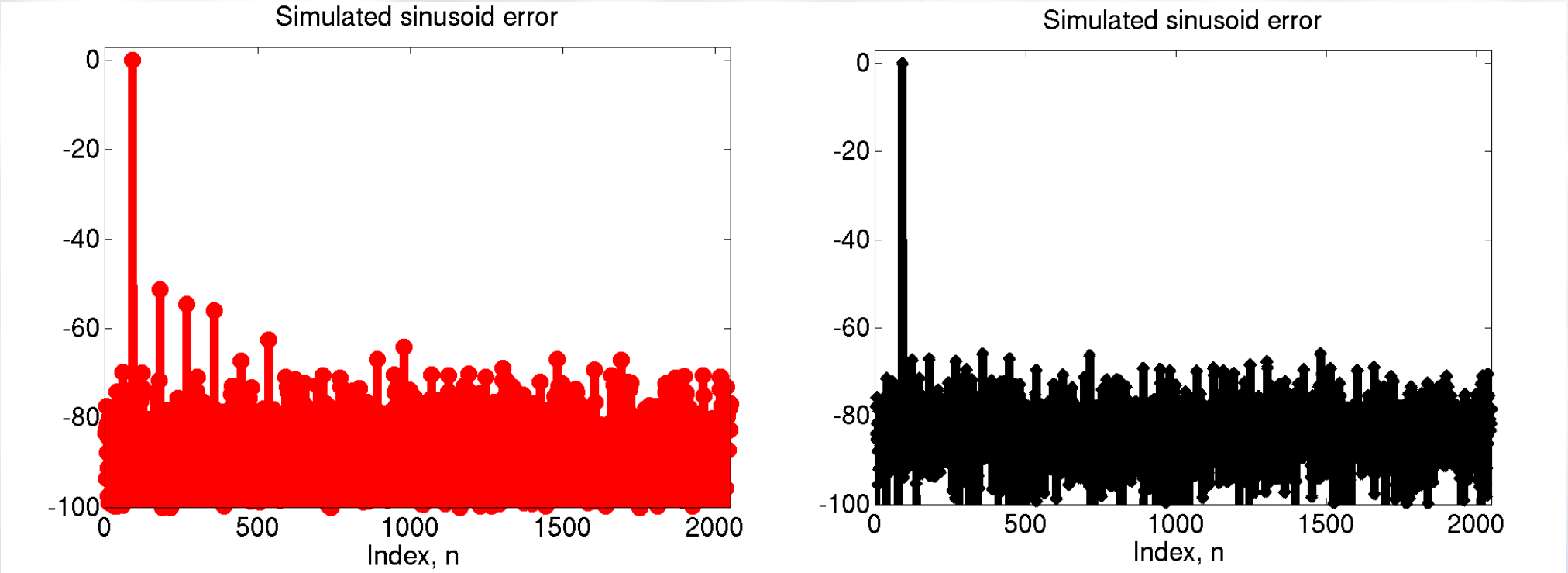
Scrambling removes some (most) of the signal-dependency



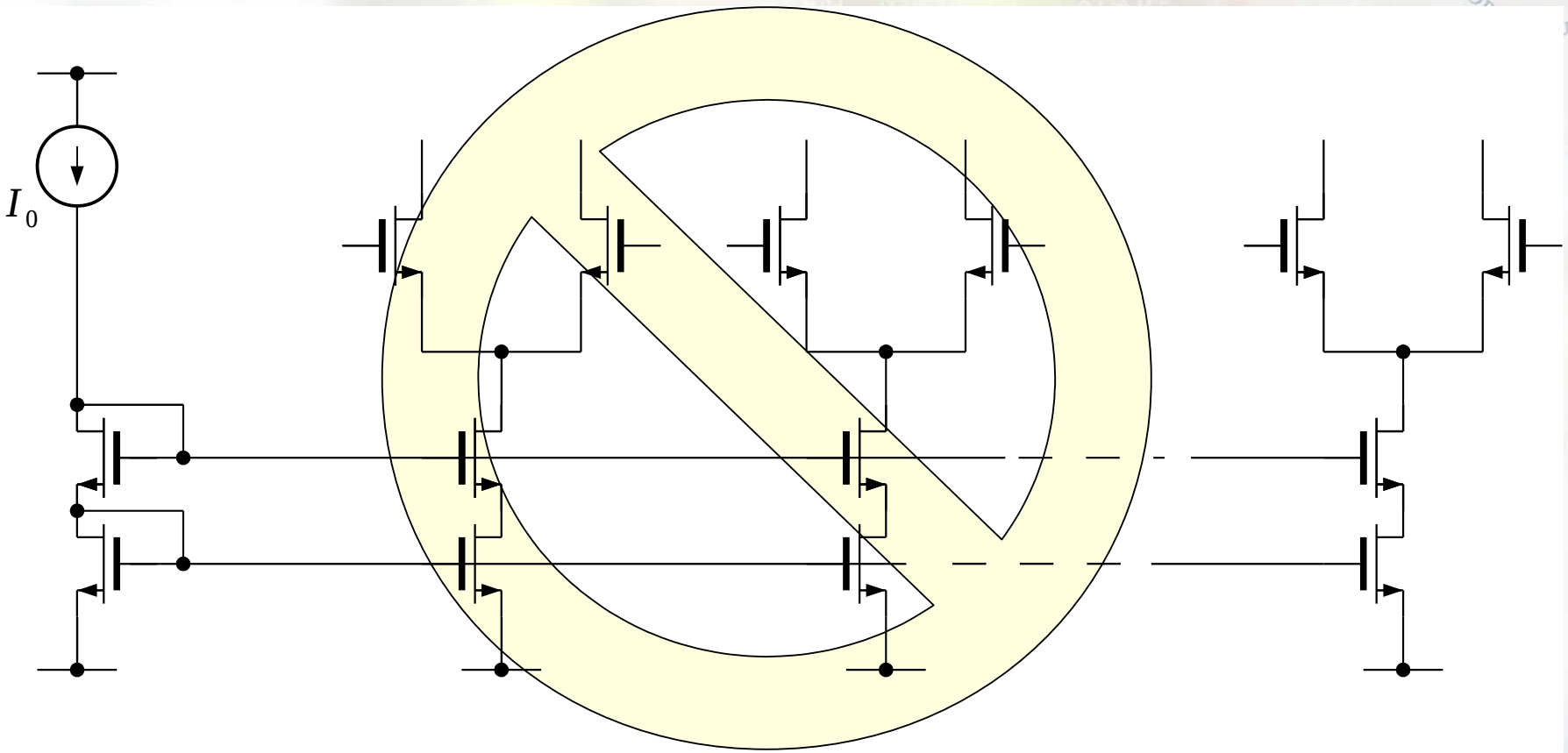
The effect in the frequency domain

Notice, though, that the SNDR is the same!

Improve the SNDR by filtering (already in place due to the oversampling)



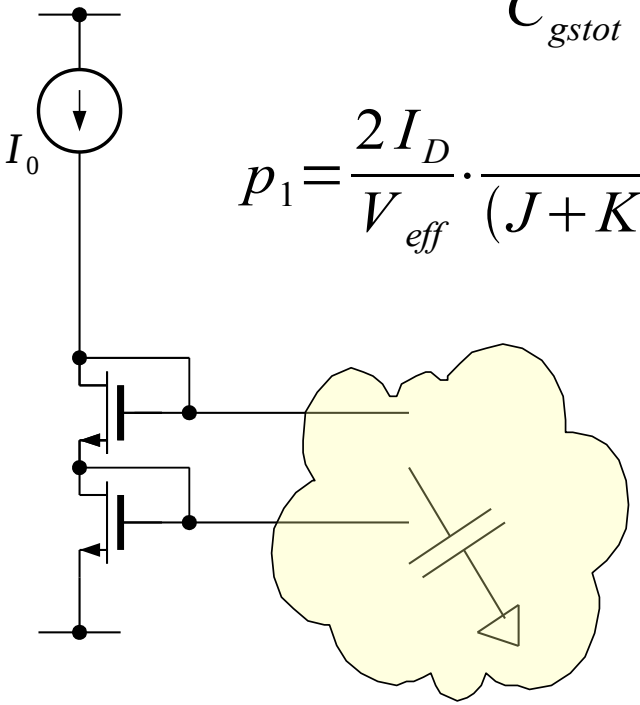
Biasing scheme



~16000 current sources for a 16-bit converter

Biasing scheme

$$p_1 = \frac{g_m}{C_{gstot}}$$



$$p_1 = \frac{2I_D}{V_{eff}} \cdot \frac{1}{(J+K)\cdot C_{ox}\cdot W\cdot L/2} = \frac{2I_{unit}\cdot J}{V_{eff}} \cdot \frac{1}{(J+K)\cdot C_{ox}\cdot W\cdot L/2}$$

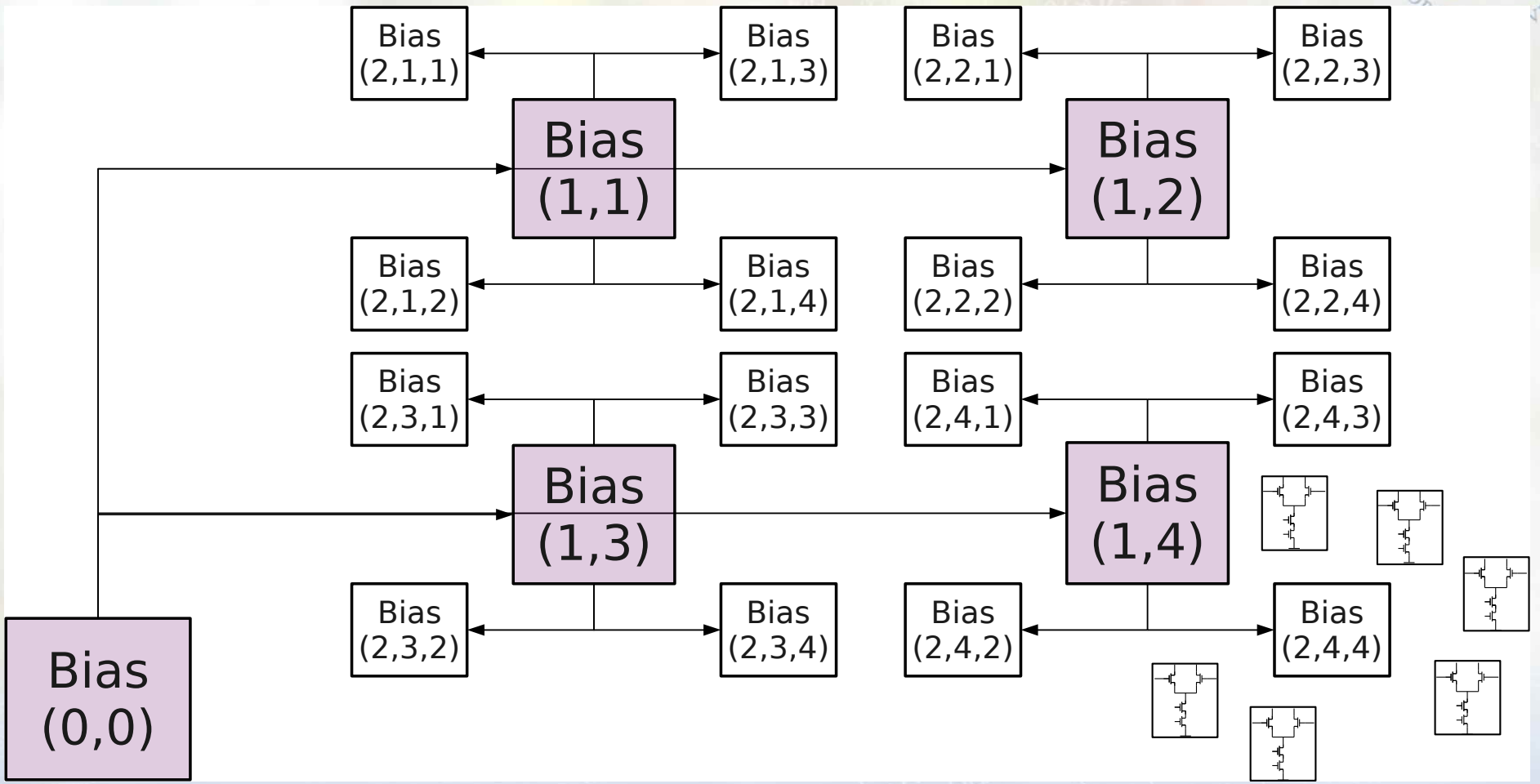
$$p_1 \sim V_{eff} \cdot \frac{1}{1+\frac{K}{J}} \cdot \frac{1}{L^2}$$

Large ratio implies low pole implies slow

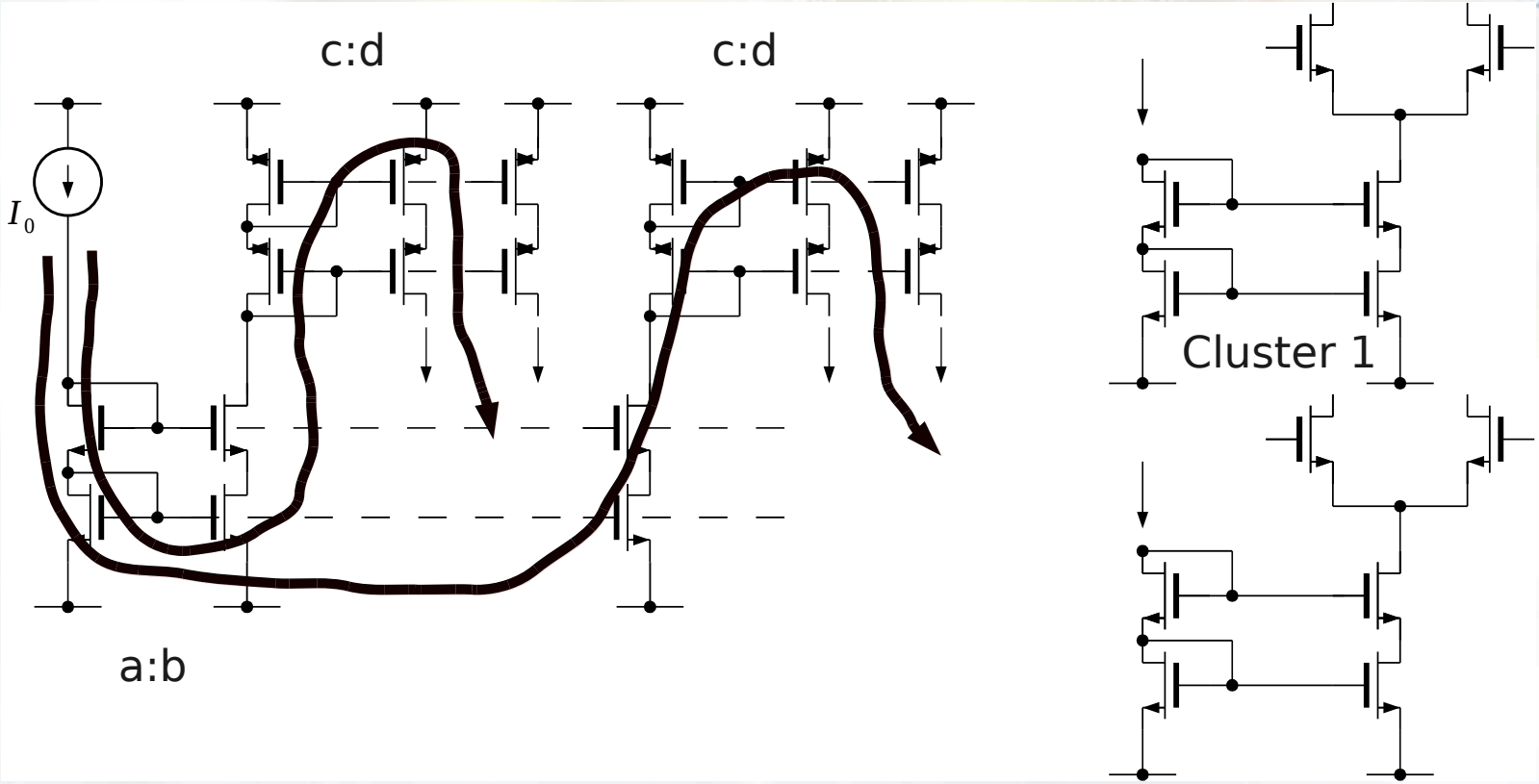
⇒ Taper to speed up.

Trade-off between speed and noise supression!

Biasing scheme

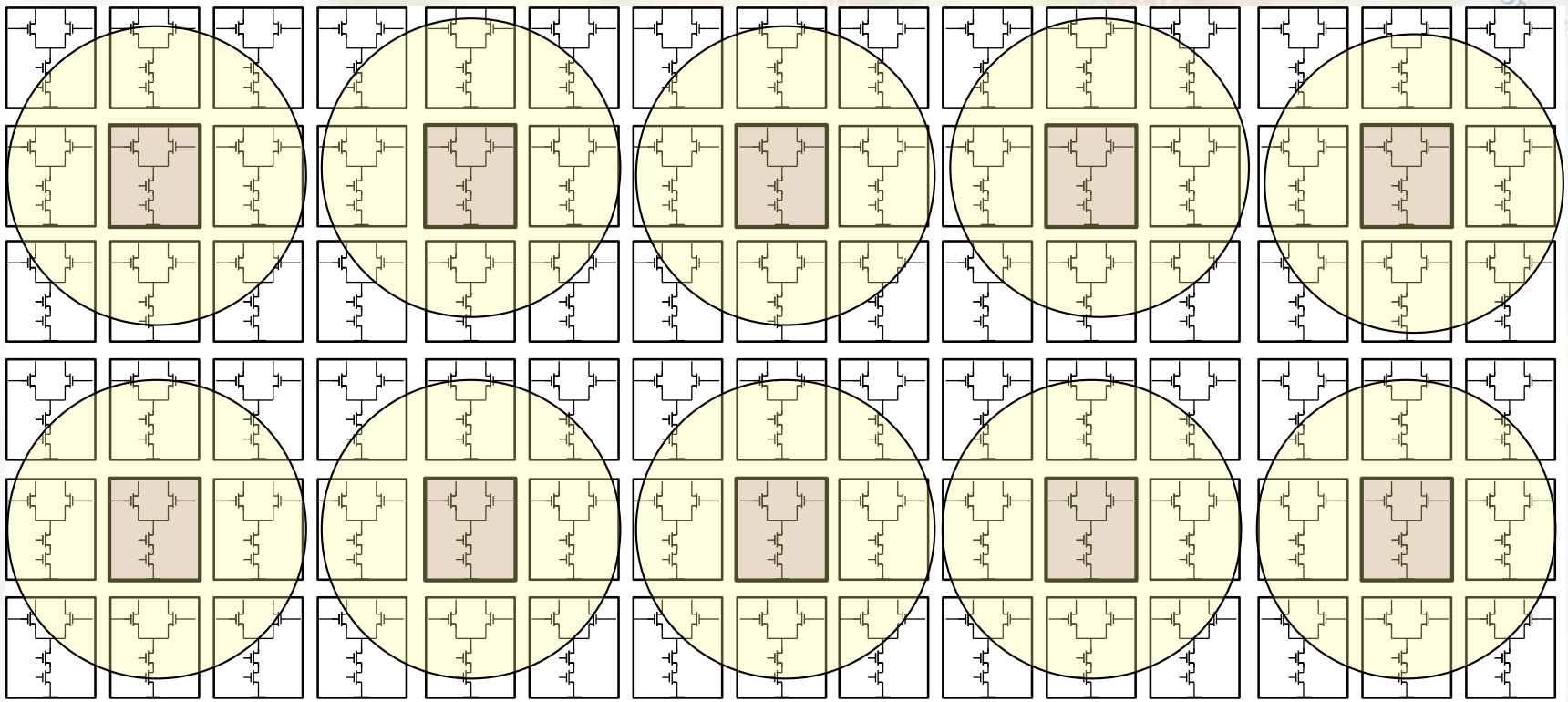


Biasing scheme



More branches implies more mismatch and noise. Trade-off!

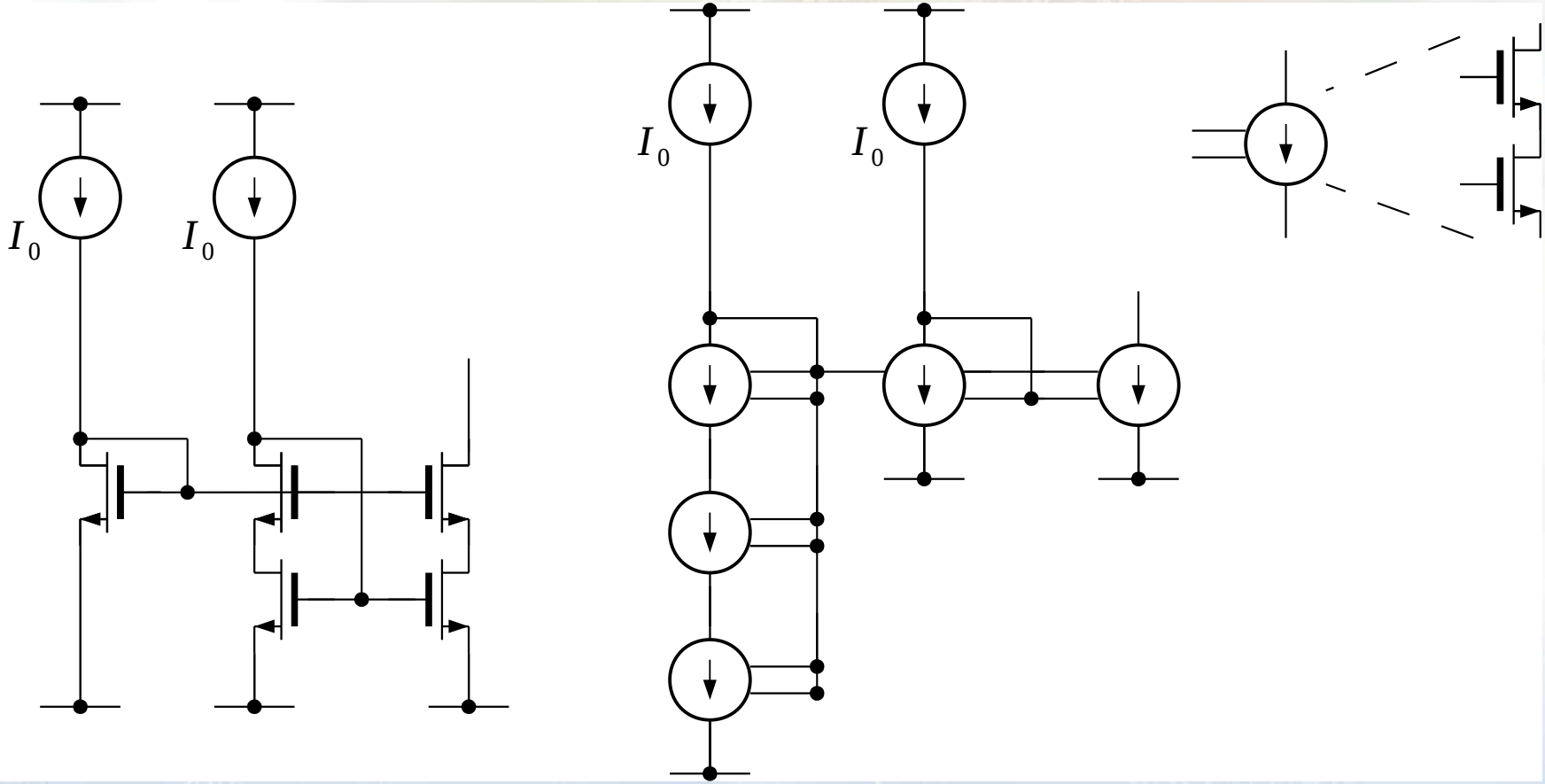
Biasing scheme



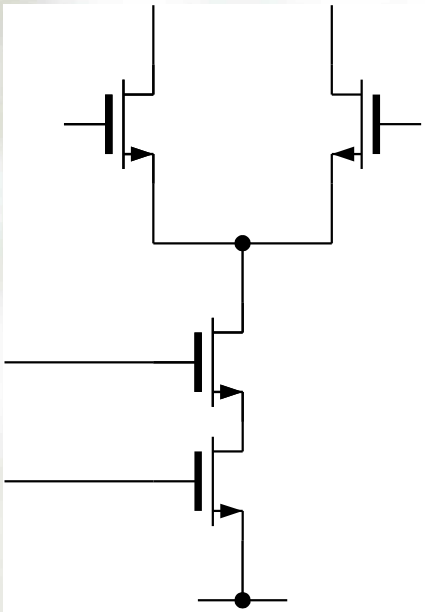
Sacrifice some of the unit cells and replace with bias components. Let them distribute bias to several rows and columns! (N.b. a row is signal dependent!)

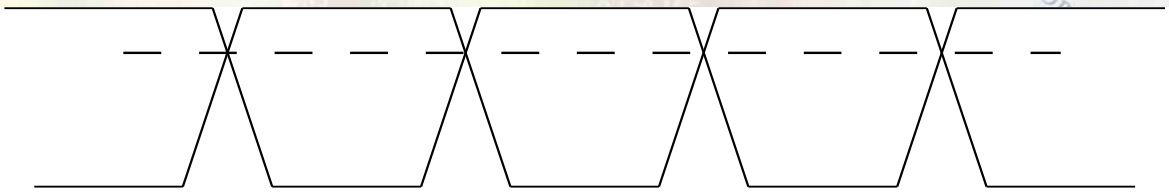
Biasing scheme, use wide-swing mirrors

Use the unit current source as a macro to generate cascode voltage



Switching scheme

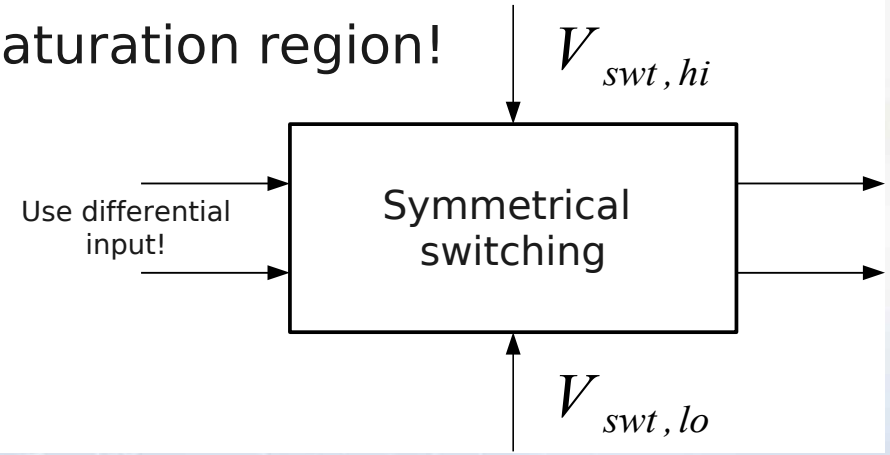




Overlapping switch signals, such that the switch is never turned off > use some kind of SR latch or so.

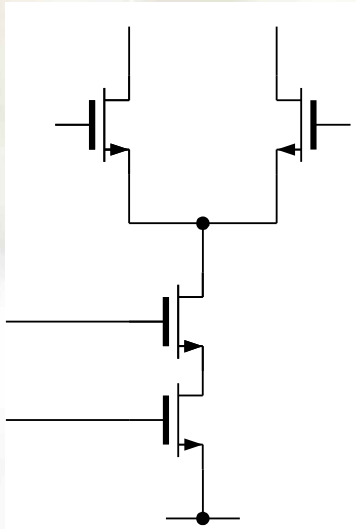
Switching must be symmetrical and data independent!

Switches are operating in saturation region!



Switching levels

Saturation should be guaranteed to obtain high impedance



$$V_{out,lo} - V_{cm} > V_{swt,hi} - V_{cm} - V_T$$

$$V_{DD} - V_{swing} > V_{swt,hi} - V_T$$

$$-V_{swing} > -V_T \Rightarrow V_T > V_{swing}$$

OUCH!!!

There is a risk that we slip out of saturation region

This requirement gives us a maximum swing at the output, ie., a dependency between current and load impedance.

$$I_{max} = \frac{V_{swing}}{R_{load}} \Rightarrow I_{unit} = \frac{V_{swing}}{R_{load} \cdot 2^N} < \frac{V_T}{R_{load} \cdot 2^N}$$

Concluding remarks

Mismatch

$$WL = \frac{1}{\sigma_r^2} \cdot \left(A_\beta^2 + \frac{4 A_{VT}^2}{V_{eff}^2} \right) \quad \text{where} \quad \sigma_r = \frac{1}{3} \cdot \sqrt{\frac{2^{2(N-\mathrm{ENOB})} - 1}{6 \cdot 2^N}}$$

Swing

$$I_{unit} < \frac{V_T}{R_L \cdot 2^N}$$

Impedance (example single-transistor source)

$$R_{out} = \frac{g_m}{g_P^2} \sim \frac{L_{src} \cdot \sqrt{(WL)_{sw}}}{I_{unit}^{1.5}} \quad \text{where} \quad \mathrm{ENOB} \approx 3.2 + 6.6 \cdot \log_{10} \frac{Z_{unit}}{Z_L} - 2 \cdot N \ \text{(HD3)}$$

which then is combined with

$$I_{unit} = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot V_{eff}^2$$

Concluding remarks (Omitted parts)

Noise from individual current sources:

$$i_{tot}^2(f) = 2^N \cdot i_{unit}^2(f) = \frac{4kT\gamma \cdot 2^N}{g_m} = \frac{4kT\gamma \cdot 2^N}{\sqrt{2\alpha I_{unit}}}$$

And quite a few others:

- Noise from biasing scheme
- PSRR
- CMRR
- Total maximum area
- Power consumption (don't forget the digital parts)
- Bandwidth requirements

What did we do today?

Oversampling

- Sigma-delta modulator and its principles

Case-study current-steering DAC

- A general study of the high-speed current-steering DAC
- Some design guidance
- Understanding impact of impedance and mismatch

What will we do next time?

Case-study pipelined ADC

- Architecture
- Comparator
- Sample-and-hold

Wrap-up