Lecture 4, ATIK

Operational (transconductance) amplifiers, Noise

LiU EXPANDING REALITY

What did we do last time?

Wrapping up the simple amplifier stages and current mirrors

Suggesting cascodes to increase gain

Multiple poles

Stability and stability analysis

Compensation

What will we do today?

Differential circuits

- Why differential?

Operational amplifiers

- More on how we design them

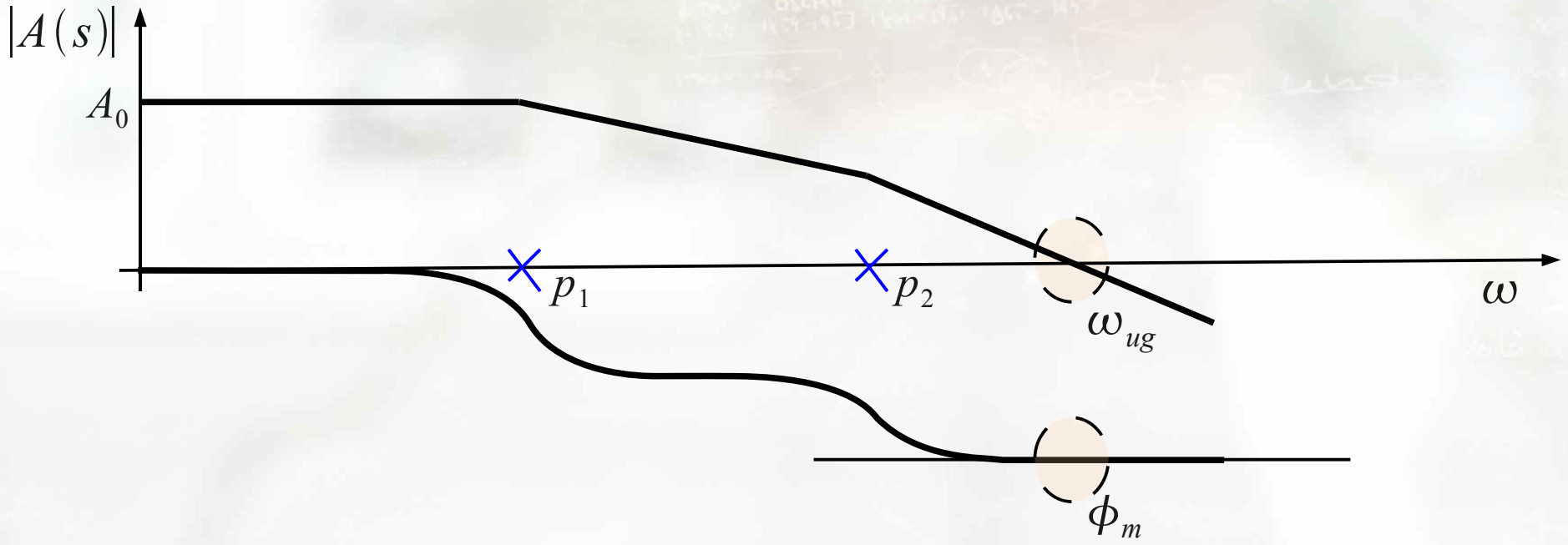
Circuit noise

- Thermal and flicker noise
- Noise bandwidth

Wrapping up CMOS design!

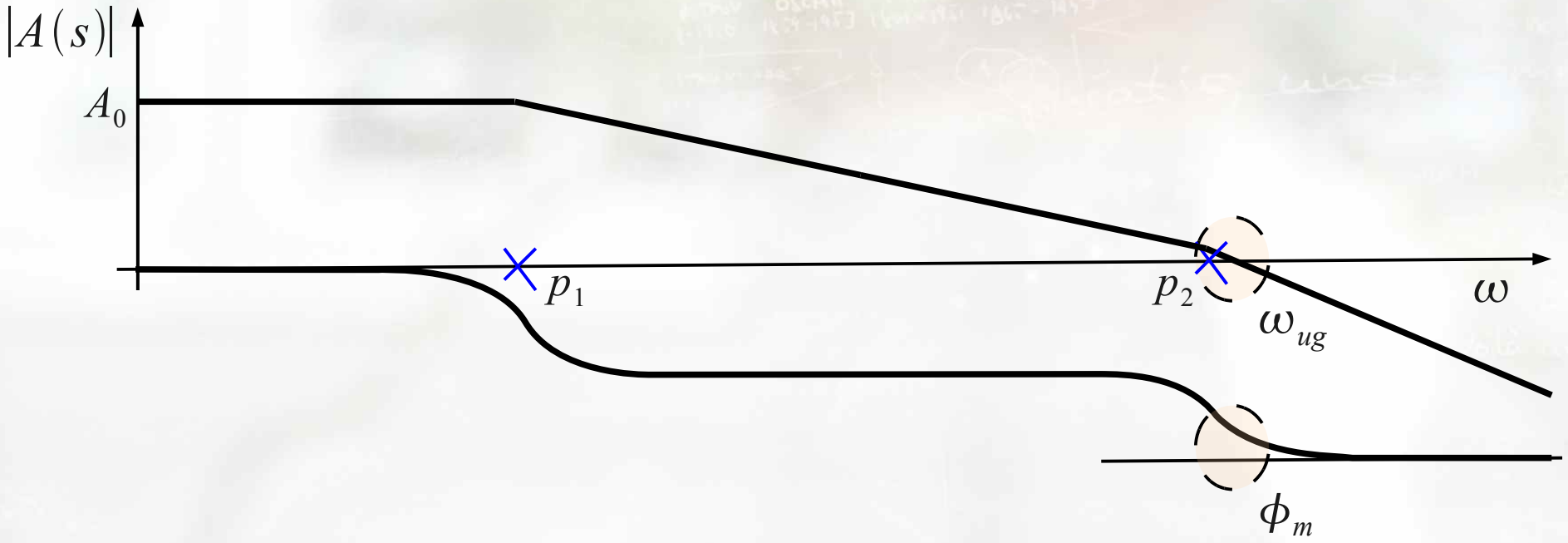
Poles and zeros revisited

Stable?



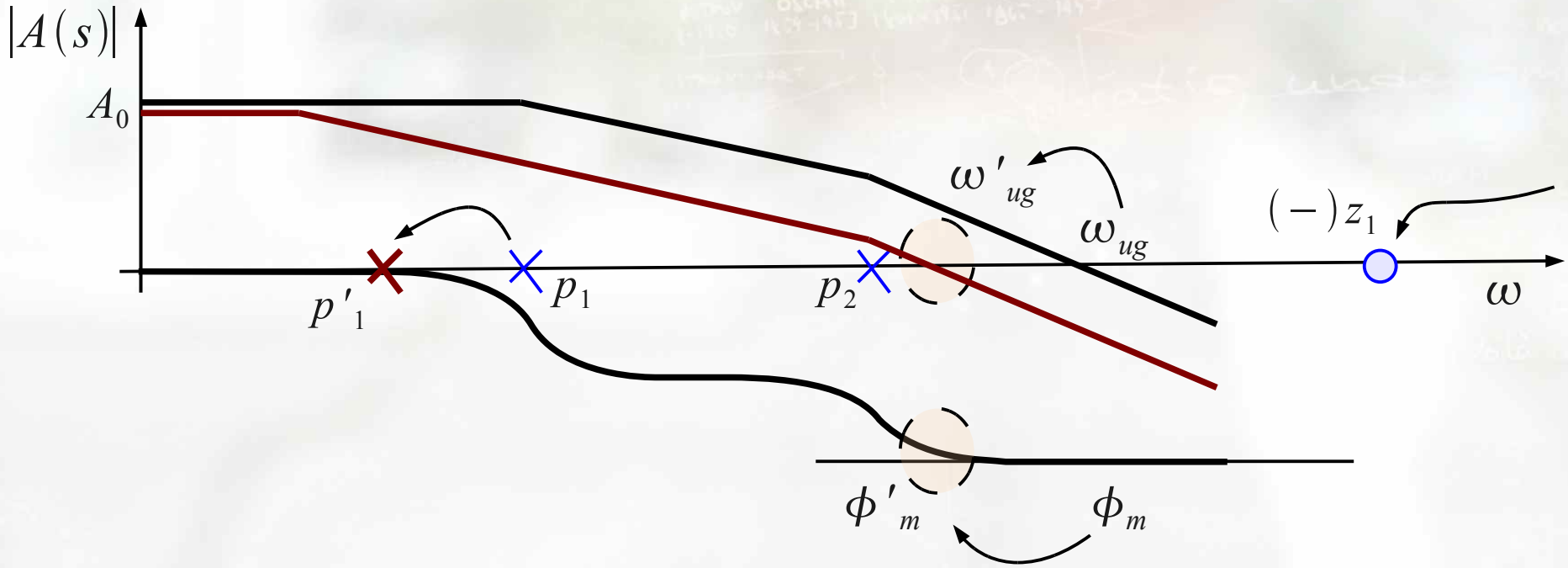
Poles and zeros revisited

Stable?



Compensation

What is the cost associated with compensation?



Compensation, two cases:

1) "Internal" node sees a low-impedance node

Typically: output load dominates, and we should drive a capacitive load

Load-compensation, i.e., increase cap externally

2) "Internal" node sees a high-impedance node

Typically: internal load dominates, and we should drive a resistive load

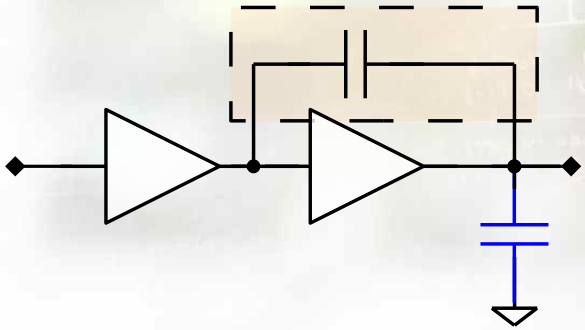
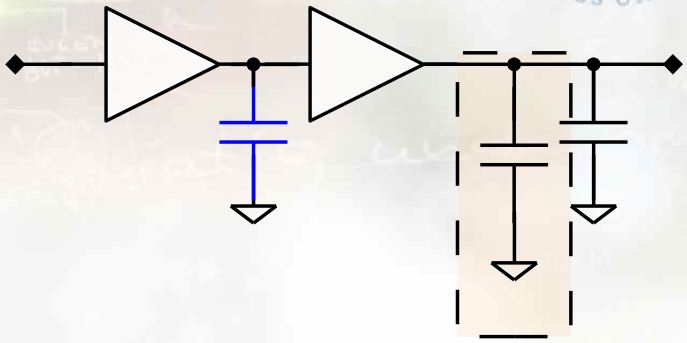
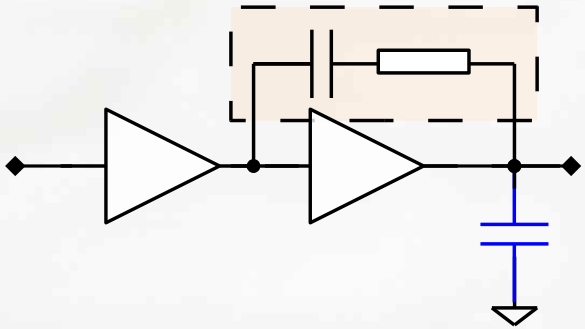
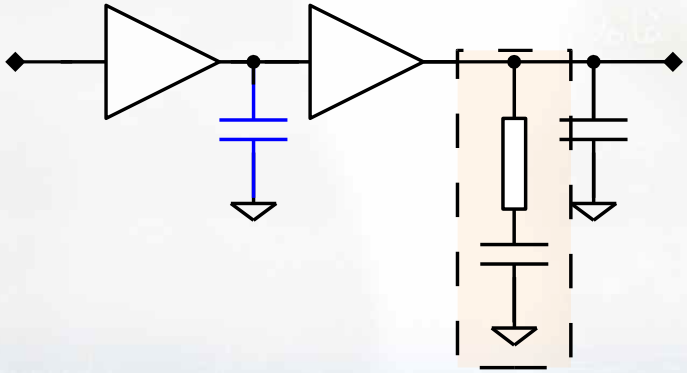
Miller-compensation, i.e., utilize the second-stage gain to multiply C_C

As always, some exceptions to the rule:

We could add common-drain at output

Nested compensation, active compensation, ... and more ...

Compensation compiled:

	Miller	Load compensation
Cap		
Cap + Res		

Rule-of-thumbs for hand-calculation

Use MATLAB or similar to support your calculations for better understanding

See for example

```
/site/edu/es/TSTE08/antikPoleZero.m
/site/edu/es/TSTE08/antikSettling.m
```

In the end, use the simulator.

It has to be robust over several corners, temperatures, and other variations.

Hand calculations are incorrect per definition

Model corresponds quite well with circuit once you have identified the different stages

See for example exercises

Differential signals

Differential signals

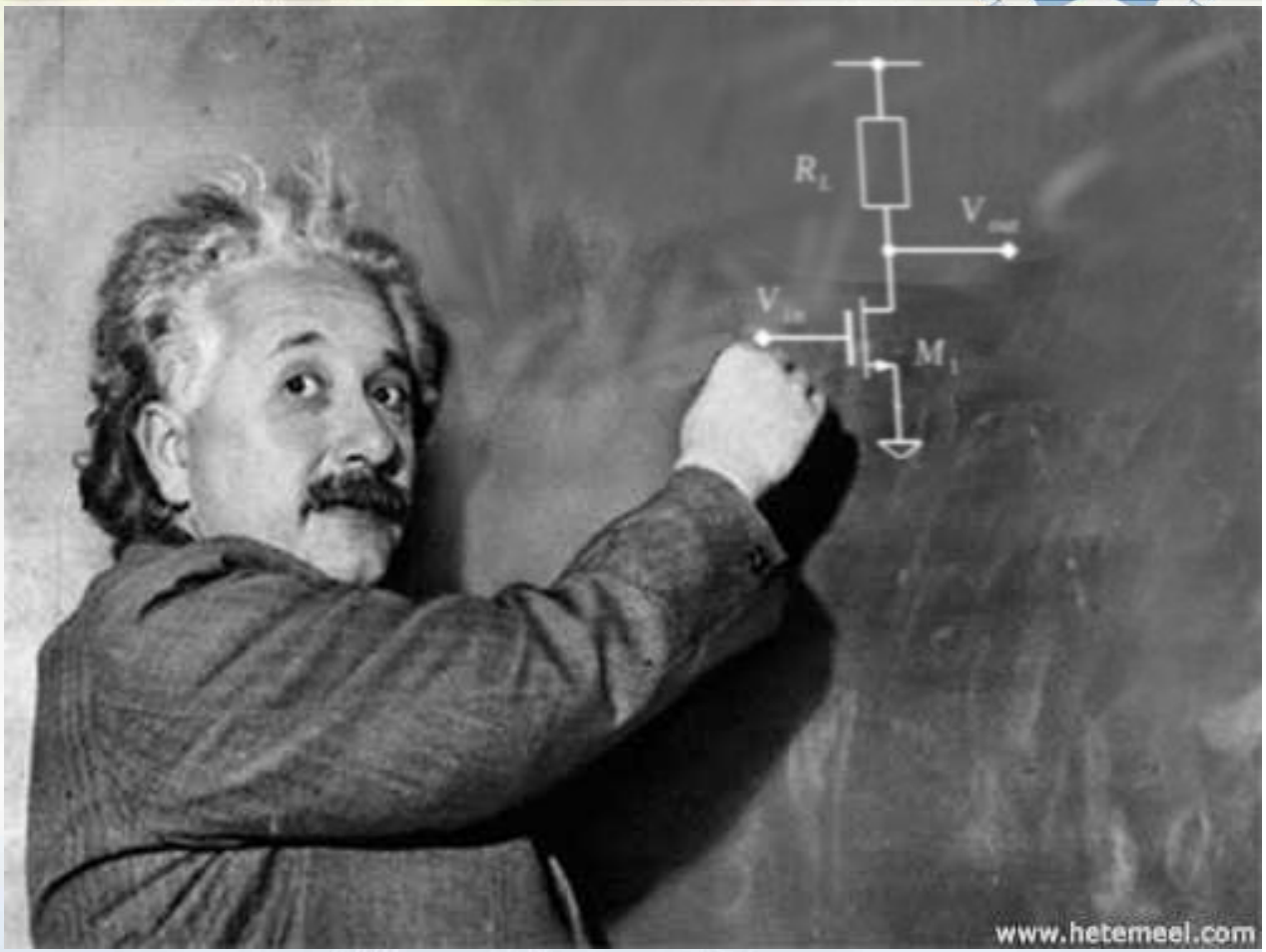
$$\Delta V = V_p - V_n$$

Common-mode signal

$$\nabla V = \frac{V_p + V_n}{2}$$

Common-mode supression

Should cancel common-mode (why?)



Differential signals, the matrix

Compile the transfer functions into handy matrix

$$\begin{bmatrix} \Delta V_{out} \\ \nabla V_{out} \end{bmatrix} = \begin{bmatrix} A_{df} & A_{df,cm} \\ A_{cm,df} & A_{cm} \end{bmatrix} \begin{bmatrix} \Delta V_{in} \\ \nabla V_{in} \end{bmatrix}$$

Common-mode rejection ratio

$$\mathrm{CMRR} = \frac{A_{df}}{A_{cm}}$$

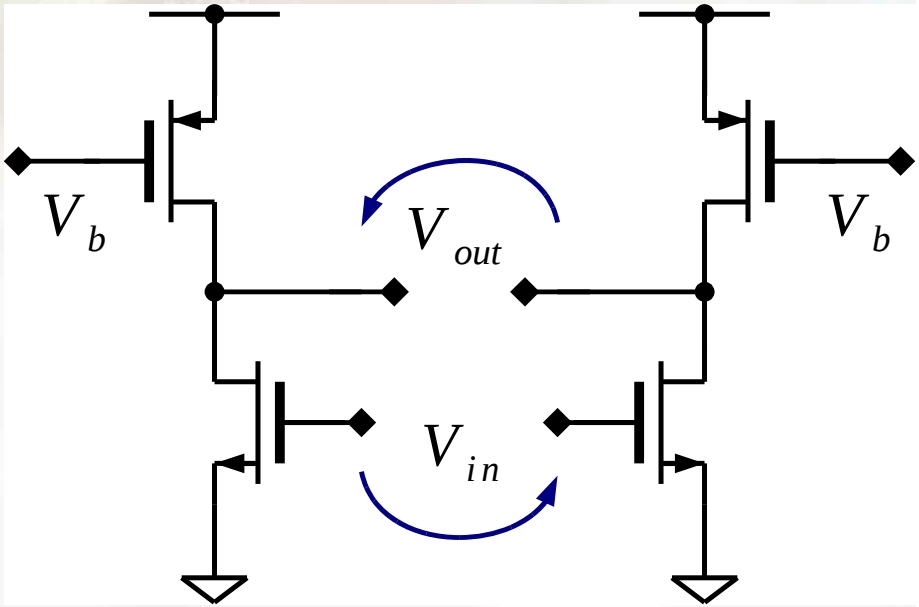
Design targets

- Maximize the differential gain
- Minimize the common-mode gain

Differential signals, two CS stages

Common-mode range (CMR)

Common-mode levels for which the transistors operate in saturation



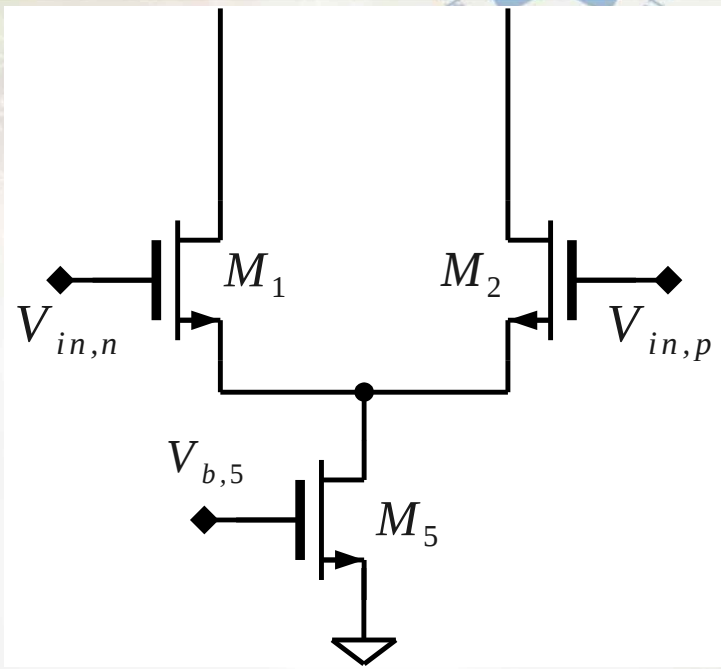
The common-mode rejection is 0 dB!

Effectively there is no rejection!

Differential signals, differential pair

Improved (infinite) CMRR to the cost of CMR

$\Delta I = 4\alpha \cdot V_{eff} \cdot \Delta V$ and $\nabla I = I_0/2$ (!)



Further on

$$I_0 = 2\alpha \cdot \left(V_{eff}^2 + \Delta V^2 \right)$$

combines into

$$\Delta I = 4\alpha \cdot \Delta V \cdot \sqrt{\frac{I_0}{2\alpha} - \Delta V^2} \quad (!)$$

such that

$$\frac{d\Delta I}{d\Delta V} = 4\alpha \cdot \sqrt{\frac{I_0}{2\alpha}} = 4\alpha V_{eff} = \frac{2I_0}{V_{eff}}$$ (ADF) and $\frac{d\nabla I}{d\nabla V} = 0$ (ACM)

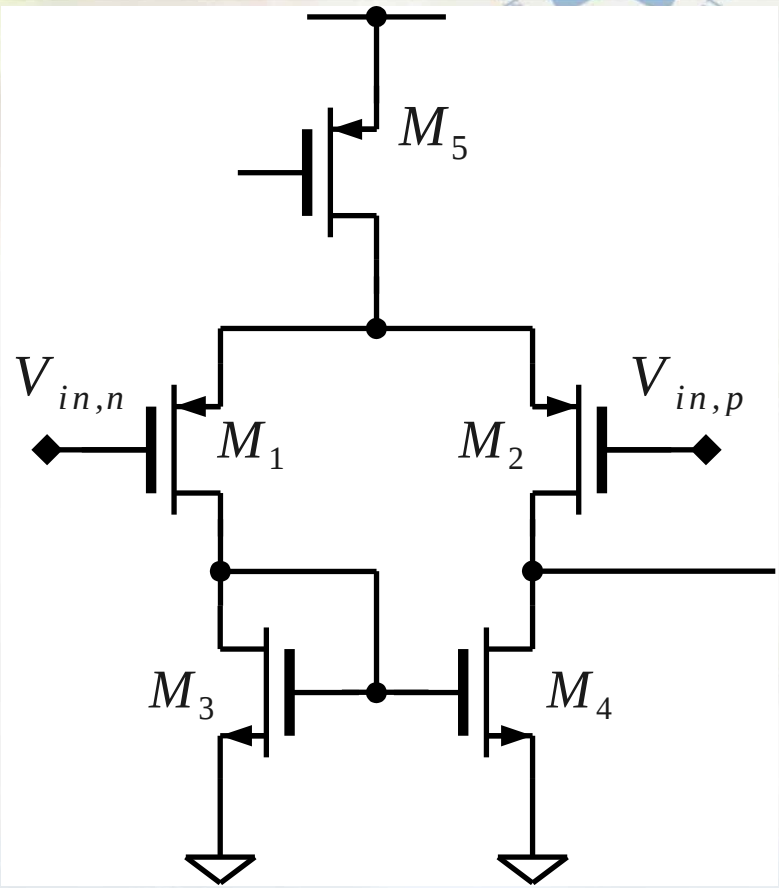
Differential pair with active load

Current-to-voltage conversion

- Resistors
- Current mirror active load
- Current-source active load

Common-mode can be further supressed using a common-mode feedback circuit (CMFB)

- Additional feedback amplifier sensing the common-mode level at the output



Operational amplifiers

Operational transconductance amplifier (OTA)

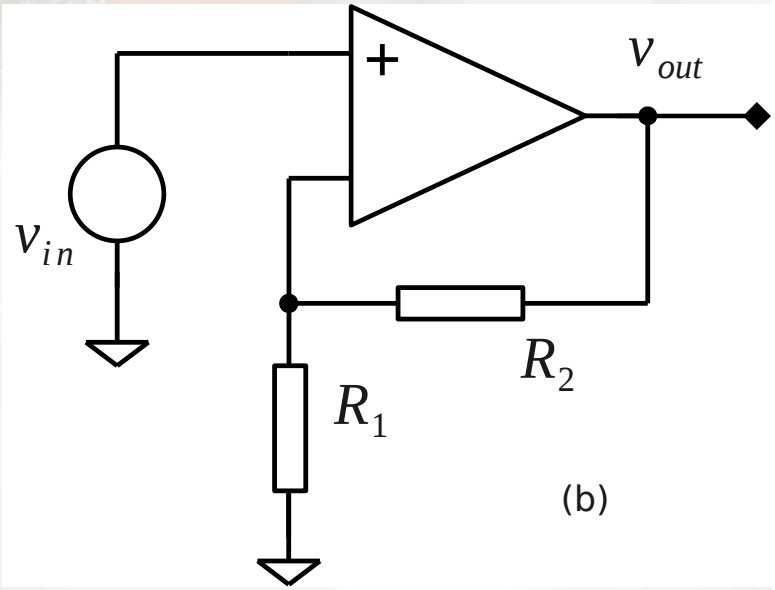
- Drive capacitive load, typically on-chip

Operational amplifiers (OP)

- Drive resistive load, typically off-chip

Specifications

- Differential input, opt. differential output
- Infinite gain
- Infinite input impedance
- Infinite (OTA) / Zero (OP) output impedance



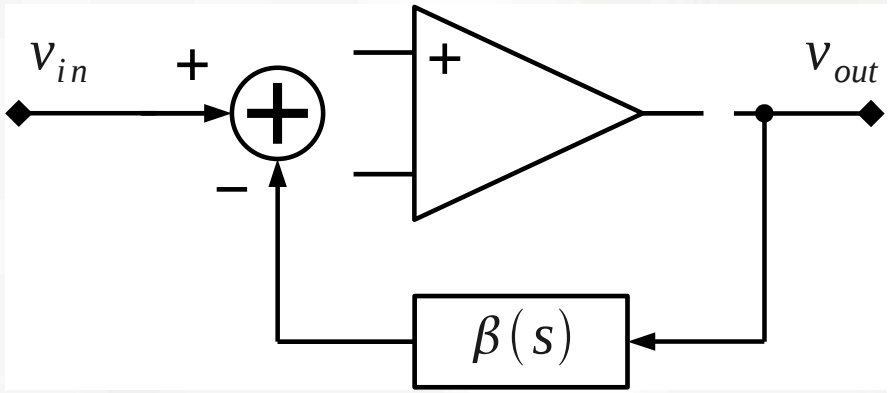
Always used in feedback (otherwise it is a comparator)!

Why do you want controlled feedback?

Gain is now under control!

No variation with gm / gds, instead given by (normally) high-accuracy components

"Unlimited" drive capability



Isolation of input and output

Linearization

Remember, it is a regulation loop. It is designed to track the changes, anything added in the loop will be supressed.

Telescopic OTA

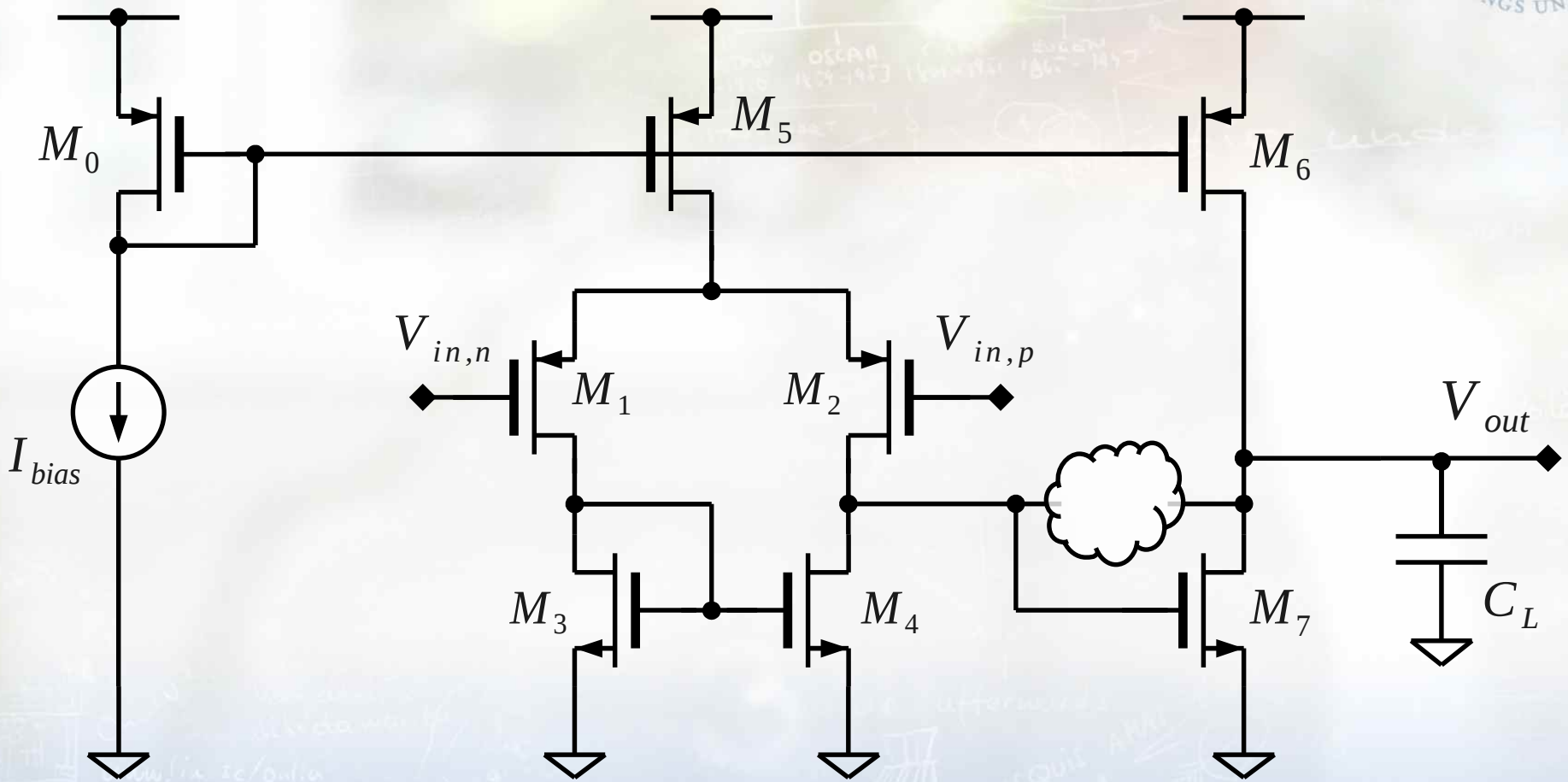
Stack many cascodes on top of each-other and use gain-boosting

etc.

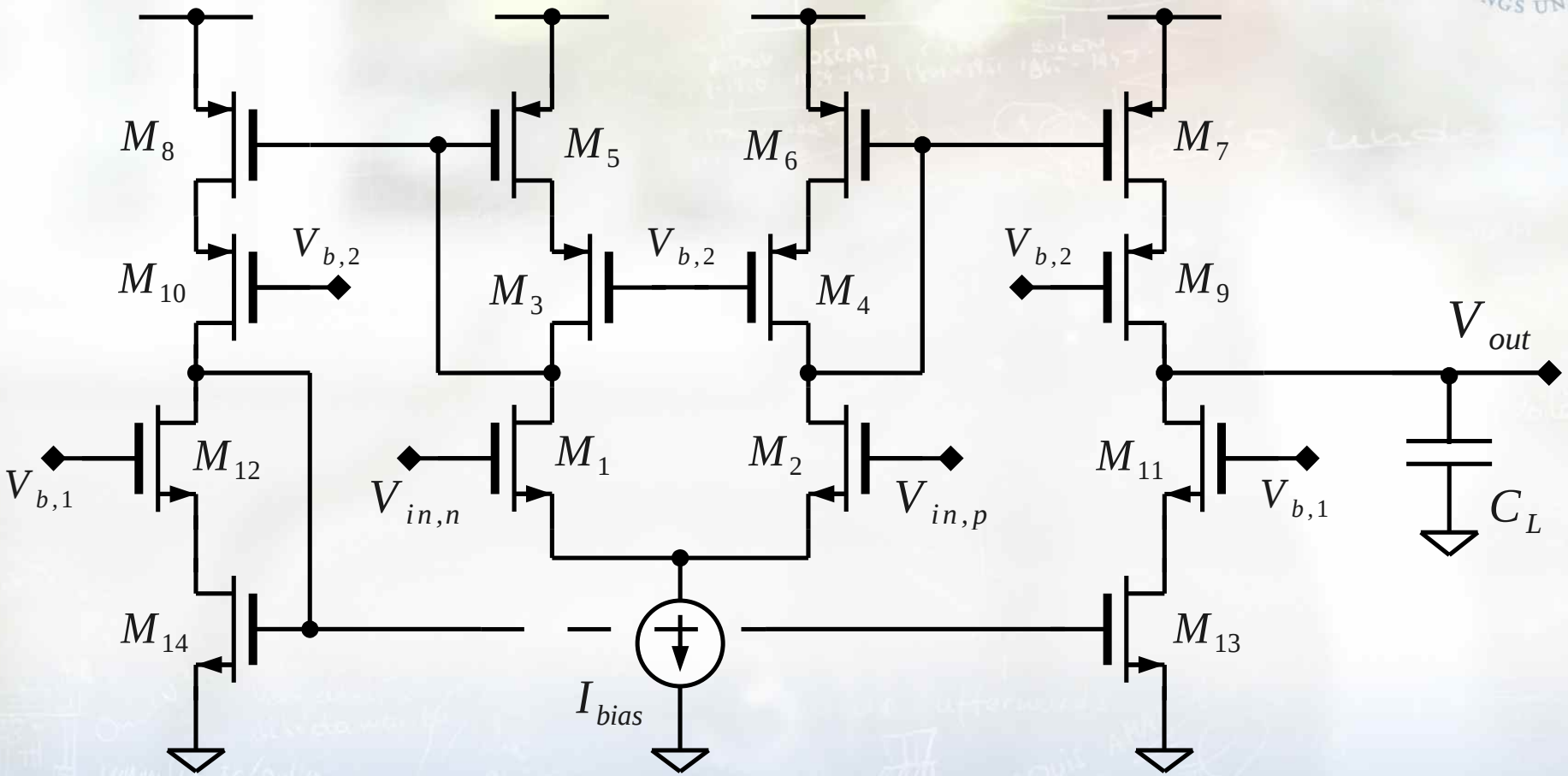
Deliberately omitted, since it is not applicable for modern processes.

Swing is eaten up.

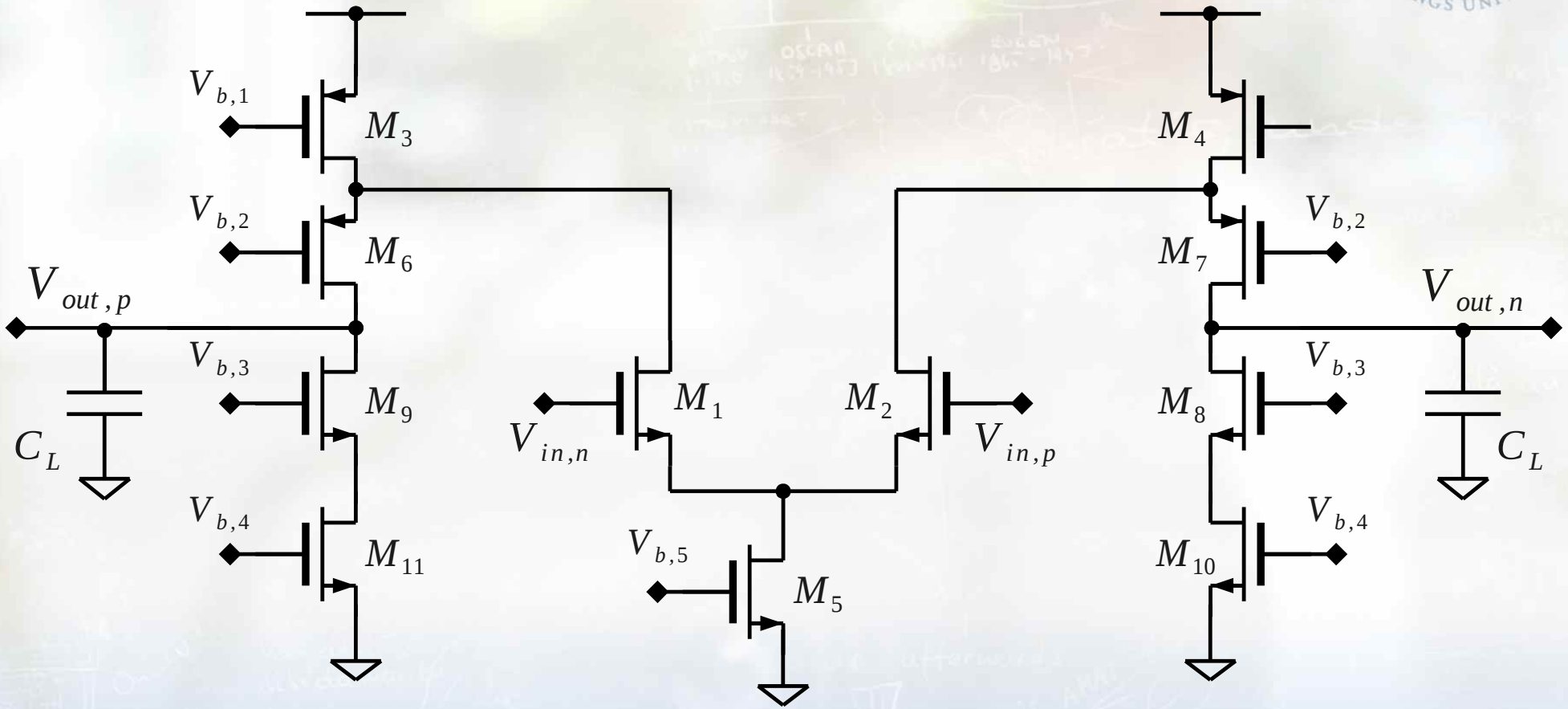
Two-stage OP/OTA



Current-mirror OP/OTA



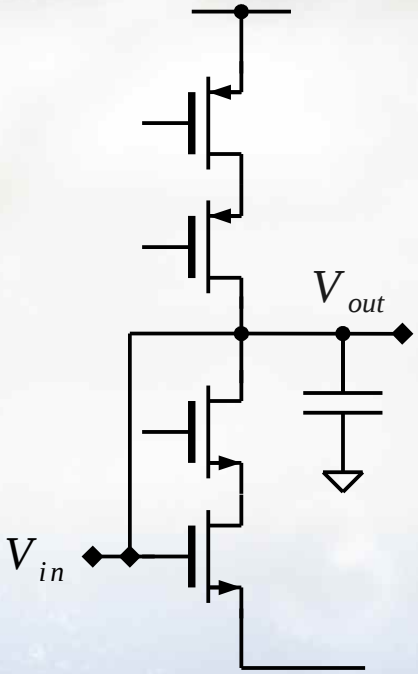
Folded-cascode OP/OTA

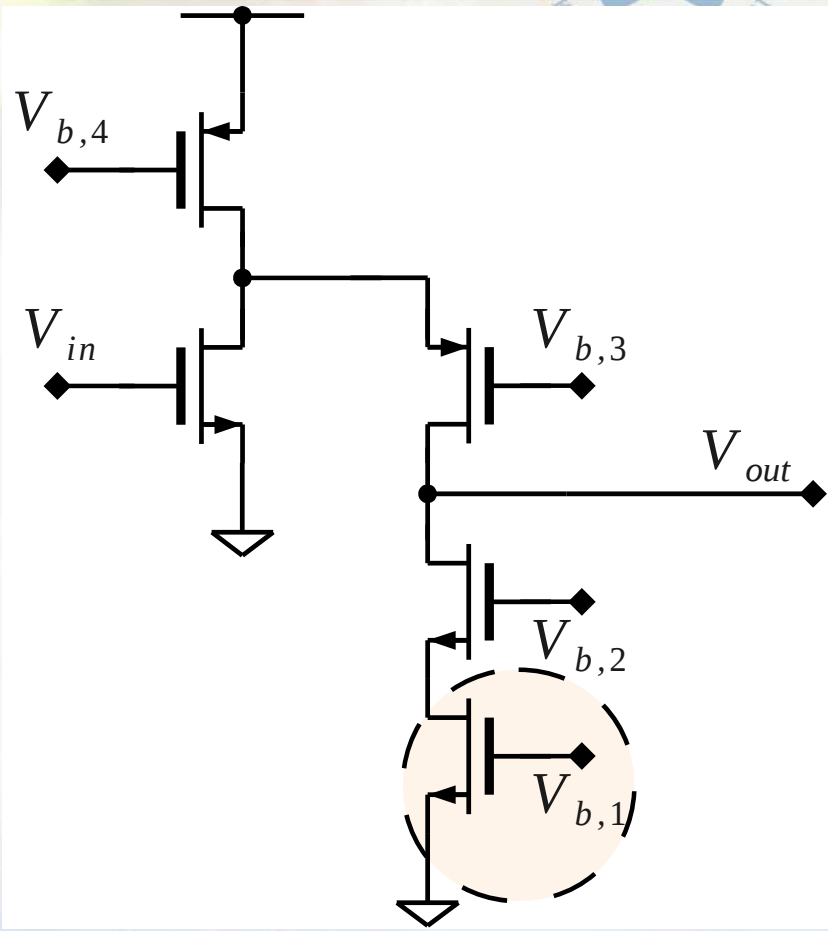


Why folded-cascode?

Consider the CMR in buffer configuration

In telescopic OTA, the swing will be very small since bias transistor "locks" the voltage level





OP/OTA Compilation

Laboratory on the design of a current-mirror OP/OTA

Much better to understand with hands-on experience and play-around with simulator

Cookbook recipes

Hand-outs with step-by-step explanation of the design of OP/OTAs

http://www.es.isy.liu.se/courses/ANIK/download/opampRef/ANTIK_0NNN_LN_opampHandsouts_A.pdf

Compensation techniques

http://www.es.isy.liu.se/courses/ANIK/download/opampRef/ANTIK_0NNN_LN_opampCompensationTable_A.pdf

OP/OTA Compilation, cont'd

Important things to think about

- Systematic offset in two-stage amplifiers
- In a non-cascoded current-mirror OTA, the K factor scaling does not help.

Power-supply rejection, PSRR

$$\mathrm{PSRR} = \min\left(\frac{A_{df}}{A_{vdd}}, \frac{A_{df}}{A_{vss}}\right)$$

- Measured from both positive and negative supply (small-signal exercise)

Many mismatch analyses must be done

- In order to see true offset (see above)
- PSRR and CMRR heavily dependent on the balance in your system

Noise

Any circuit has noise and you as a designer have to reduce it or minimize the impact of it.

> "A disturbance, especially a random and persistent disturbance, that obscures or reduces the clarity of a signal."

Consequences

- We need to use stochastic variables and power spectral densities, expectation values, etc.
- We need to make certain assumptions (models) of our noise sources in order to calculate

Superfunction and spectral densitites

Spectral density (PSD)

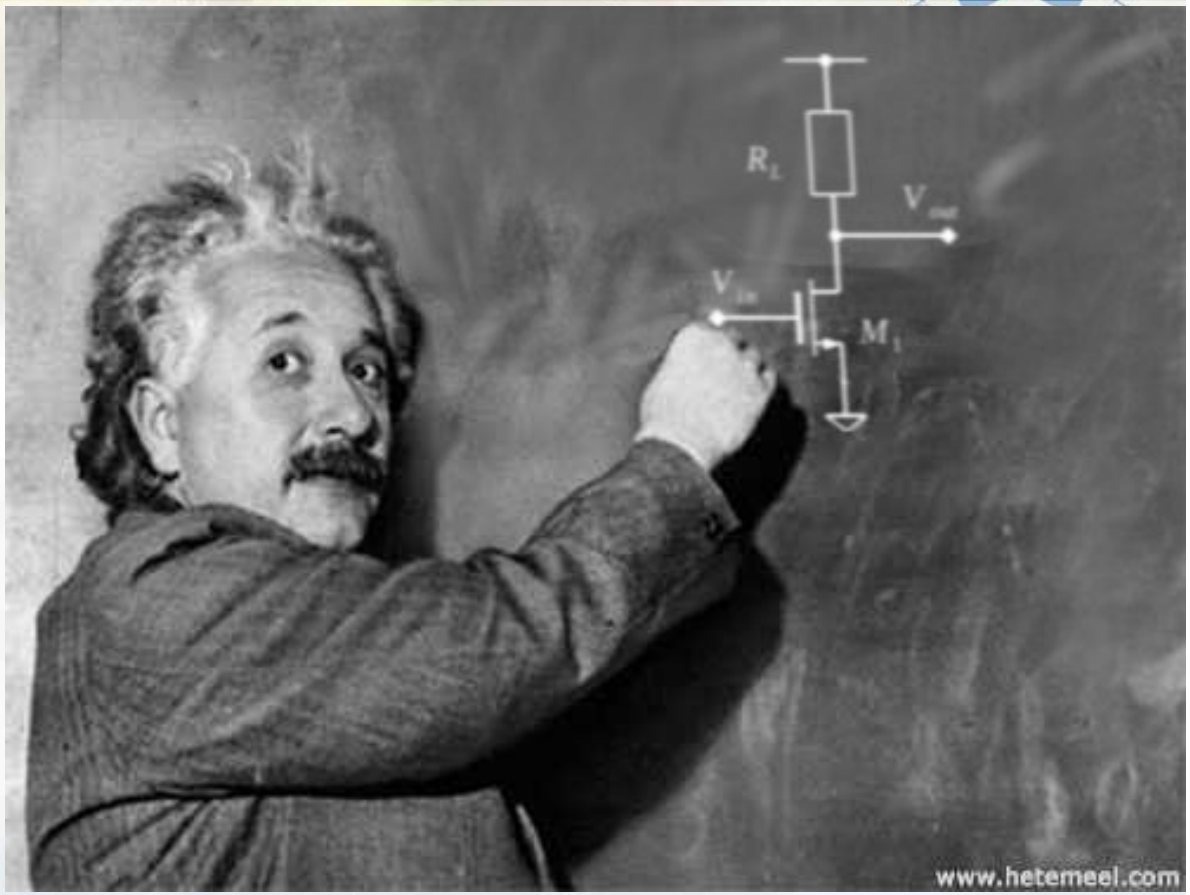
Superfunction

$$S_0(f)=\sum |A_i(f)|^2 \cdot S_i(f)$$

Total noise

$$V_{tot}^2=\int v_n^2(f)\,df$$

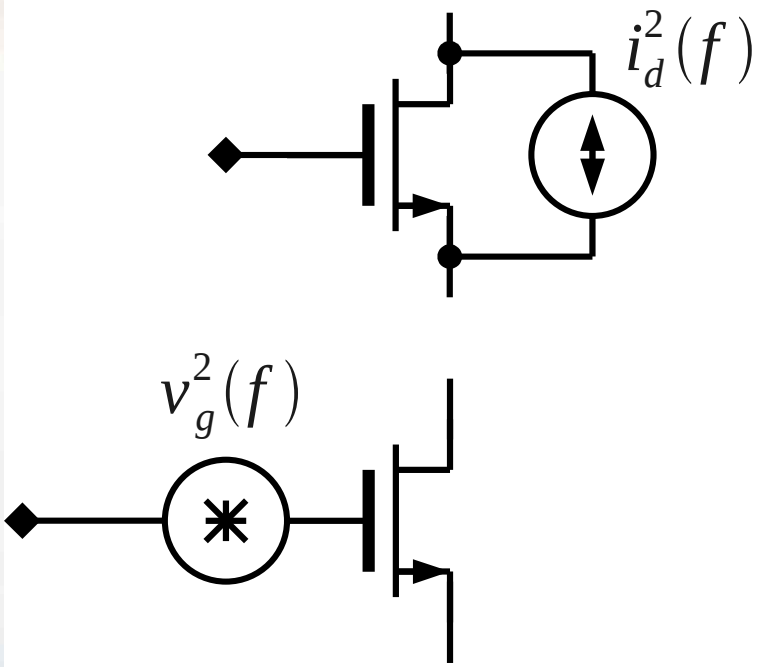
$$V_{tot}^2=v_n^2(0)\cdot\frac{p_1}{4}$$



Thermal noise, white noise

Resistor

$$v_n^2 = 4kTR \quad \text{or} \quad i_n^2 = \frac{v_n^2}{R^2} = \frac{4kT}{R}$$



Transistor

$$v_g^2 = \frac{4kT\gamma}{g_m} \quad \text{or} \quad i_d^2 = v_g^2 \cdot g_m^2 = 4kT\gamma g_m$$

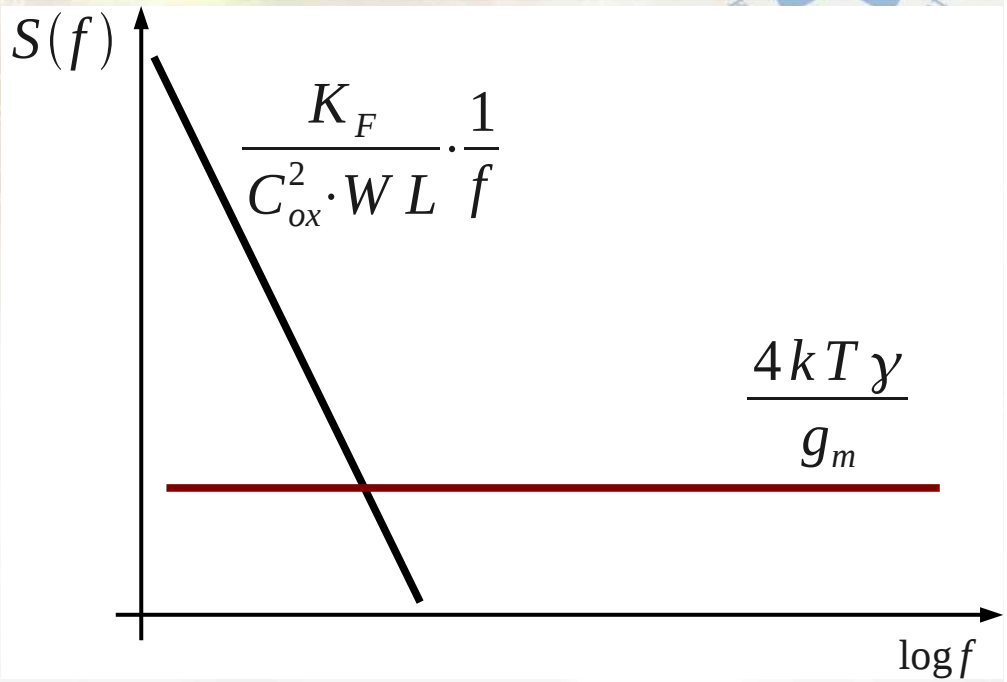
Flicker noise, 1/f-noise, pink noise

Resistor

$$v_n^2 = \frac{v_{bias}^2 \cdot k}{W\,L \cdot f} \quad \text{and} \quad i_n^2 = R^2 \cdot v_n^2$$

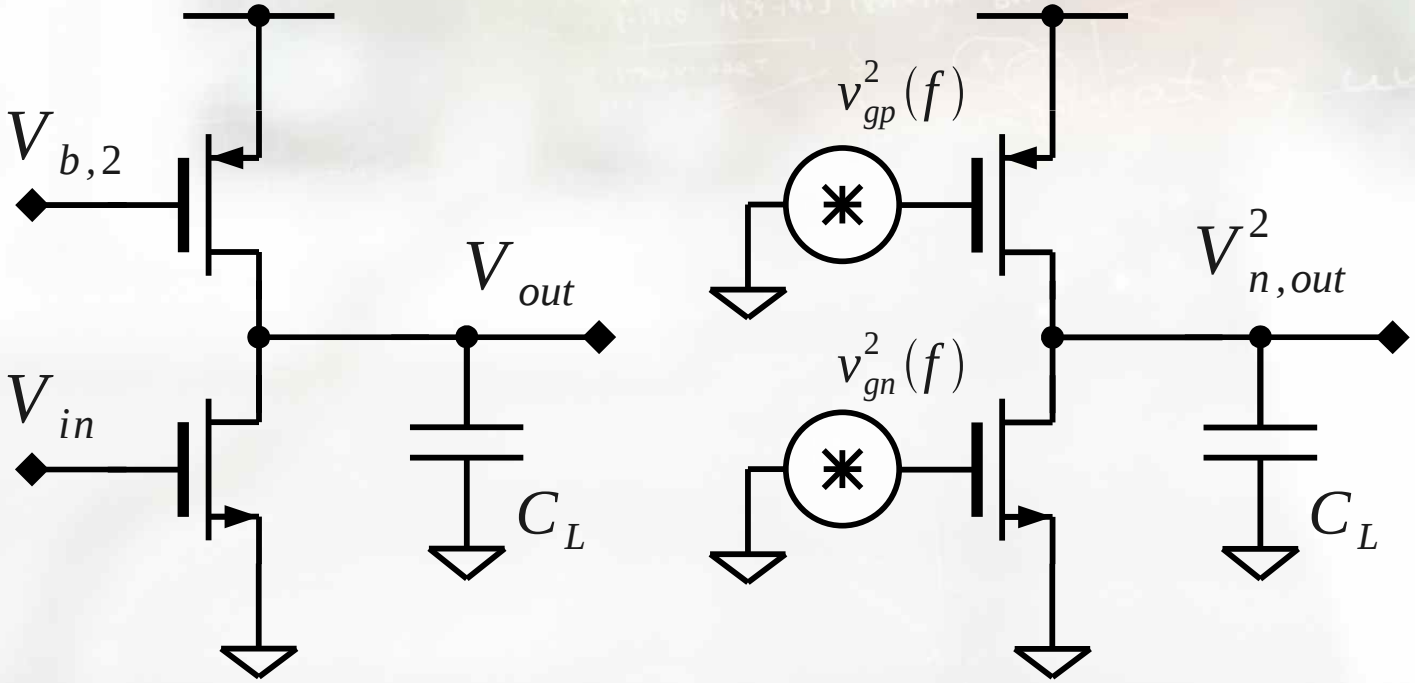
Transistor

$$v_g^2 = \frac{K_F}{C_{ox}^2 \cdot W\,L} \cdot \frac{1}{f} \quad \text{and} \quad i_d^2 = g_m^2 \cdot v_n^2$$



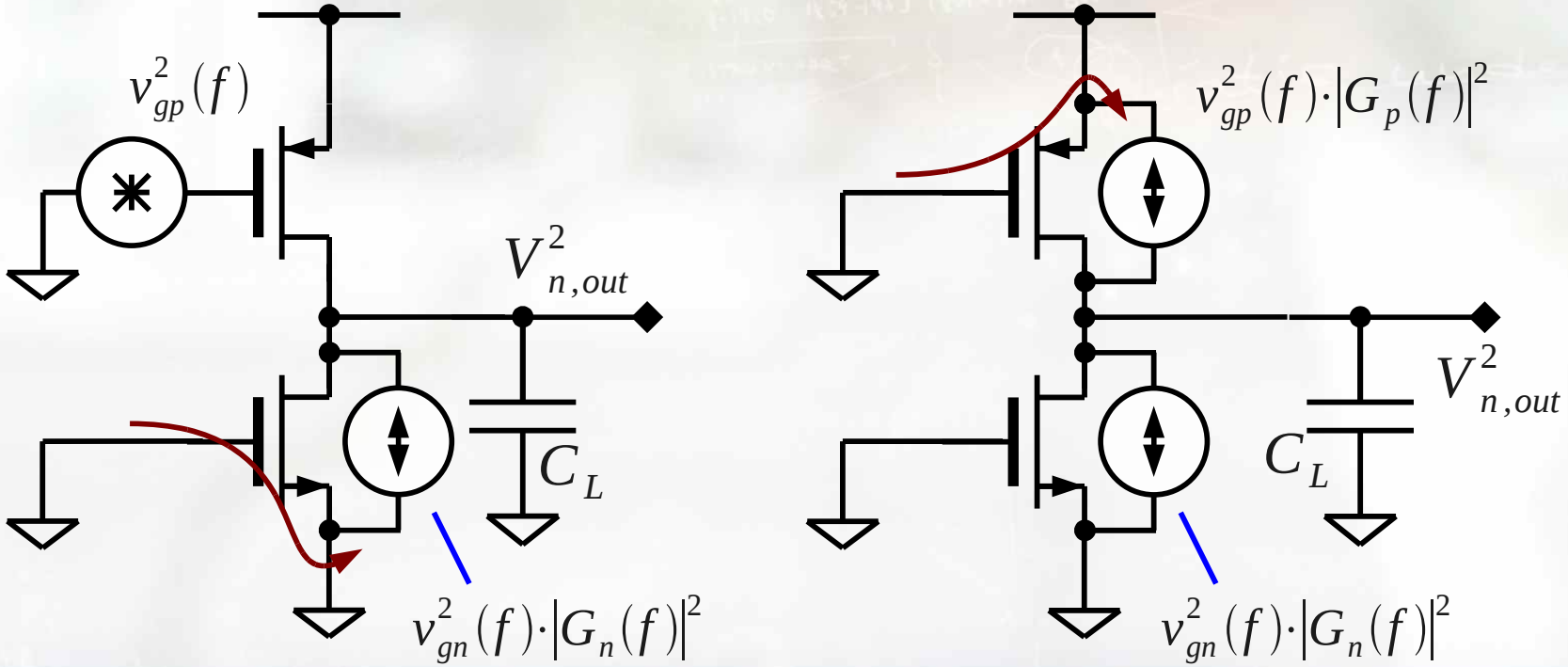
Noise compiled in one example

Common-source with noisy transistors



Noise compiled in one example, cont'd

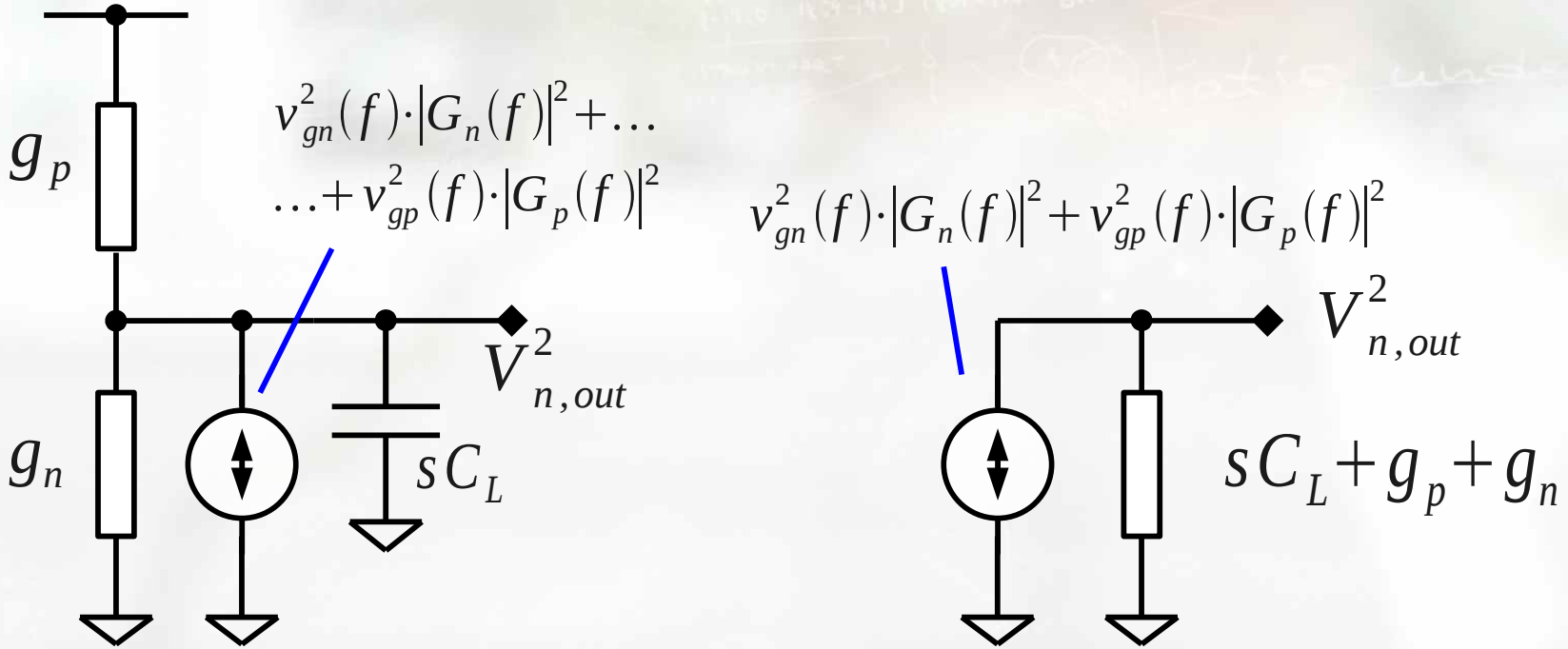
Potentially reorder the sources for convient calculations



Notice the use of transconductance from voltage to current.

Noise compiled in one example, cont'd

Equivalent small-signal schematics (ESSS)



Noise compiled in one example, cont'd

The general transfer function to the output is given by

$$V_{n,out}^2(f) = \frac{v_{gn}^2(f)\cdot\left|G_n(f)\right|^2 + v_{gp}^2(f)\cdot\left|G_p(f)\right|^2}{\left|s\,C_L + g_p + g_n\right|^2}$$

Insert the values

$$V_{n,out}^2(f) = 4kT\gamma\,\frac{\dfrac{g_{mn}^2}{g_{mn}} + \dfrac{g_{mp}^2}{g_{mp}}}{(g_p+g_n)^2\cdot\left|1+\dfrac{\dfrac{s}{g_p+g_n}}{C_L}\right|} = 4kT\gamma\,\frac{\dfrac{g_{mn}+g_{mp}}{(g_p+g_n)^2}}{\left|1+\dfrac{\dfrac{s}{g_p+g_n}}{C_L}\right|^2}$$

Noise compiled in one example, cont'd

Use the brickwall approach

$$V_{n,tot}^2 = \int V_{n,out}^2(f) = V_{n,out}^2(0) \cdot \frac{p_1}{4}$$

Insert the expressions

$$V_{n,tot}^2 = 4kT\gamma \frac{g_{mn}+g_{mp}}{(g_p+g_n)^2} \cdot \frac{g_p+g_n}{4C_L} = \frac{kT\gamma}{C_L} \cdot \frac{g_{mn}+g_{mp}}{g_p+g_n}$$

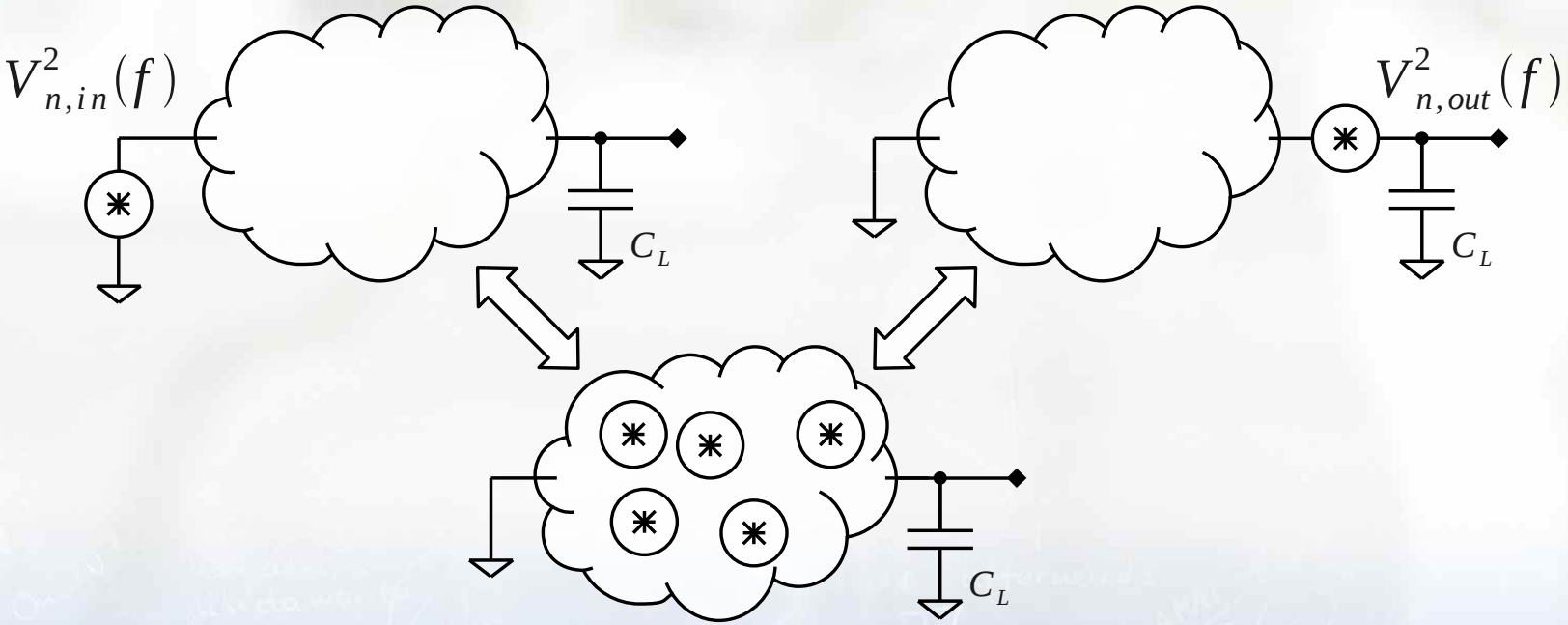
and conclude

$$V_{n,tot}^2 = \frac{kT\gamma}{C_L} \cdot A_0 \cdot \left(1 + \frac{g_{mp}}{g_{mn}}\right)$$

Input-referred noise

Revert the output noise back to the input:

$$V_{n,in}^2(f) = \frac{V_{n,out}^2(f)}{|A_{in}(f)|^2}$$



The common-source example

Input-referred noise

$$V_{n,in}^2(f) = \left[4kT\gamma \frac{\frac{(g_{mn}+g_{mp})}{(g_p+g_n)^2}}{\left| 1+\frac{\frac{s}{(g_p+g_n)}}{C_L} \right|^2} \right] \cdot \left[\frac{\left| 1+\frac{\frac{s}{(g_p+g_n)}}{C_L} \right|^2}{\frac{g_{mn}^2}{(g_p+g_n)^2}} \right] = \frac{4kT\gamma}{g_{mn}} \cdot \left(1+\frac{g_{mp}}{g_{mn}} \right)$$

What does this mean?

Bias transistor should be made with low transconductance!

- Visible from the formula

Gain transistors should be made with high transconductance!

- Visible from the formula

Gain should be distributed between multiple stages, c.f., Friis.!

- Left as an exercise

What did we do today?

Differential circuits

- Why differential?
- CMRR, CMR

Operational amplifiers

- More on how we design them
- Cookbook recipes
- PSRR

Circuit noise

- Thermal and flicker noise
- Noise bandwidth

What will we do next time?

Switched capacitor circuits

- The basics
- Charge-redistribution analysis

Nonidealties

- SC parasitics