Lecture 10, ATIK

Data converters 3

LiU EXPANDING REALITY

What did we do last time?

A quick glance at sigma-delta modulators

- Understanding how the noise is shaped to higher frequencies

DACs

- A case study of the current-steering DAC architecture.
- Suggesting some common implementation and architectural details
- Impact of impedance
- Impact of mismatch
- Some extras needed

What will we do today?

Case-study pipelined ADC

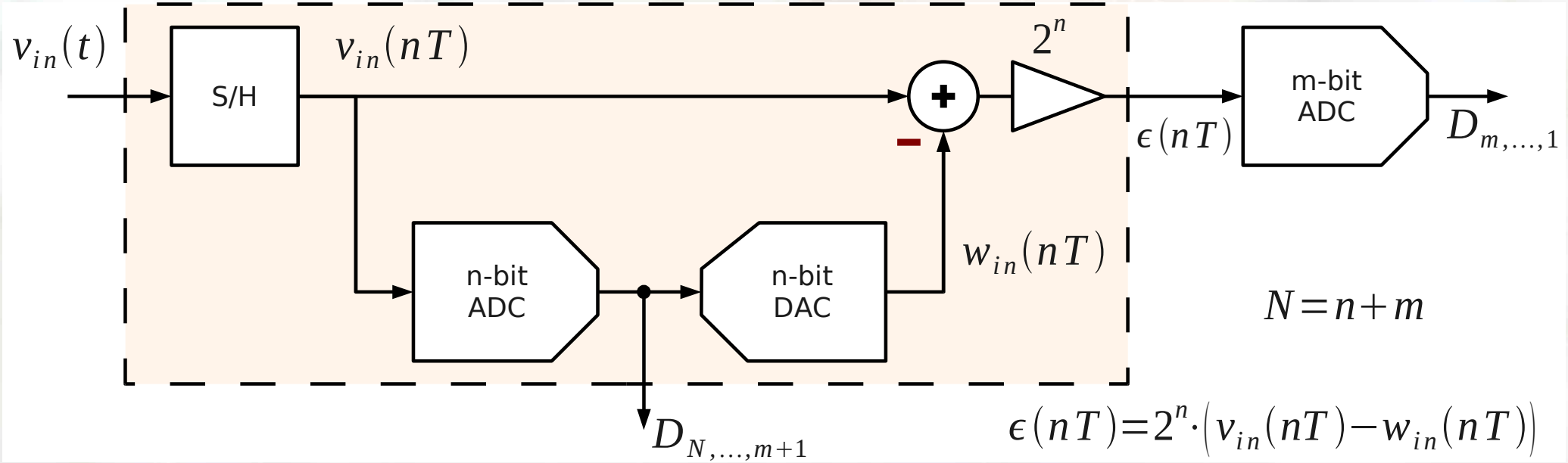
- Architecture and a general overview
- Error correction techniques
- Sample-and-hold design
- Comparator design

Wrap-up

First - the subranging ADC - Basic operation

The converter "zooms" a range and converts the residue.

If flash is used as subconverter, there is only 2^n+2^m comparators



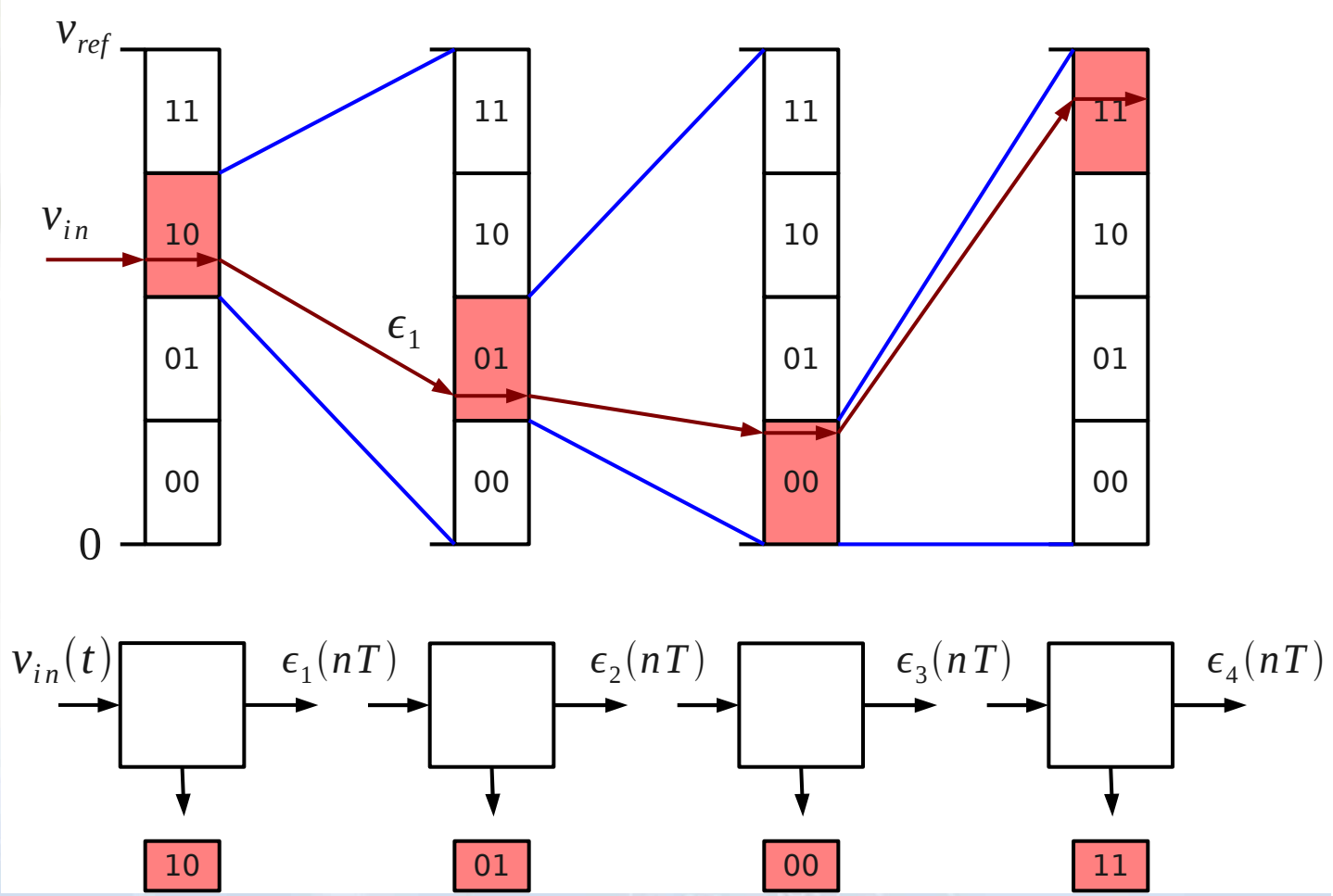
Another analog adder is required as well as a gain circuit, which limits the speed.

Pipelined ADC in one picture

Multiple subranging ADC in series

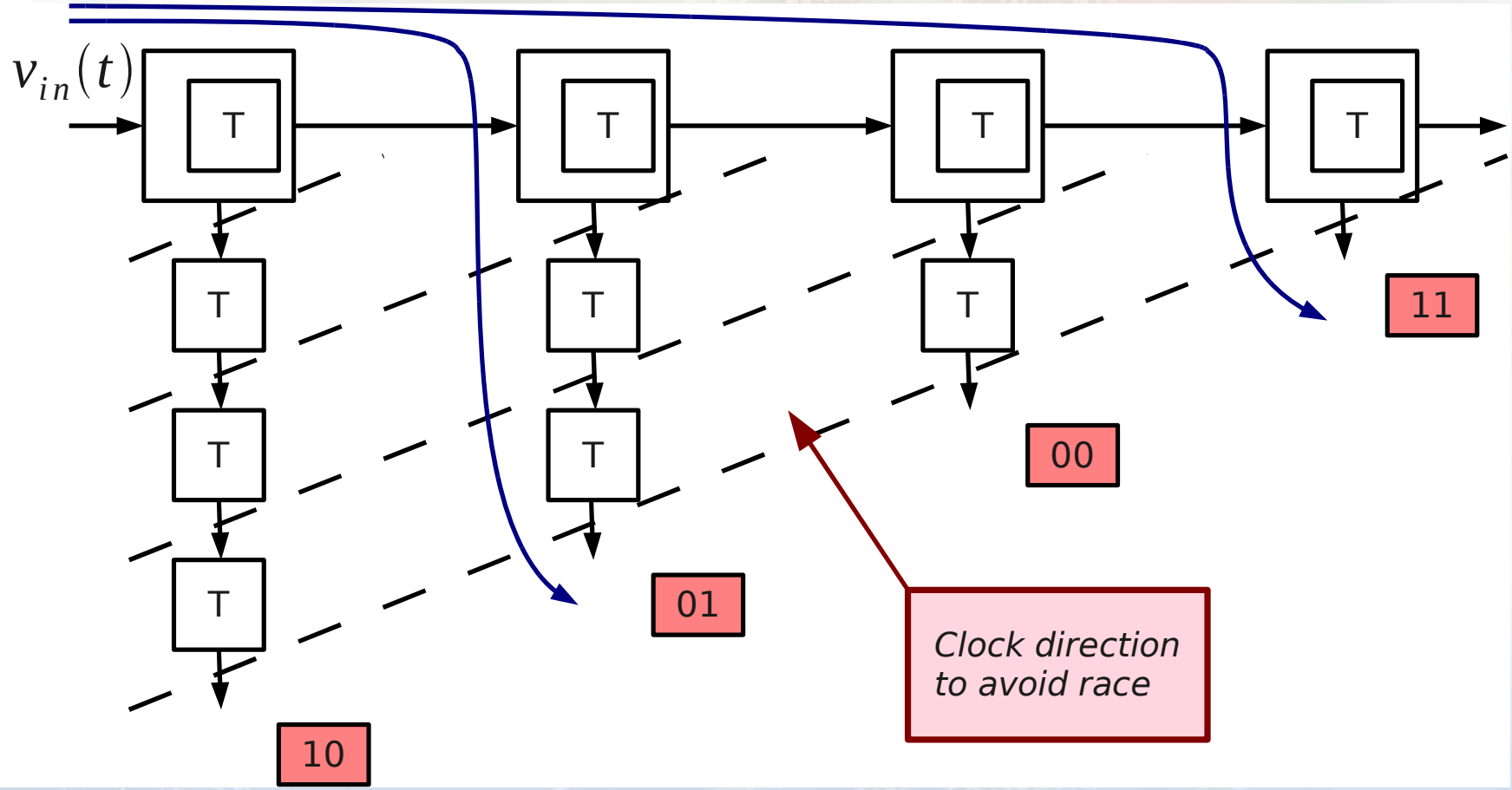
A series of refinements, zoom-ins, of the convertible range

Assume same range in each stage



Pipelined ADC - delays

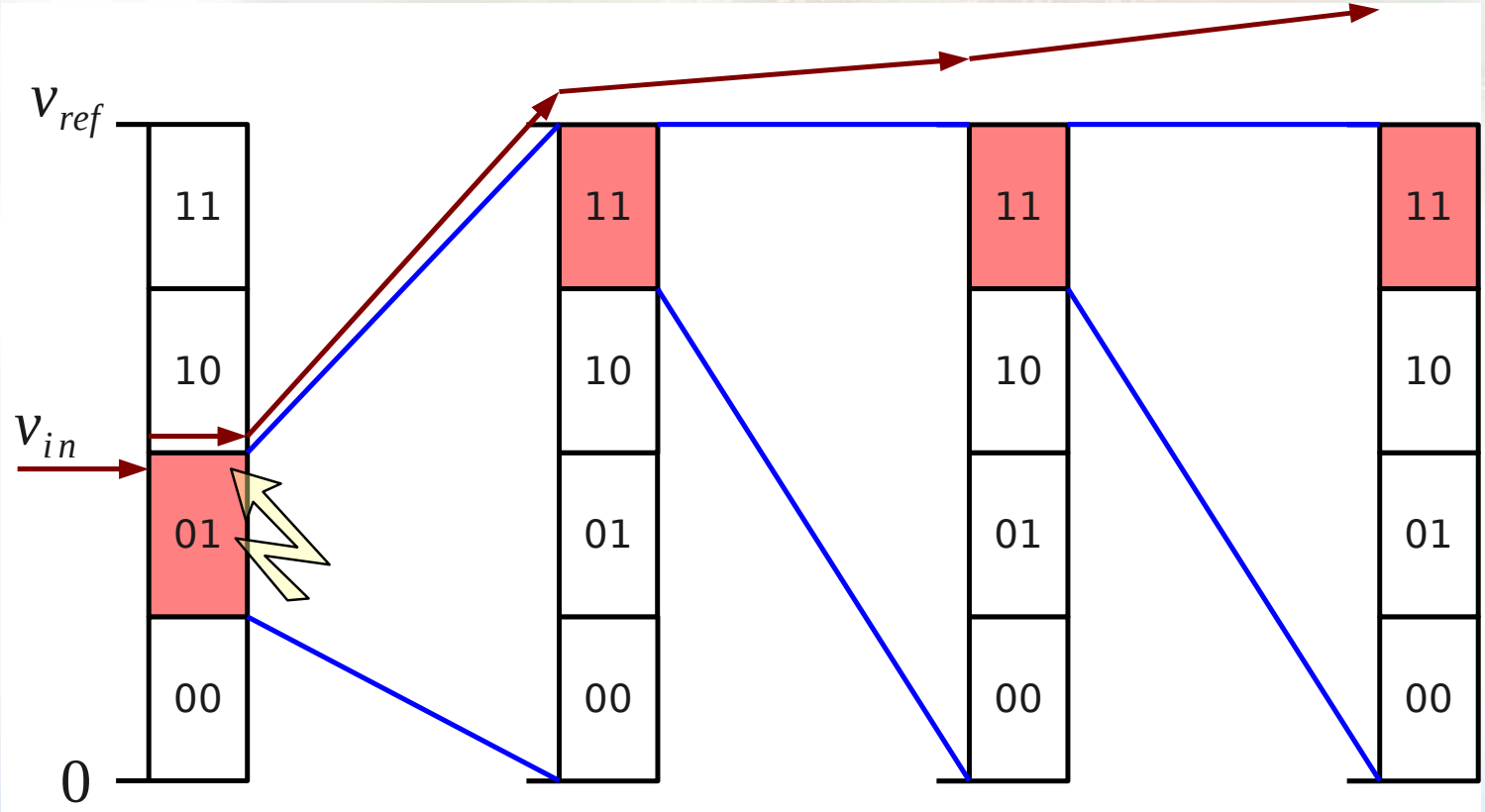
Balance the delays and "cleverly" distribute the clock to avoid race



A pipelined ADC will have longer latency

Pipelined ADC - sensitive towards errors

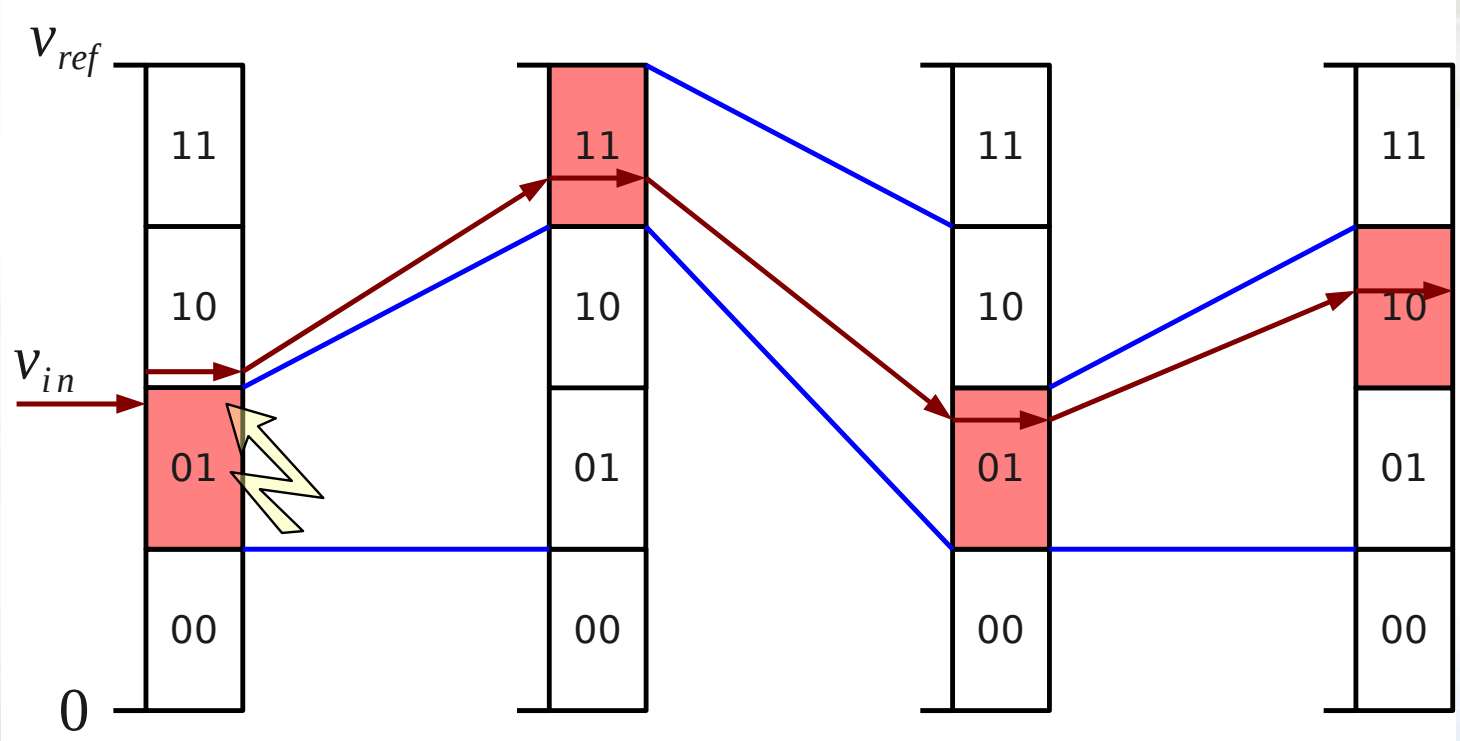
Any misinterpreted level quickly diverges and never recovers!



Overlap can be digitally corrected (without training!)

Pipelined ADC - error correction

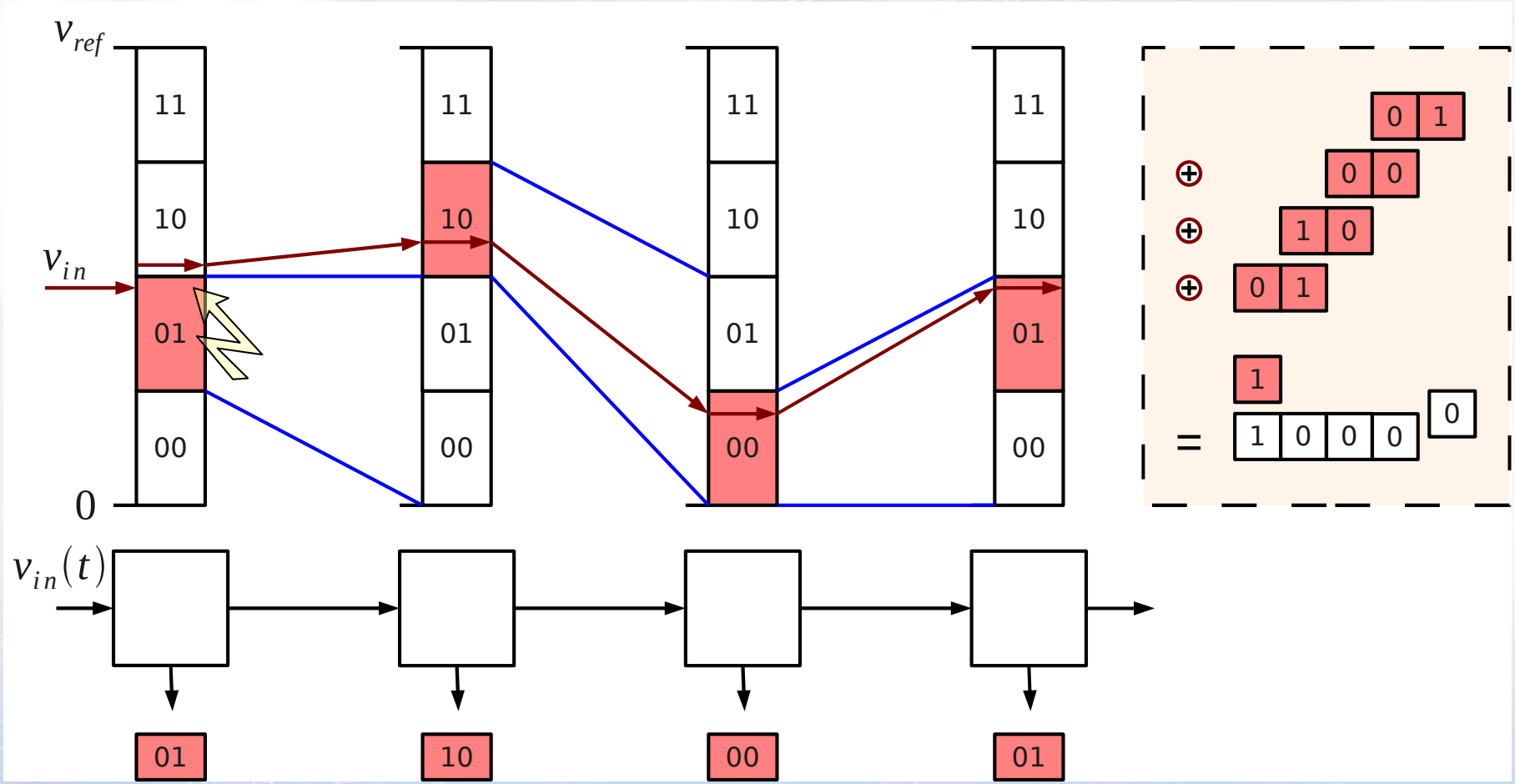
Increase the number of stages and reduce overlap, i.e., decrease the scaling factor, 2^n. Now, less likely to diverge and is able to recover.



More stages are required, but typically worth it

Pipelined ADC - error correction cont'd

Trivial circuitry to retrieve the most likely code!



PADC: Taking a look at the subcomponents

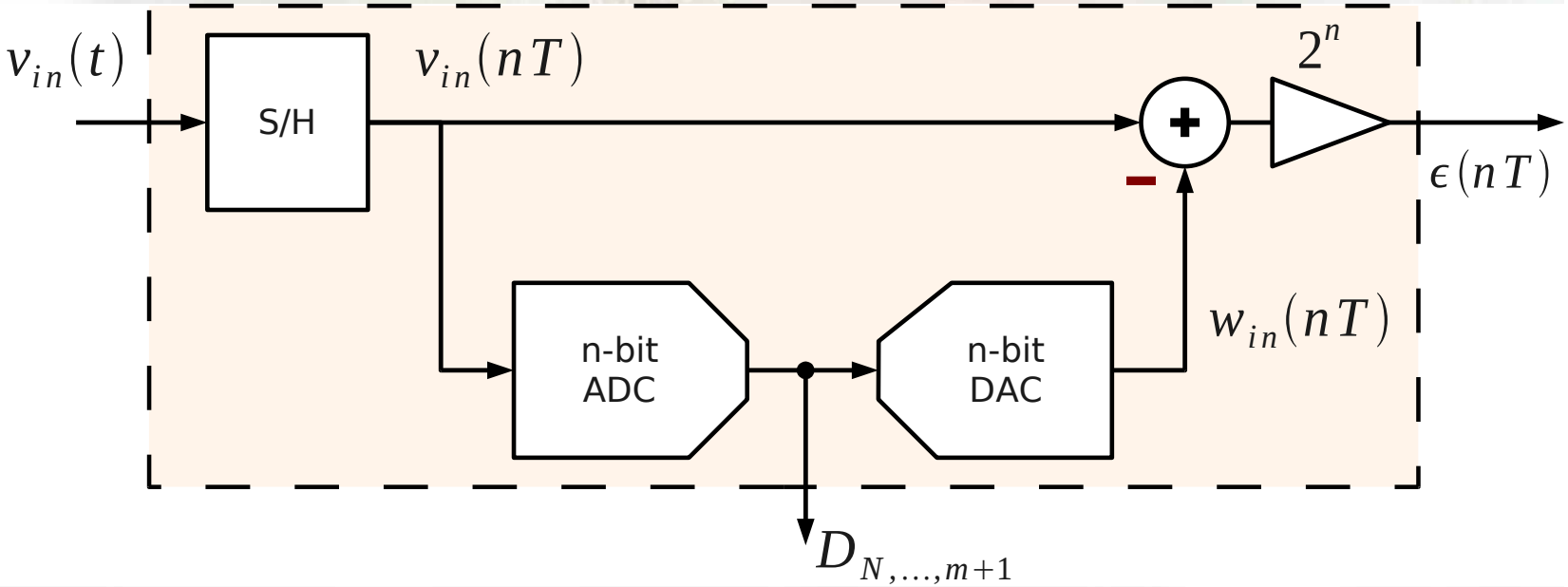
Sample-and-hold

Sub-ADC

Sub-DAC

Adder

Multiplier

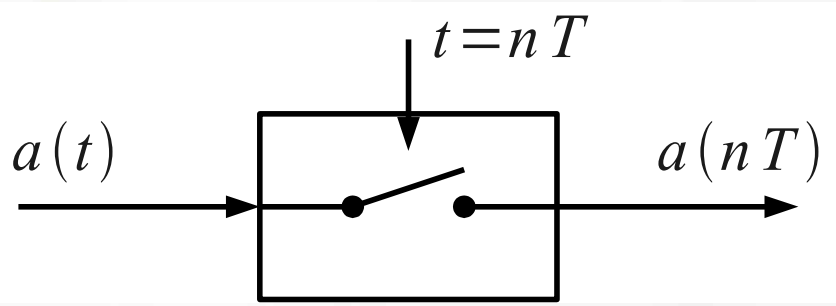


Sample-and-hold process

The input should be sampled and held to reduce the jitter in the subcomponents.

Inherent delays will otherwise cause mismatch.

Jitter (interdelay) is a very strong limitation on obtainable performance



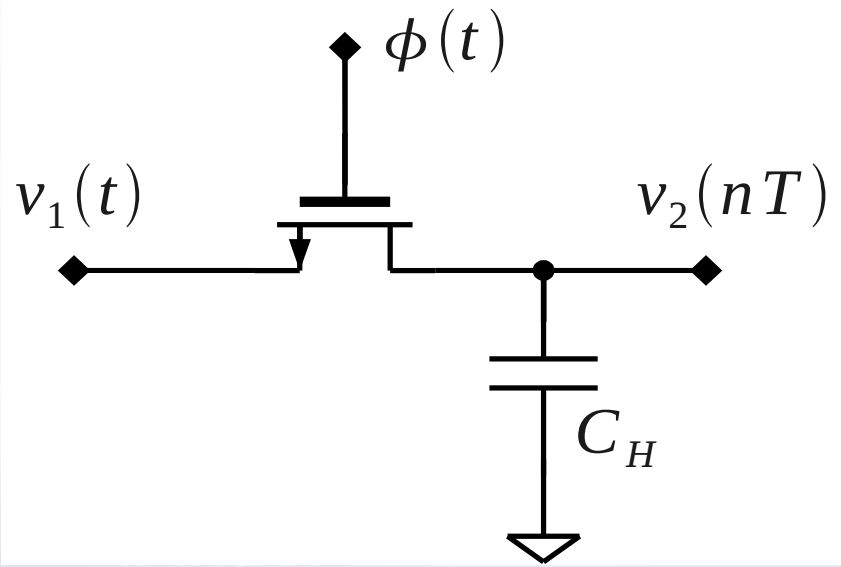
S/H at input of ADC must have full accuracy !!!

Sample-and-hold, 1st-level implementation

Passive sampling

Limitations

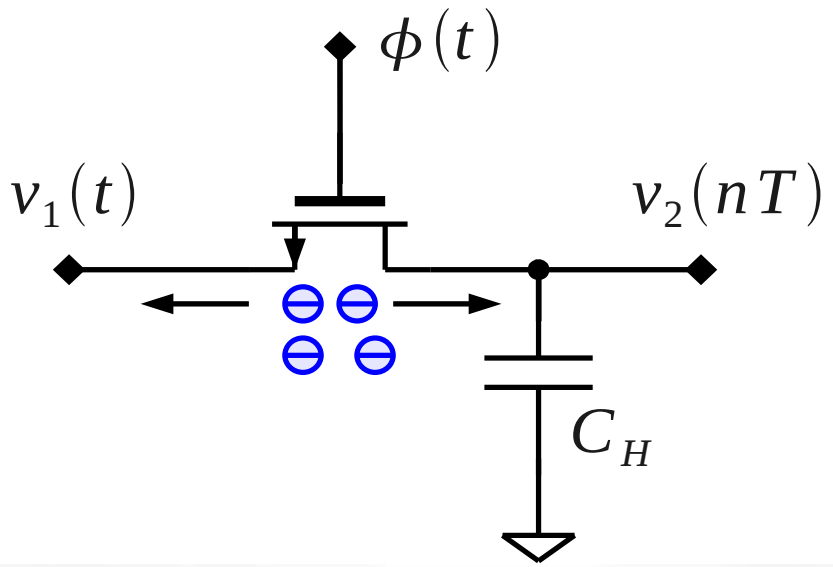
- Clock-feedthrough
- Charge-injection
- On-resistance
- Distortion
- Jitter
- Noise



Sample-and-hold charge injection

Channel charge injection

$$\Delta V_2(nT) \sim \frac{W\,L \cdot C_{ox} \cdot \left(V_\phi - V_T - V_2(nT)\right)}{C_H}$$



Large capacitor is good!

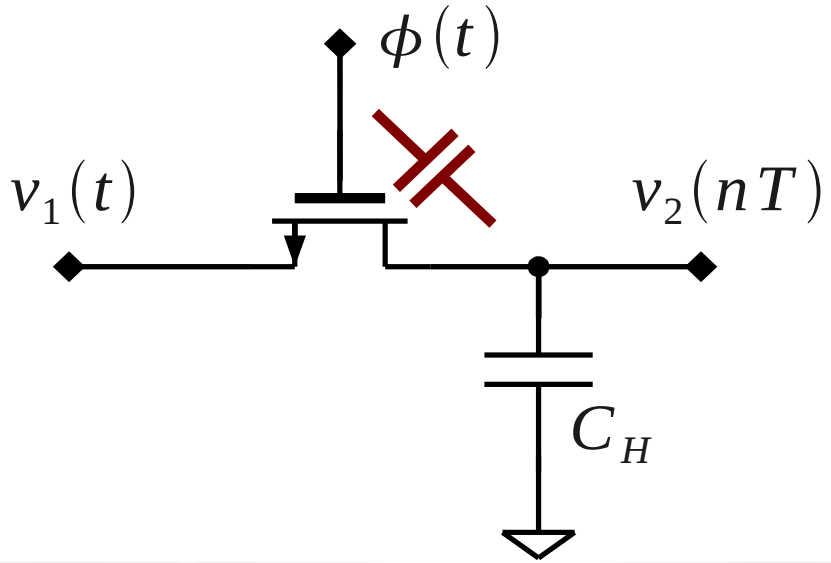
Force the delta voltage to always be lower than the LSB voltage:

$$V_{ref} \cdot \frac{W \cdot L \cdot C_{ox}}{2\,C_H} < \frac{\Delta}{2} \Rightarrow W \cdot L < \frac{C_H}{C_{ox} \cdot 2^{N+1}}$$

Sample-and-hold clock feedthrough

Clock feed-through

$$\Delta V_2(nT) = \frac{C_{ol}}{C_H} \cdot \left(V_\phi - V_2(nT) \right)$$



such that

$$V_2(nT) = V_1(nT) \cdot \left(1 + \frac{C_{ol}}{C_H} \right) - \frac{C_{ol}}{C_H} \cdot V_T$$

Large capacitor is good!

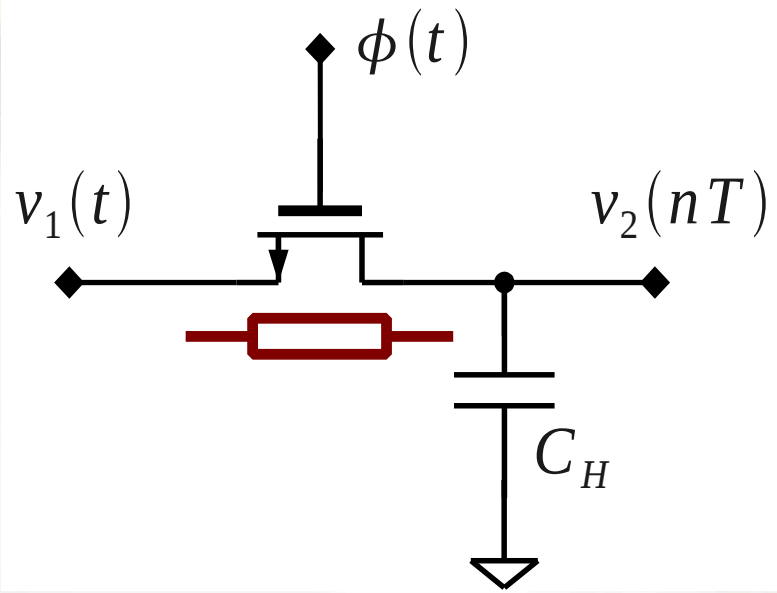
Force the delta voltage to always be lower than the LSB voltage:

$$V_{ref} \cdot \frac{C_{ol}}{C_H} < \frac{\Delta}{2} \Rightarrow C_{ol} < \frac{C_H}{2^{N+1}}$$

Sample-and-hold bandwidth

Non-zero resistance

$$G_{on} = \alpha \cdot \left(V_{phi} - V_T - V_1(nT) \right)$$



Bandwidth limitation, but also distortion due to signal-dependent resistance

Large capacitor is bad!

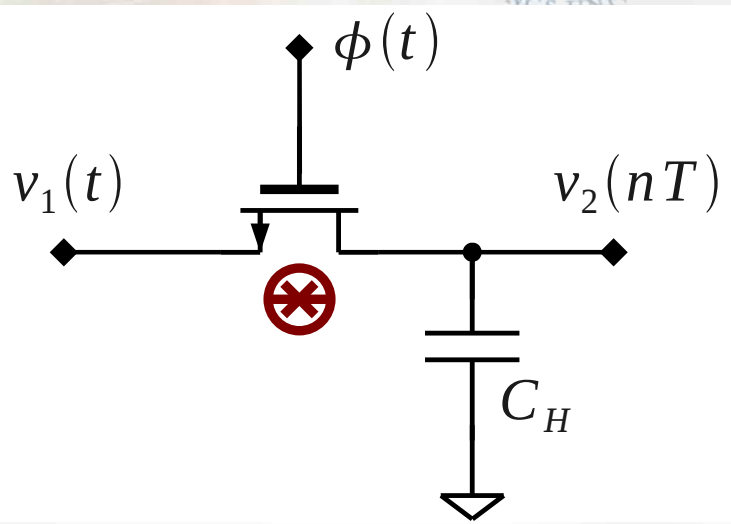
For a full-scale step at the input, we should settle within 1 LSB accuracy, i.e.

$$V_{ref} \cdot e^{\frac{-G_{on}}{2C_H \cdot f_s}} < \frac{\Delta}{2} \Rightarrow -\frac{G_{on}}{2C_H \cdot f_s} < -\ln 2^{N+1} \Rightarrow R_{on} \ll \frac{0.5 \cdot \ln 2}{C_H \cdot f_s \cdot (N+1)}$$

Noise

Given by the bandwidth and the brickwall pole

$$v_{n,tot}^2 = \frac{kT}{C_H}$$



Large capacitor is good!

Quantization noise should be larger than noise, i.e.

$$v_{n,tot}^2 < \frac{\Delta^2}{12} \Rightarrow C_H > 12\,kT \cdot \frac{2^{2N}}{V_{ref}^2}$$

Sub-ADC

Most likely a flash ADC

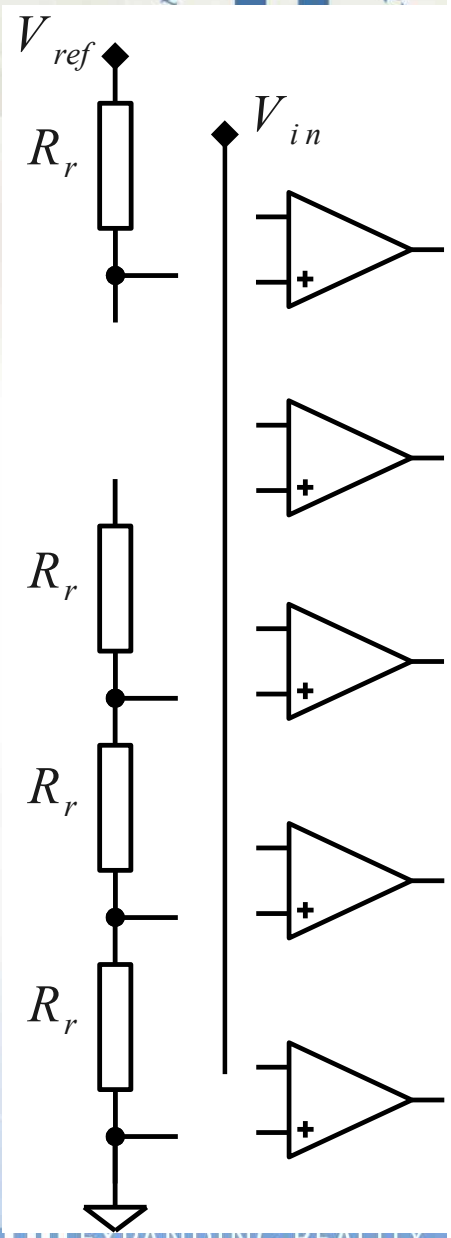
- Fastest and best choice for low number of bits

Use a resistive divider to create reference voltages

Offset and matching of resistors must match the accuracy of the active pipeline stage

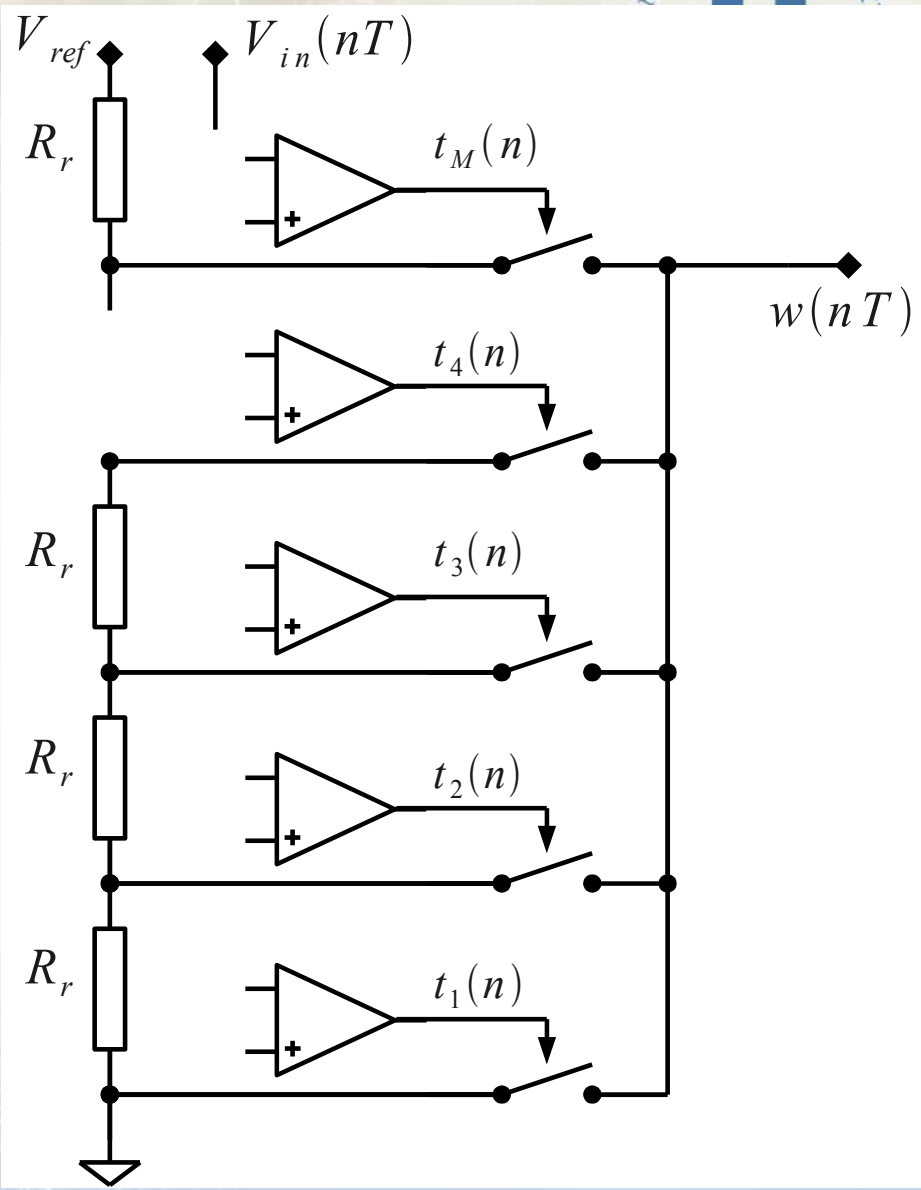
- Mismatch information will give requirements on transistors and resistor sizes

- Relative error is inversely dependent on the area



Sub-DAC

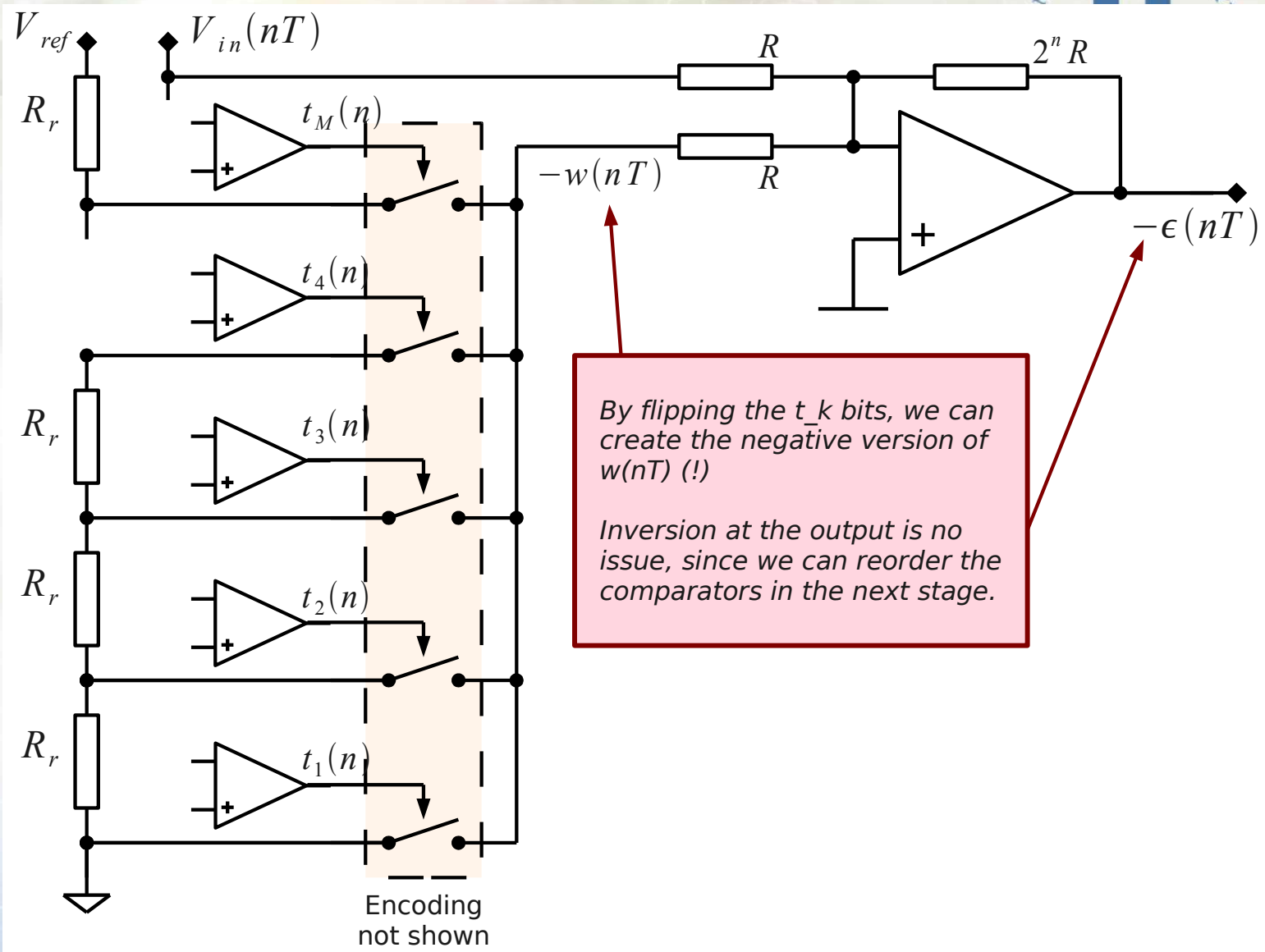
Reuse the resistive divider for the sub DAC!



Notice that the picture does not display the correct decoding of the t_i bits for control of the DAC switches. (A thermometer-to-walking-one converter consisting of a bank of XOR gates is needed.)

Adder/gain

A rather compact design can be obtained reusing and combining difference active and passive components.



Resistance is futile...

Why?

Noise and OTA design

Go for capacitor-based circuits

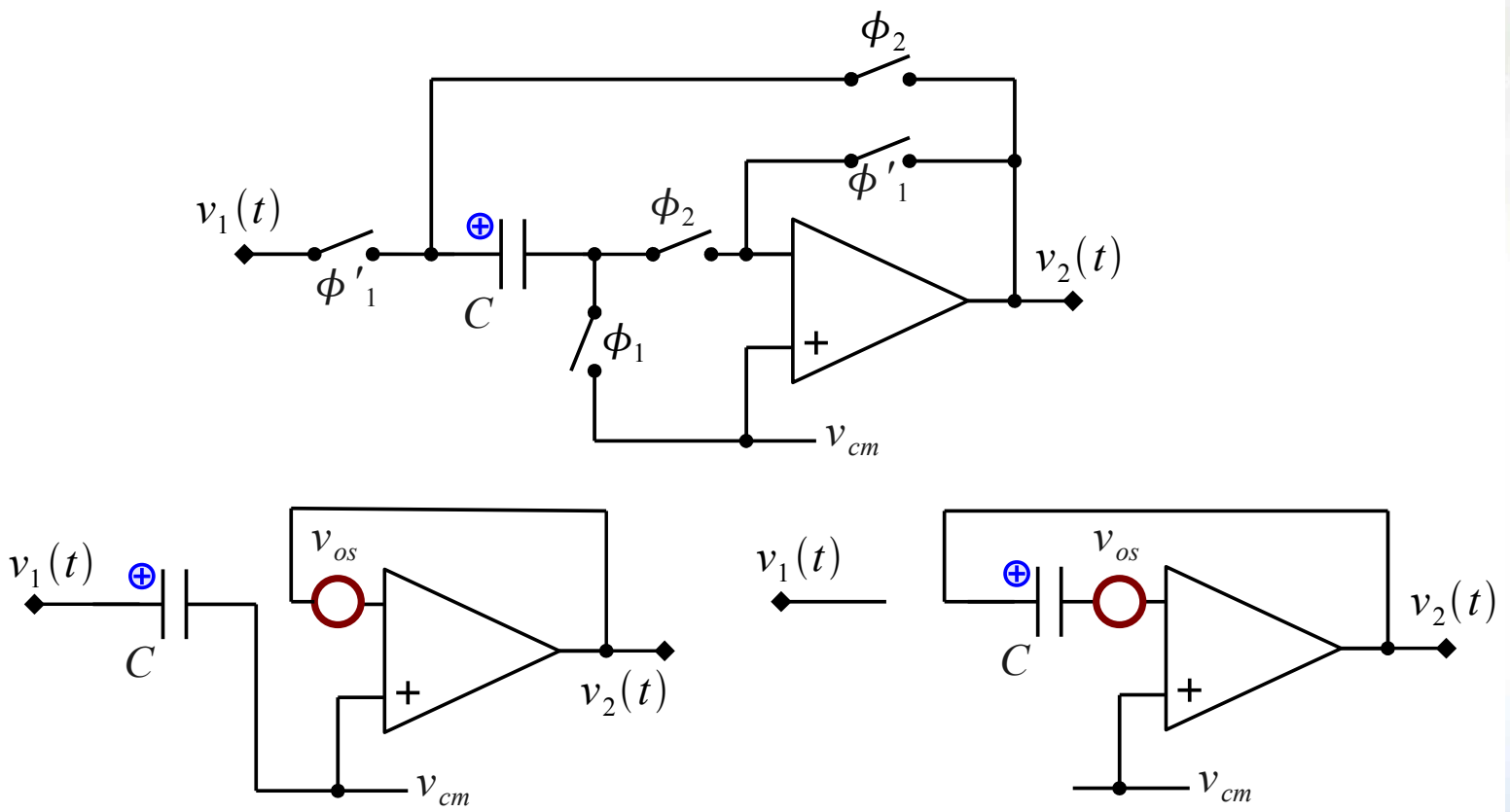
Switched-capacitor comparators in the sub ADC

Switched-capacitor DAC

Switched-capacitor summation and multiplier

Active S/H with offset cancellation

Uses bottom-plate sampling to minimize charge feedthrough

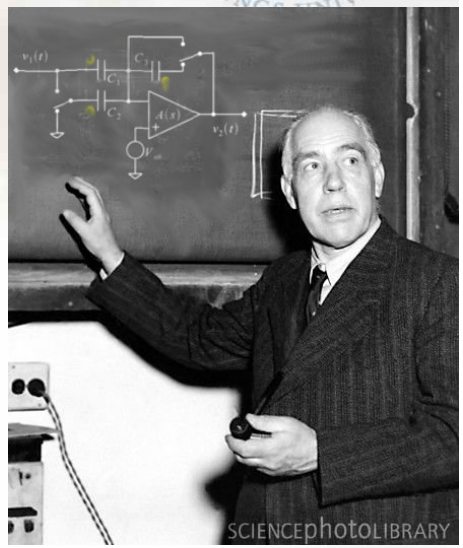


$v_2 = v_1 - v_{os}$, i.e., offset sensitive, but output is buffered and isolated.

Comparators

A comparator is not an OP! Consider speed vs. gain

$$A(s)=\frac{A_0}{1+s/p_1}\Rightarrow\tau=\frac{1}{p_1}\approx\frac{A_0}{\omega_{ug}}$$

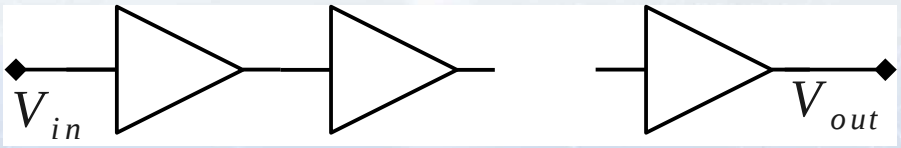


vs three-stage example

$$A'(s)=\frac{A'_0{}^3}{\left(1+s/p'_1\right)^3}\Rightarrow\tau'=3\cdot\frac{1}{p'_1}=\frac{3A'_0}{\omega_{ug}}$$, with $A'_0=A_0^{1/3}$

$$\tau'=\tau\cdot\frac{3A'_0}{A_0}=\tau\cdot\frac{3}{A_0^{2/3}}$$

(Phase margin is not necessarily an issue!)



Comparators, speed vs resolution 1

Characteristic resolution parameter, c_r, is the smallest level that can toggle the output to reliable levels

$$V_{OH}-V_{OL}=A_0\cdot\left(V_{IH}-V_{IL}\right)\Rightarrow c_r=\frac{V_{OH}-V_{OL}}{A_0}$$

Assume a first-order system and apply an input step:

$$v_{out}(t)=V_{OL}+A_0\cdot v_{step}\cdot\left(1-e^{-\omega_c t}\right)$$

Apply the smallest possible signal

$$v_{out}(t)=V_{OL}+A_0\cdot c_r\cdot\left(1-e^{-\omega_c t}\right)=V_{OL}+\left(V_{OH}-V_{OL}\right)\cdot\left(1-e^{-\omega_c t}\right)$$

Check when we pass the mid-level at the output

$$v_{out}(\tau)=V_{OL}+\frac{V_{OH}-V_{OL}}{2}=V_{OL}+\left(V_{OH}-V_{OL}\right)\cdot\left(1-e^{-\omega_c\tau}\right)\Rightarrow 0.5=1-e^{-\omega_c\tau}\Rightarrow\tau=\frac{\ln 2}{\omega_c}$$

Comparators, speed vs resolution 2

Assume now that the input step is K times larger:

$$v_{out}(\tau') = V_{OL} + \frac{V_{OH} - V_{OL}}{2} = V_{OL} + \left(V_{OH} - V_{OL}\right) \cdot K \cdot \left(1 - e^{-\omega_c \tau'}\right) \Rightarrow$$

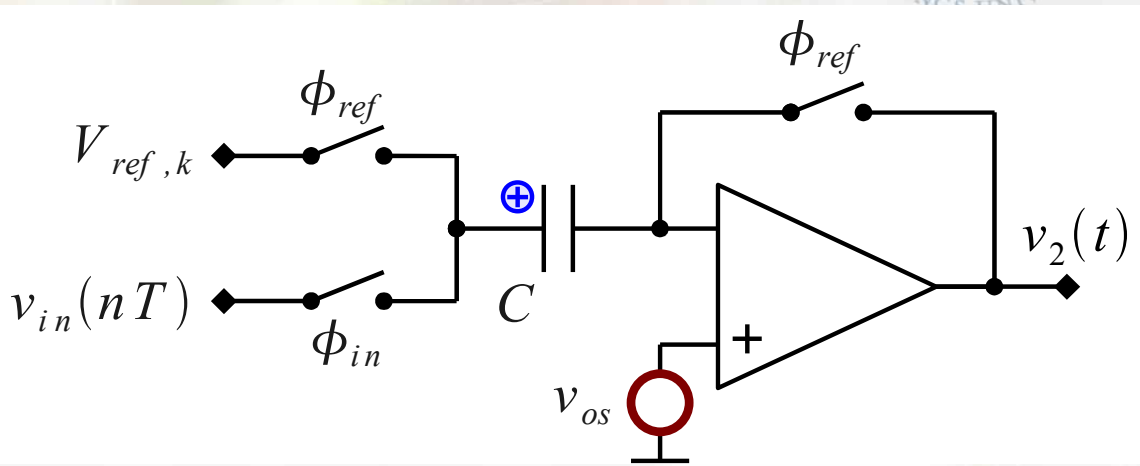
$$0.5 = K \cdot \left(1 - e^{-\omega_c \tau'}\right) \Rightarrow \tau' = \frac{1}{\omega_c} \cdot \ln \frac{2K}{2K-1} \Rightarrow \tau' = \tau \cdot \frac{\ln \frac{2K}{2K-1}}{\ln 2} \approx \frac{\tau}{2K \cdot \ln 2}$$

If K goes towards infinity, the delay goes towards 0.

The more accuracy, the lower sample frequency!

Comparators, offset "cancellation" 1

The sub ADC takes sampled input and reference at two different phases:



First reference is selected

$$q(\phi_{ref}) = C \cdot \left(V_{ref,k} - V_2(\phi_{ref}) \right)$$

where

$$V_2(\phi_{ref}) = v_{os} \cdot \frac{A}{1+A}$$

Then signal is selected and charge must be preserved

$$q(\phi_{in}) = C \cdot \left(v_{in}(\phi_{in}) - v_{os} + \frac{V_2(\phi_{in})}{A} \right) = q(\phi_{ref}) = C \cdot \left(V_{ref,k} - v_{os} \cdot \frac{A}{1+A} \right)$$

$$V_2(\phi_{in}) = -A \cdot \left(v_{in}(\phi_{in}) - V_{ref,k} \right) + v_{os} \cdot \frac{A}{1+A}$$ (no amplified offset)

Comparators, offset cancellation in OTA

Correlated double sampling

First phase

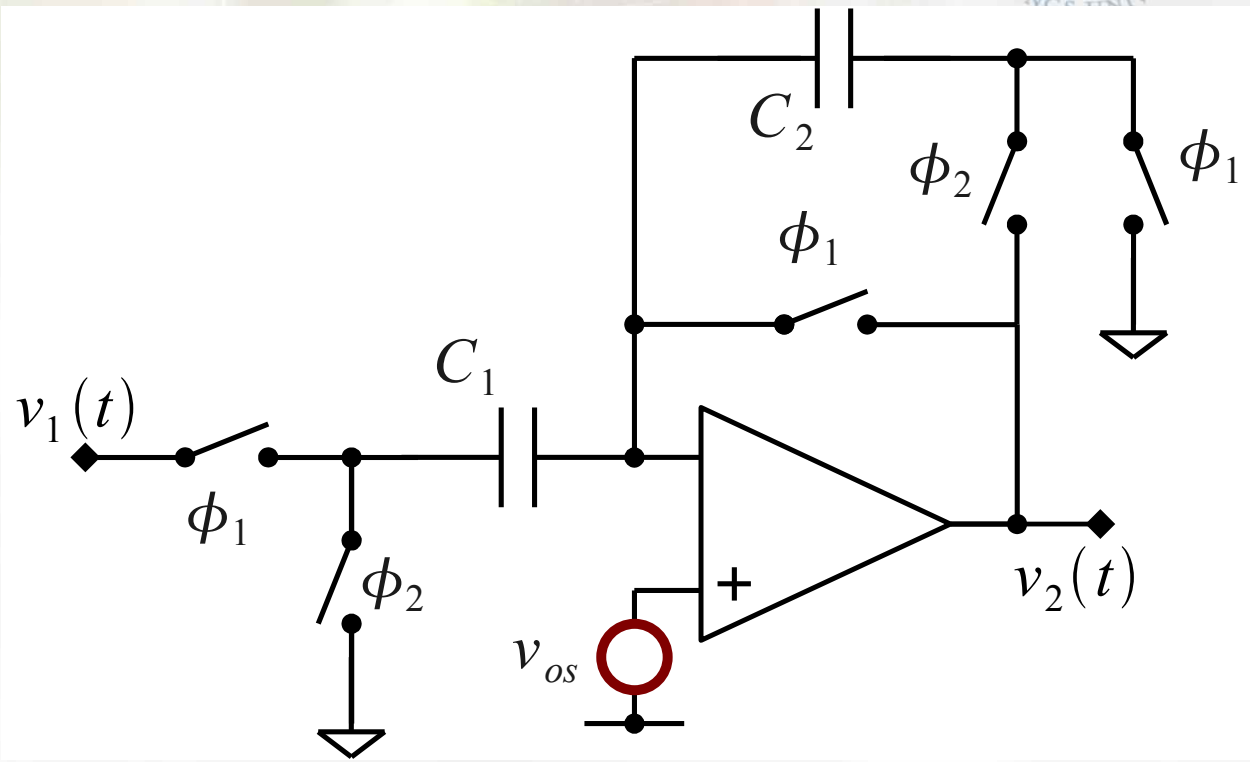
$$q_1 = C_1 \cdot (v_1 - v_{os})$$

$$q_2 = C_2 \cdot (0 - v_{os})$$

Second phase

$$q_1 = -C_1 \cdot v_{os}$$

$$q_2 = C_2 \cdot (v_2 - v_{os})$$

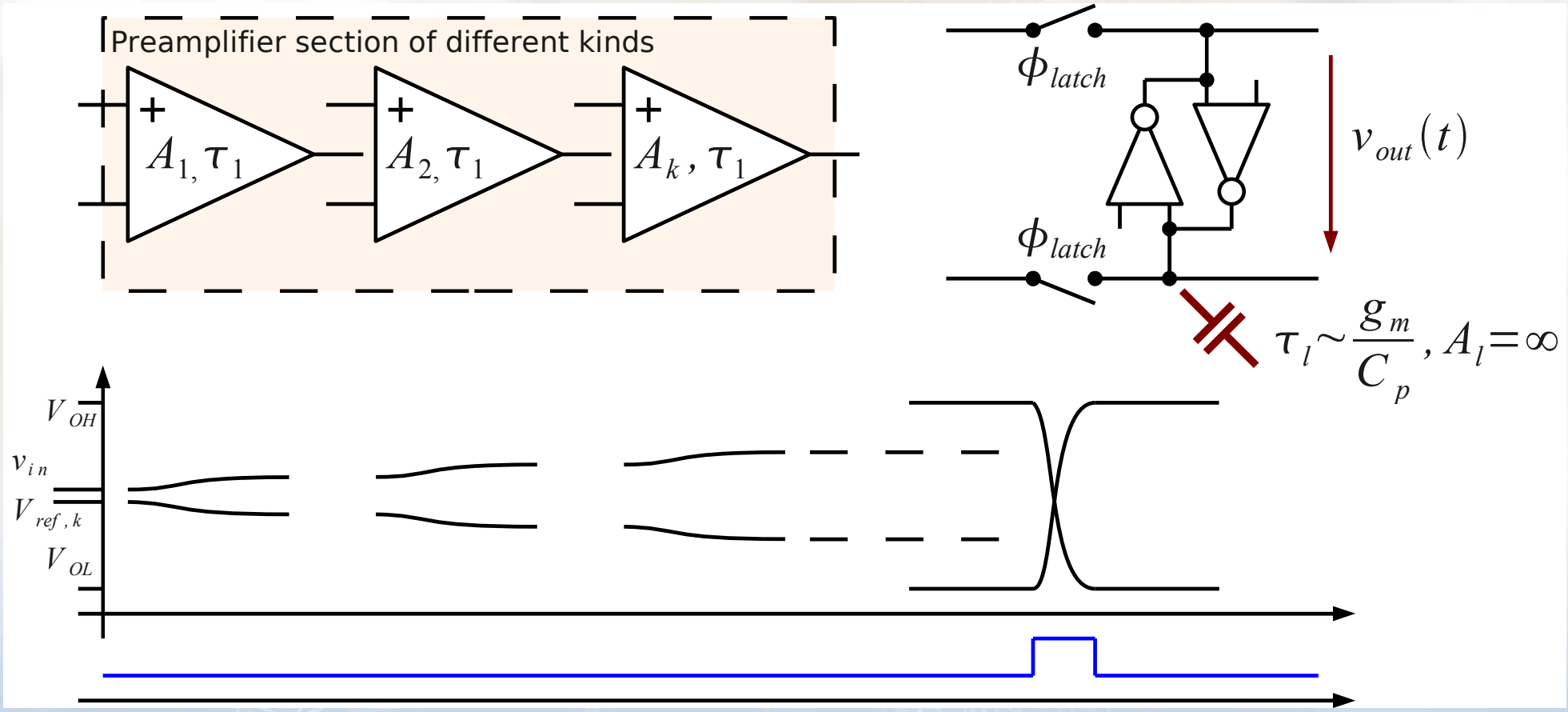


Total charge is preserved

$$C_1 \cdot (v_1 - v_{os}) - C_2 \cdot v_{os} = -C_1 \cdot v_{os} + C_2 \cdot (v_2 - v_{os}) \Rightarrow \frac{v_2}{v_1} = \frac{C_1}{C_2}$$ [OFFSET CANCELLED]

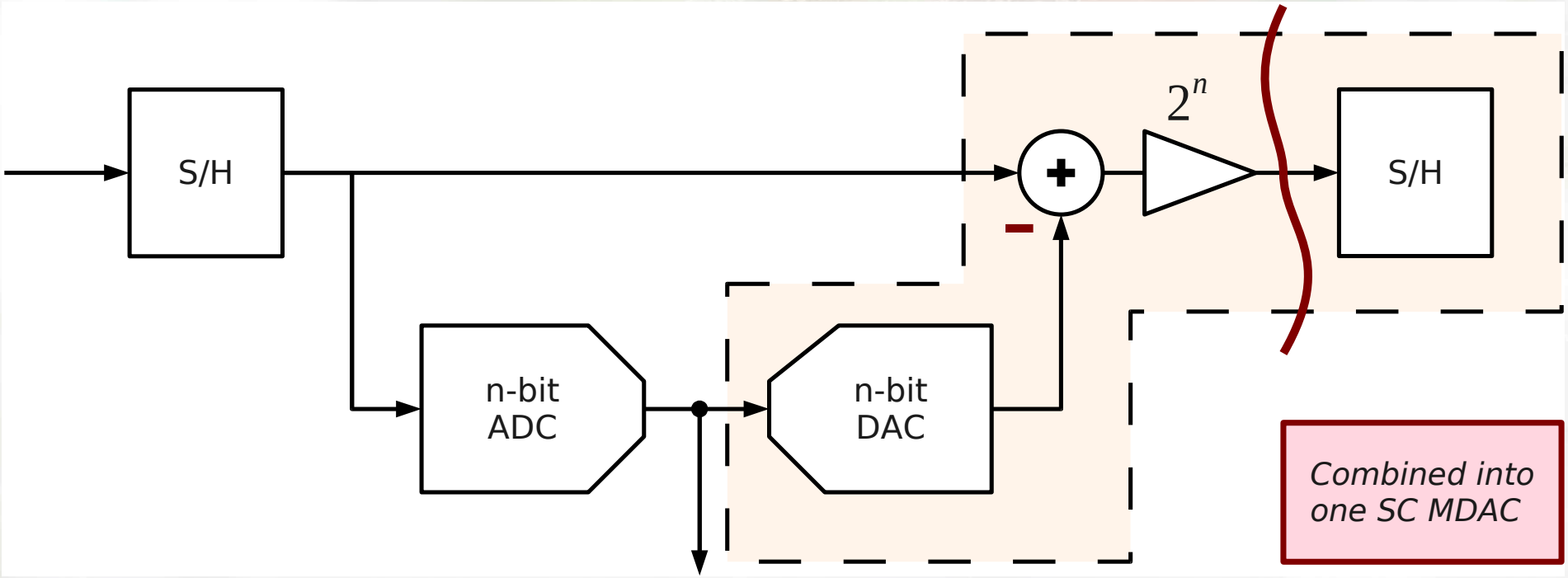
Comparators, structure

Use (low-gain) preamplifiers and then high-speed positive-feedback latch, which has infinite (DC) gain (time/gain trade-off)



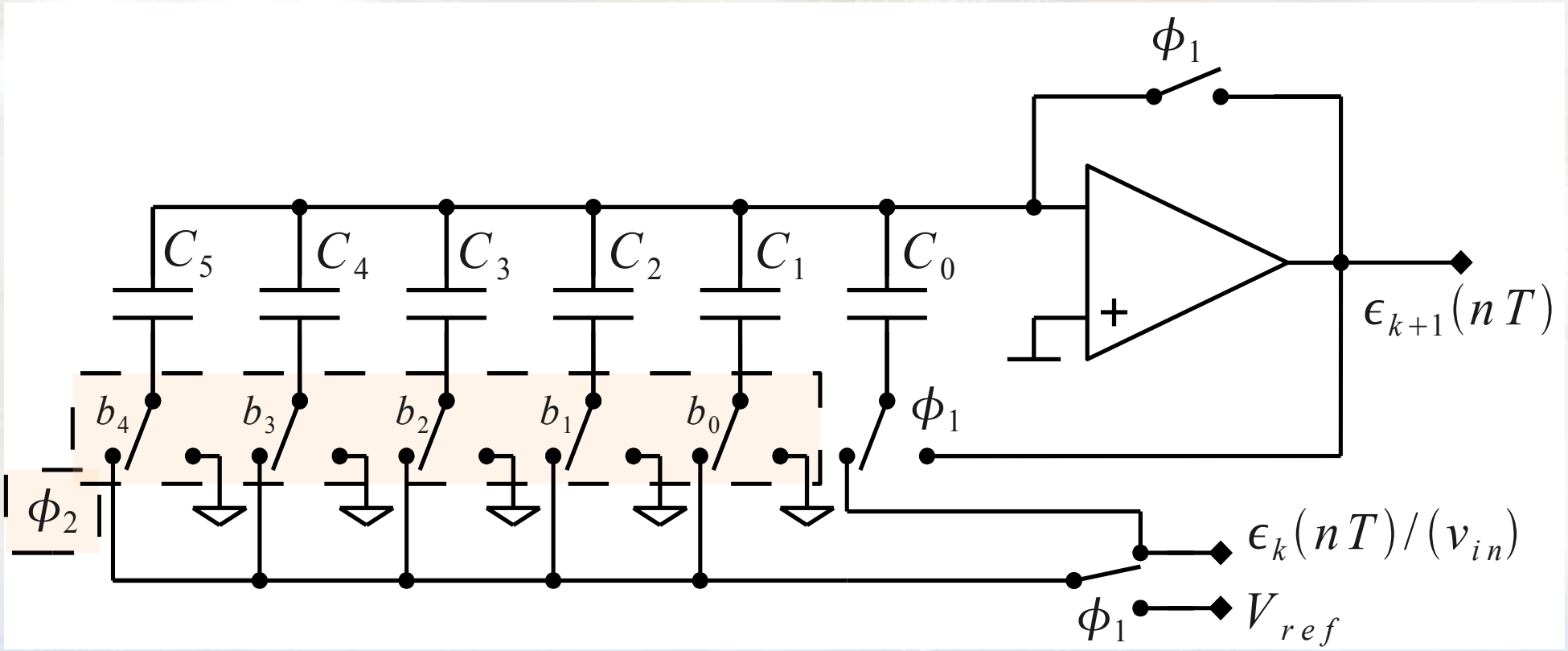
MDAC, concept

Combines the sub-DAC, adder, gain, and sample-and-hold



MDAC, SC implementation

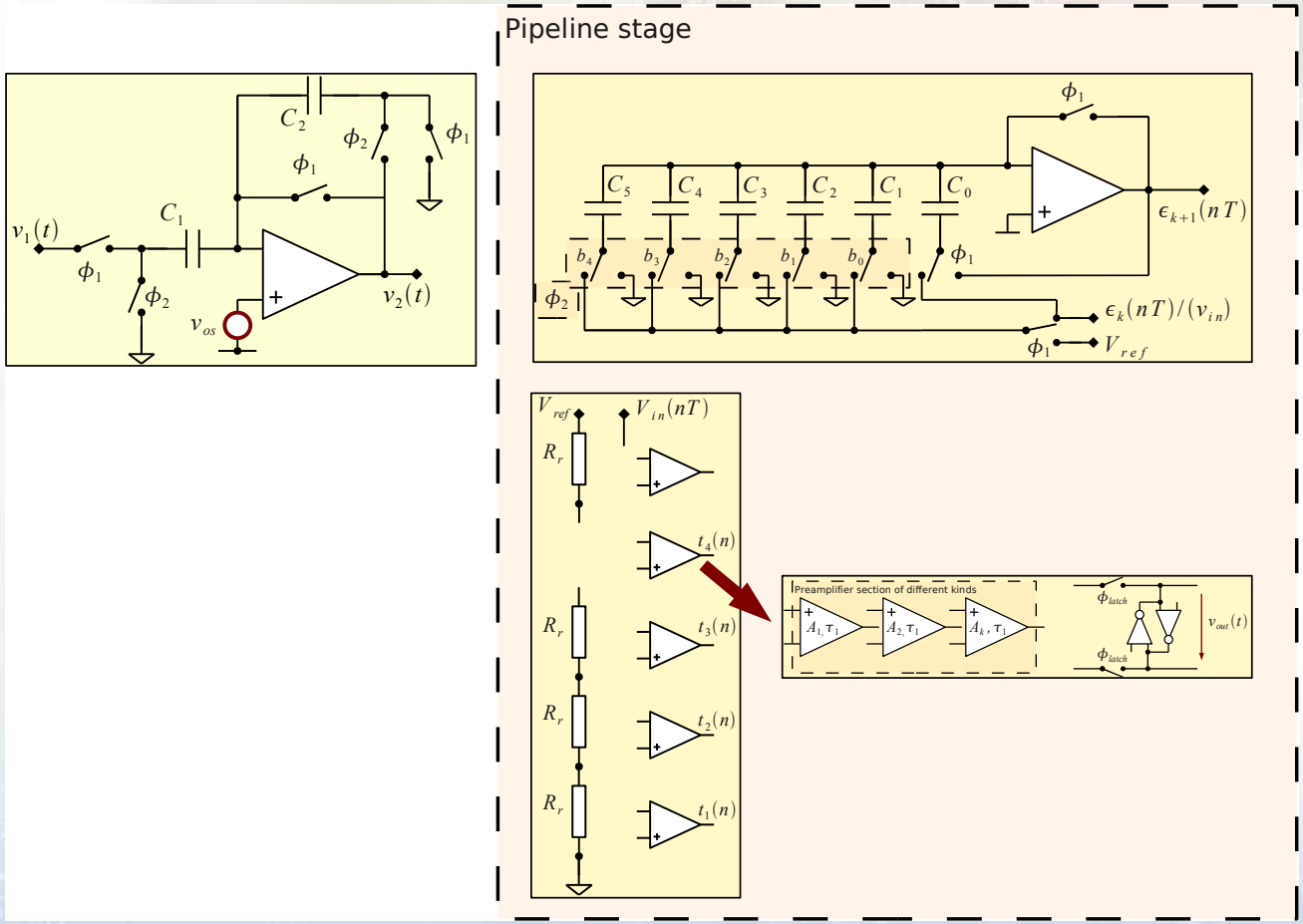
Bits b_i from the ADC (in the 5-bit example below they are binary)



Left as exercise to prove operation ...

Pipelined ADC, conclusions

Compact SC solution



What did we do today?

Looked at a pipelined ADC as design example

- Suggested a compact, resistive structure
- Described an error correction technique
- Outlined some examples on limiting factors on performance
- Outlined an offset cancellation technique for comparators
- Outlined a switched-capacitor architecture

What will we do next time?

Exam ...

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