



# Lecture 6, ANIK

Operational amplifiers  
Stability, compensation, etc.

# What did we do last time?



## Differential signals

Why differential?

Common-mode definitions

## Differential pair

Analysis

Operation

## Mismatch

Impact of mismatch on design/performance/behavior

# What will we do today?

Operational amplifiers

Stability

Frequency analysis

Compensation



# Operational amplifiers



## Operational amplifiers

- drive resistive loads
- have zero output impedance
- act like a voltage source

## Operational transconductance amplifiers

- drive capacitive loads
- have infinite output impedance
- act like a current source

# Gain increased with multi-stage amplifiers



Single-stage (cascodes) vs two-stage?

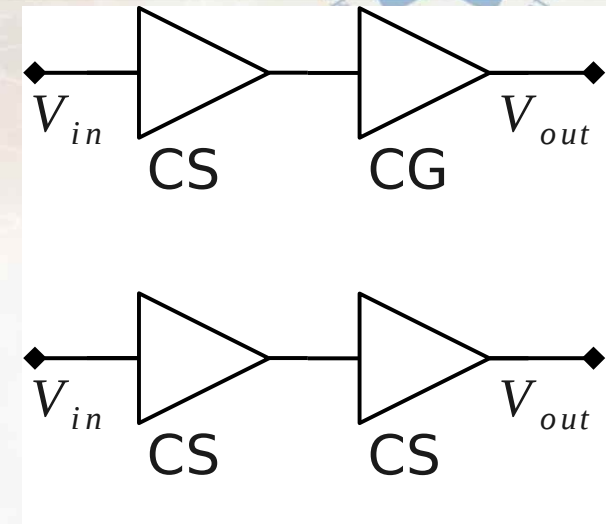
They will have the same DC gain

They will not have the same output impedance

Multiple poles ("one per stage")

The transfer function (in both cases) is

$$A(s) = \frac{A_1 \cdot A_2}{\left(1 + \frac{s}{p_{11}}\right) \cdot \left(1 + \frac{s}{p_{12}}\right)}$$



# Multiple poles

## Case 1 (CS+CG)

First amplifier sees low-impedance load:  $(g_1 + g_{m1}) \parallel C_1 \approx g_{m1} \parallel C_1$

Second amplifier sees capacitive load:  $g_{out} \approx g_2 \parallel C_2$

## Case 2 (CS+CS)

First amplifier sees high-impedance load  $(g_1 + 0) \parallel C_1 \approx g_1 \parallel C_1$

Second amplifier sees capacitive load:  $g_{out} \approx g_2 \parallel C_2$

Notice that the  $g_2$  in Case 2 is higher than  $g_2$  in Case 1.

# Regardless what you do ... Feedback

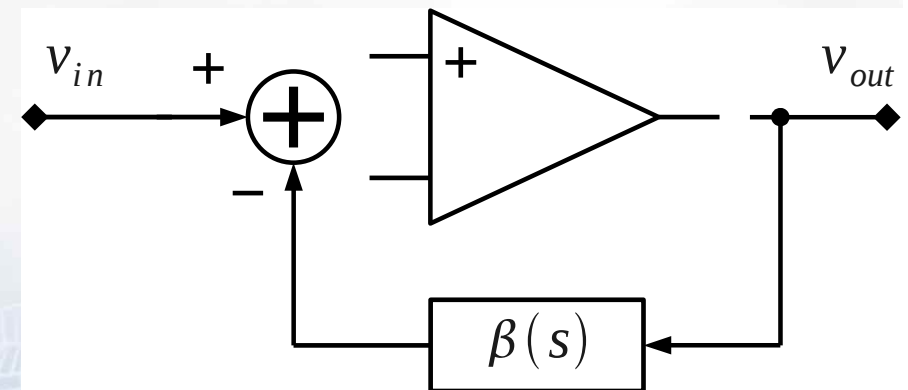


Preferrably, we have a controlled system with a closed-loop gain of:

$$Y(s) = (X(s) - \beta(s) \cdot Y(s)) \cdot A(s) \Rightarrow$$
$$\frac{Y(s)}{X(s)} = \frac{A(s)}{1 + \beta(s) \cdot A(s)} = \frac{1/\beta(s)}{1 + \frac{1}{\beta(s) \cdot A(s)}}$$

A feedback factor of:  $\beta(s)$

An open-loop gain of:  $\beta(s) \cdot A(s)$



# Why do you want controlled feedback?



Gain is now under control!

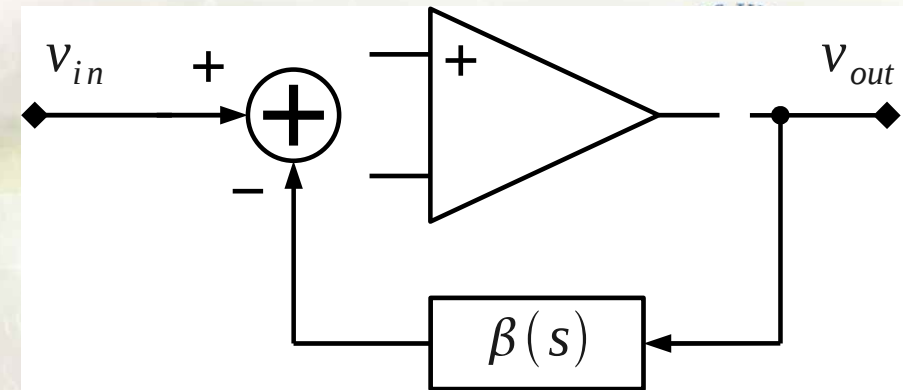
No variation with gm / gds, instead given by (normally) high-accuracy components



"Unlimited" drive capability

Isolation of input and output

Linearization



Remember, it is a regulation loop. It is designed to track the changes, anything added in the loop will be suppressed.

# The problem: Stability



In short: the transfer function must be designed such that

$$\beta(s) \cdot A(s) \neq -1$$

If this is the case, we have an infinitely high transfer function

(In reality, the proof is quite complex.)

Phase margin (how far are we off from this to happen)

Poor phase margin gives ringing in the output when applying step

Critically damped signal at approximately 70 degrees (poles become real rather than complex pair, i.e., they are well splitted)

# Stability, cont'd



Bode plot

What happens to the transfer characteristics?

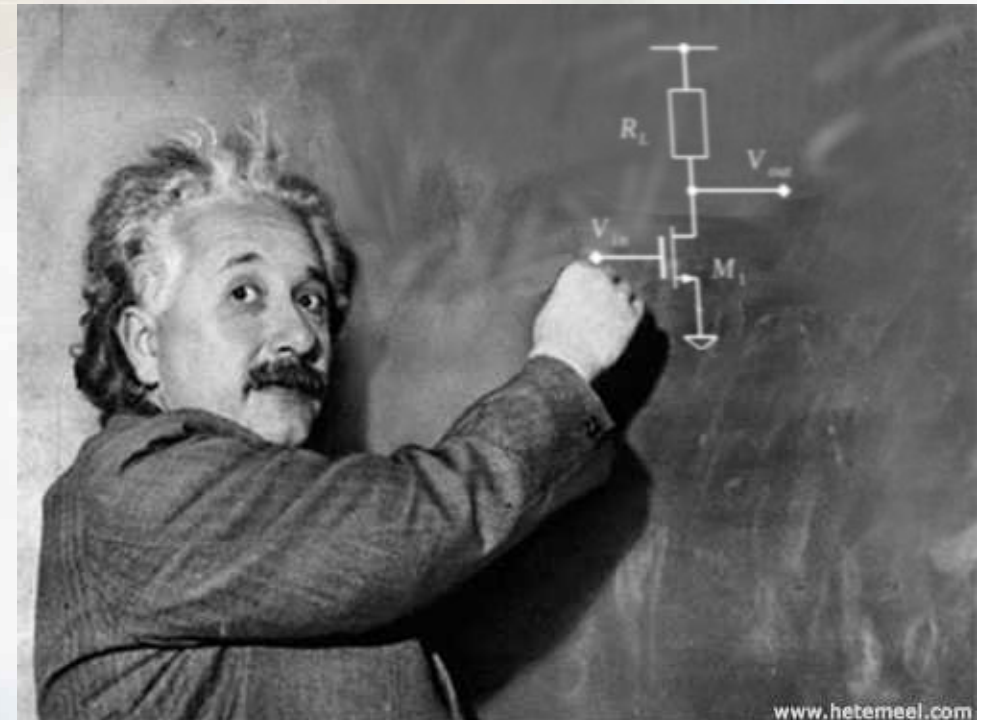
Phase margin

Step response

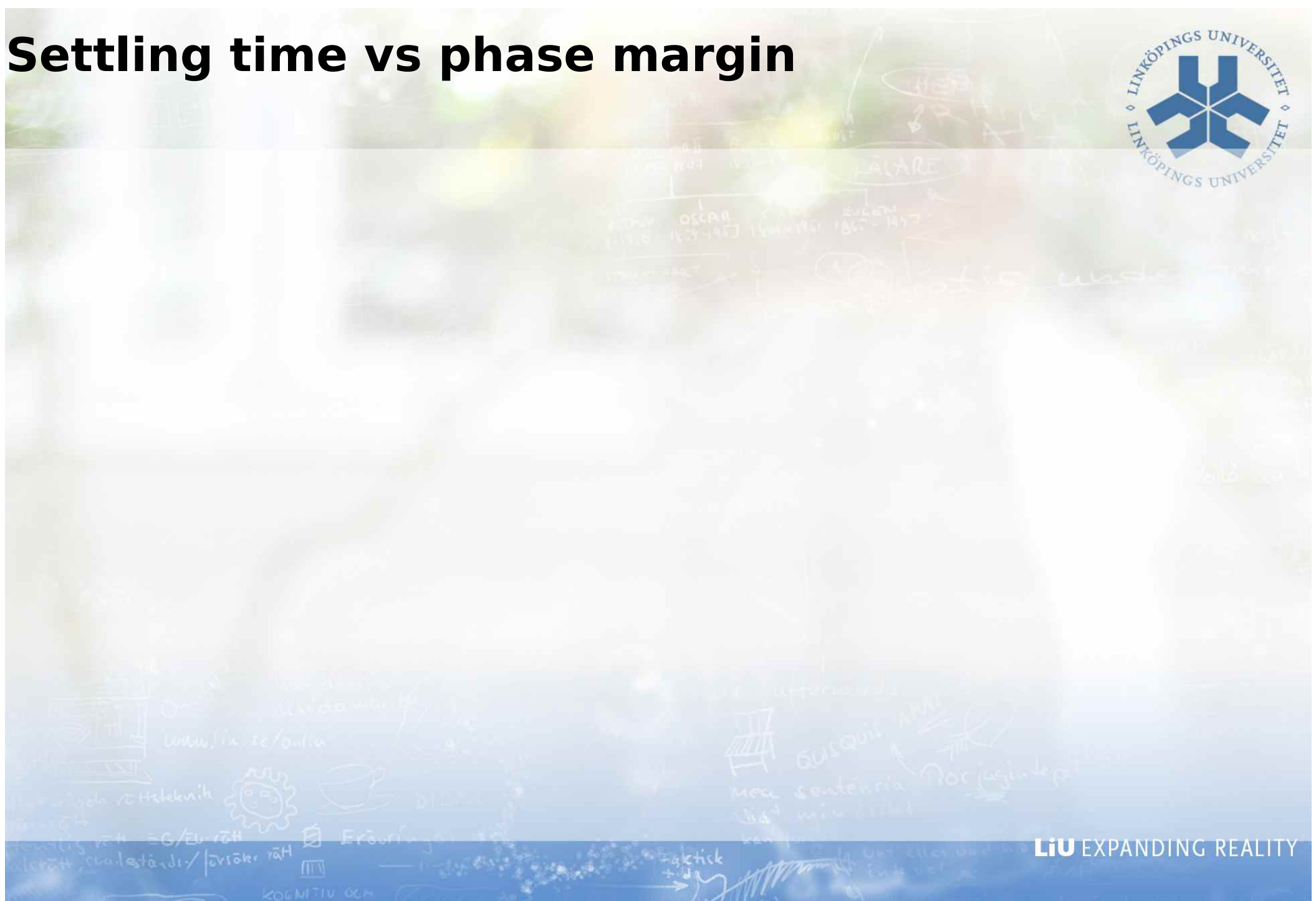
Settling

Oscillations

Critically damped at 70 degrees



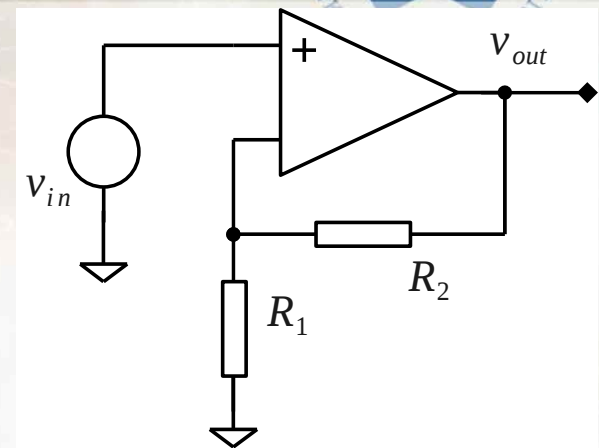
# Settling time vs phase margin



# What's behind the story?

Ideal case:

$$\frac{R_1}{R_1 + R_2} \cdot v_{out} = v_{in} \Rightarrow \frac{v_{out}}{v_{in}} = \frac{R_1 + R_2}{R_1} = \Gamma$$



Non-ideal gain case:

$$\begin{aligned} v_{out} &= A_0 \cdot \left[ v_{in} - \frac{R_1}{R_1 + R_2} \cdot v_{out} \right] \Rightarrow \frac{v_{out}}{v_{in}} = \frac{1}{\frac{1}{A_0} + \frac{R_1}{R_1 + R_2}} = \\ &= \frac{R_1 + R_2}{R_1} \cdot \frac{1}{1 + \frac{R_1 + R_2}{A_0 \cdot R_1}} = \frac{\Gamma}{1 + \frac{\Gamma}{A_0}} \end{aligned}$$

# What's behind the story, cont'd?

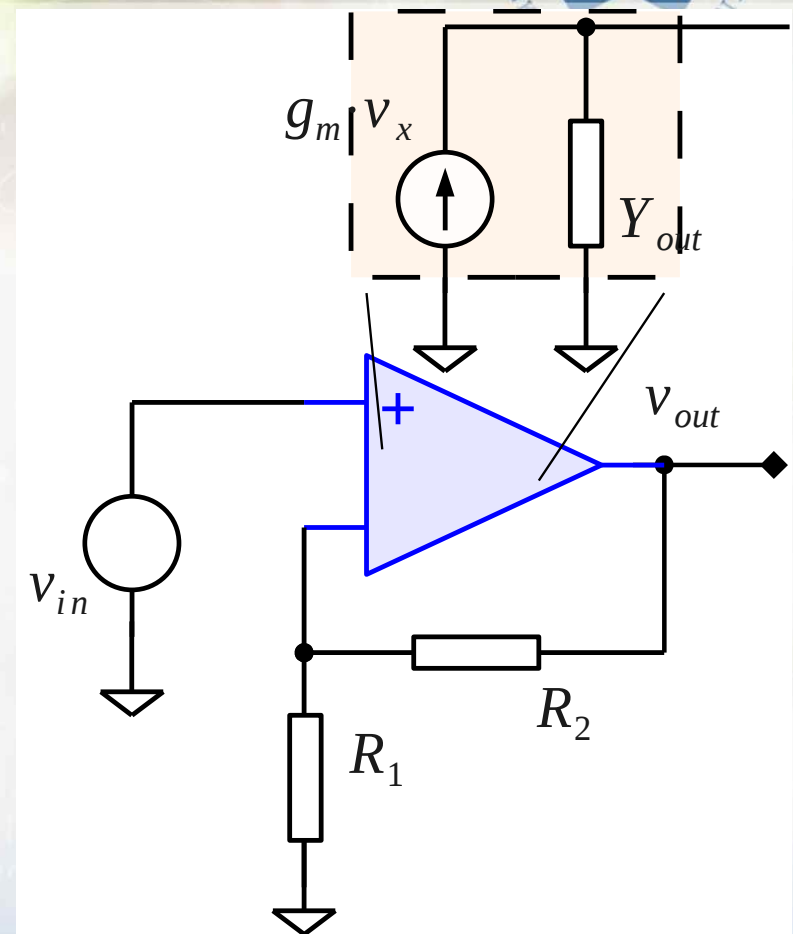
Single-pole model (ignore the effect of output impedance mismatch):

$$\frac{v_{out}}{v_{in}} = \frac{\Gamma}{1 + \frac{\Gamma}{A_0} \cdot \left(1 + \frac{p_1}{s}\right)}$$

Results in

$$\frac{v_{out}}{v_{in}} = \frac{\frac{\Gamma}{1 + \Gamma/A_0}}{1 + \frac{\Gamma/A_0}{1 + \Gamma/A_0} \cdot \frac{p_1}{s}} \approx \frac{\Gamma}{1 + \frac{p_1}{s}}$$

The amplifier will band-limit the system!



# What's behind the story, cont'd?

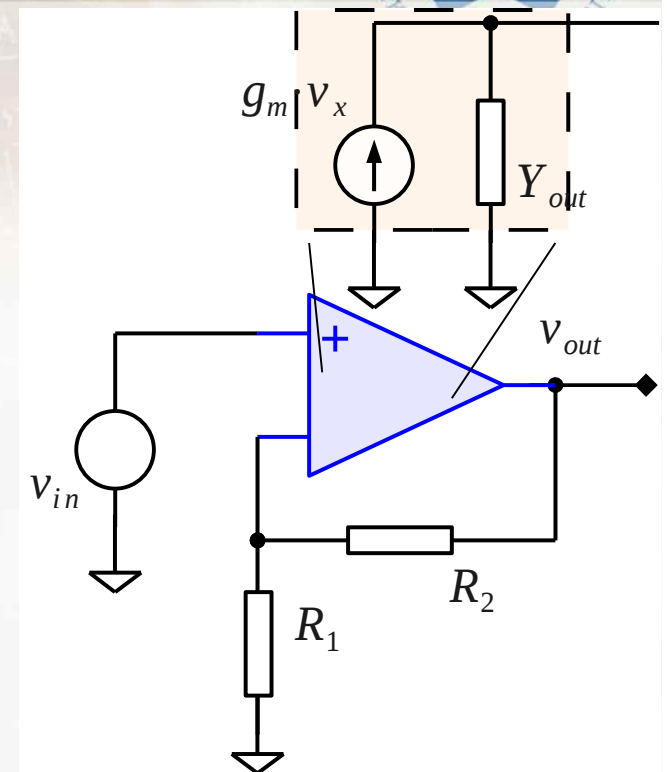


Any-pole model:

$$v_x = \frac{R_1}{R_1 + R_2} \cdot v_{out}$$

$$g_m(v_{in} - v_x) + (0 - v_{out})Y_{out} + \frac{0 - v_{out}}{R_1 + R_2} = 0$$

$$g_m v_{in} = v_{out} \cdot \left[ Y_{out} + \frac{1 + R_1 g_m}{R_1 + R_2} \right]$$



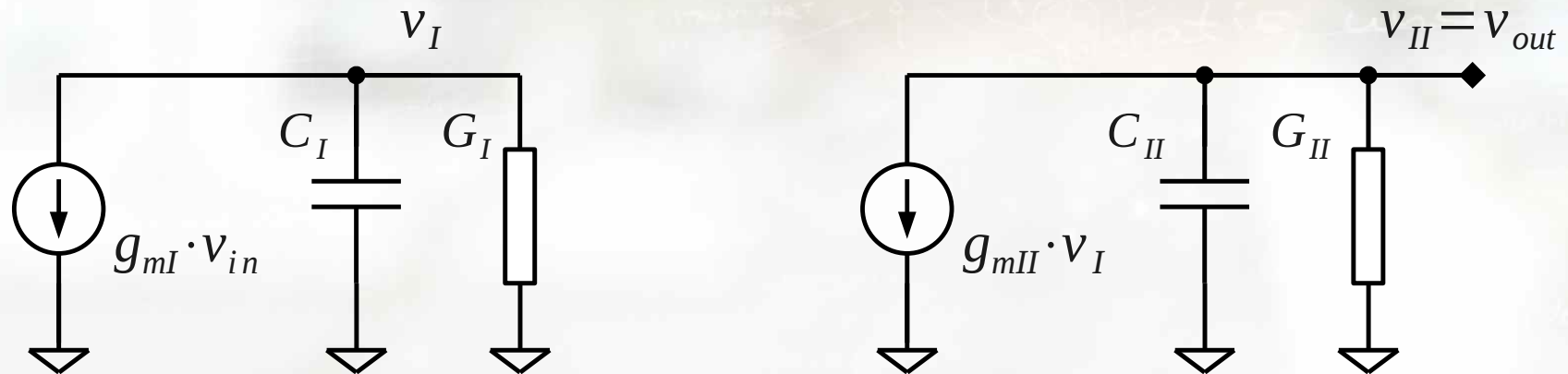
Which boils down to something more complex:

$$\frac{v_{out}}{v_{in}} = \frac{\Gamma}{1 + \frac{1}{g_m R_1} + \frac{\Gamma}{g_m / Y_{out}}}$$

# We need to be a bit more systematic



The model (high-impedance load) and focus on two-pole systems



$$p_1 = \frac{G_I}{C_I}, \quad p_2 = \frac{G_{II}}{C_{II}}, \quad A_1 = \frac{g_{mI}}{G_I}, \quad A_2 = \frac{g_{mII}}{G_{II}}$$



# Dominant pole assumption (output)



Assuming pole splitting,  $p_2 \gg p_1$ , gives us

$$A(s) = \frac{A_1 \cdot A_2}{\left(1 + \frac{s}{p_{11}}\right) \cdot \left(1 + \frac{s}{p_{12}}\right)} \approx \frac{A_1 \cdot A_2}{1 + \frac{s}{p_1} + \frac{s^2}{p_1 \cdot p_2}}$$

This implies:  $\omega_{ug} \approx A_1 \cdot A_2 \cdot p_1$  and

$$\phi_m = 180 - \arg A(j\omega_{ug}) = 180 - \operatorname{atan} \frac{\omega_{ug}}{p_1} - \operatorname{atan} \frac{\omega_{ug}}{p_2} \approx 90 - \operatorname{atan} \frac{\omega_{ug}}{p_2}$$

$$\phi_m \approx 90 - \operatorname{atan} \left( A_0 \cdot \frac{p_1}{p_2} \right)$$

# The formulas (dominant load!)



Unity-gain frequency

$$\omega_{ug} \approx \frac{g_{mI} \cdot g_{mII}}{G_I \cdot G_{II}} \cdot \frac{G_{II}}{C_{II}} = \frac{g_{mI} \cdot g_{mII}}{G_I \cdot C_{II}}$$

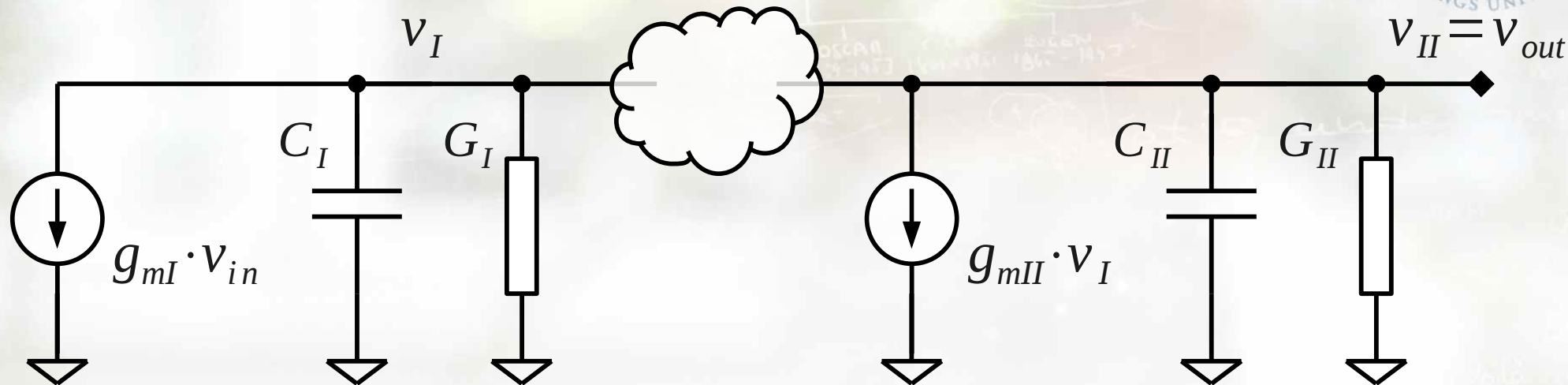
Phase margin

$$\phi_m \approx 90 - \operatorname{atan} \frac{\omega_{ug}}{p_2} = 90 - \operatorname{atan} \frac{\frac{g_{mI} \cdot g_{mII}}{G_I \cdot C_{II}}}{\frac{G_I}{C_I}} = 90 - \operatorname{atan} \frac{g_{mI} \cdot g_{mII} \cdot C_I}{G_I^2 \cdot C_{II}}$$

etc., etc., etc.

We need to be a bit more organized...

# Compensation, poles are too close



The "cloud" is typically a capacitor or a series resistor-capacitor.

# Compensation, Miller capacitance



Introduced zero	Parasitic pole	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C}$	$p_2 = \frac{-g_{mII}}{C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

Introduced zero	Parasitic pole	Phase margin
$z_1 \approx 10 \cdot \omega_{ug}$	$p_2 \approx 2.2 \cdot \omega_{ug}$	$\approx 60$

Dominant pole moves "down", parasitic pole moves "up"

Parasitic zero added (harmful for phase margin)

# Compensation, Nulling resistor 1



Introduced zero	Parasitic poles	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C} \cdot \frac{1}{1 - R_Z \cdot g_{mII}}$	$p_2 = \frac{-g_{mII}}{C_{II}}, \quad p_3 = \frac{-1}{R_Z \cdot C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

$$R_Z = \frac{1}{g_{mII}} \cdot \left( 1 + \frac{C_{II}}{C_C} \right)$$

Introduced zero	Parasitic pole	Phase margin
$z_1 \rightarrow p_2$	$p_3 \approx 1.73 \cdot \omega_{ug}$	$\approx 60$

# Compensation, Nulling resistor 2



Introduced zero	Parasitic poles	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C} \cdot \frac{1}{1 - R_Z \cdot g_{mII}}$	$p_2 = \frac{-g_{mII}}{C_{II}}, p_3 = \frac{-1}{R_Z \cdot C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

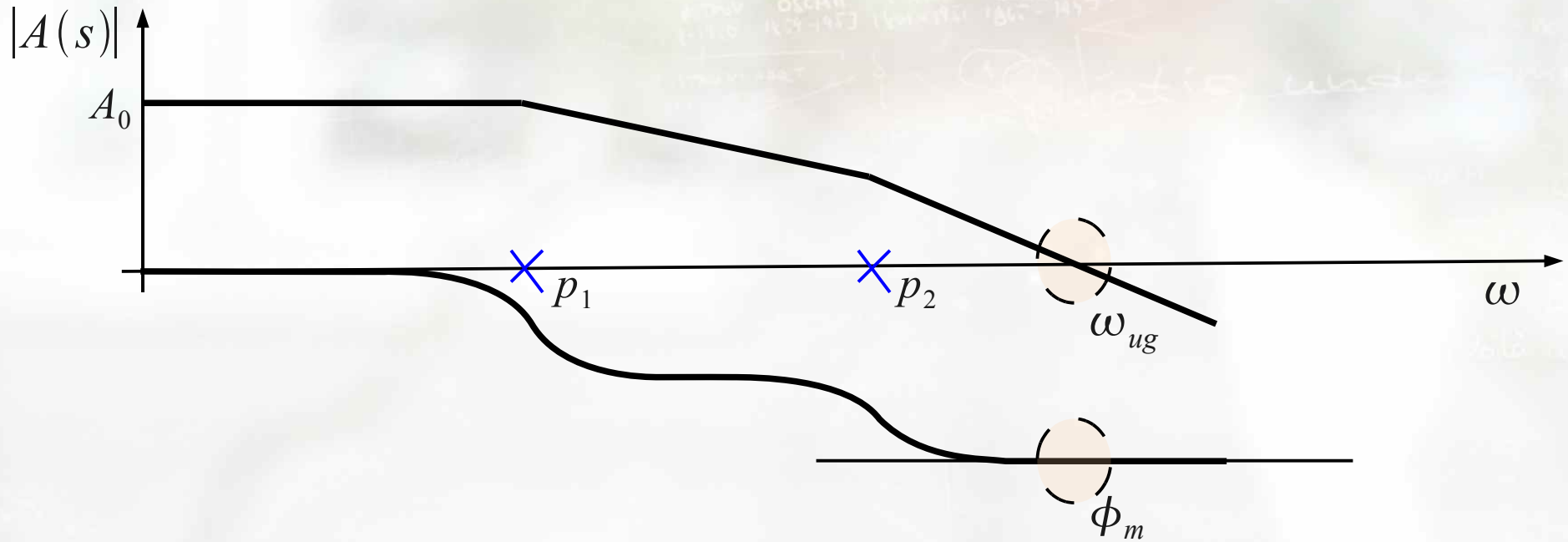
$$R_Z = \frac{1}{g_{mII}}$$

Introduced zero	Parasitic pole	Phase margin
$z_1 \rightarrow \infty$	$p_2 \approx 1.73 \cdot \omega_{ug}, p_3 > 10 \cdot \omega_{ug}$	$\approx 60$

# Poles and zeros revisited



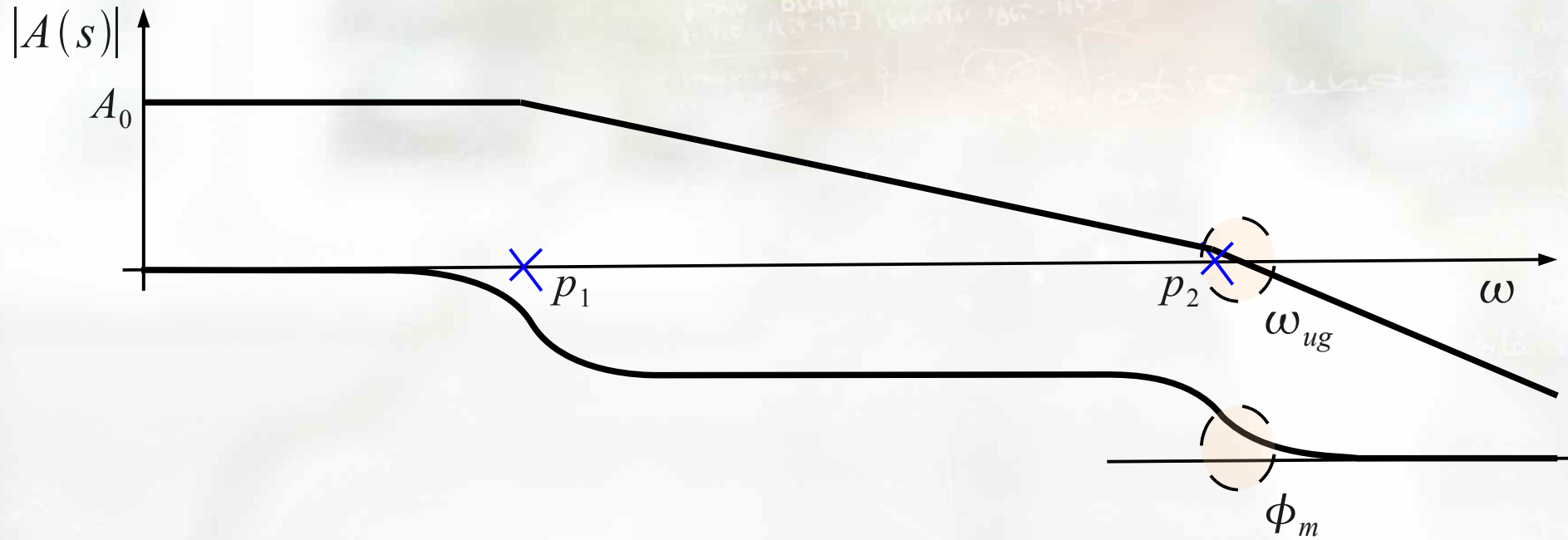
Stable?



# Poles and zeros revisited



Stable?

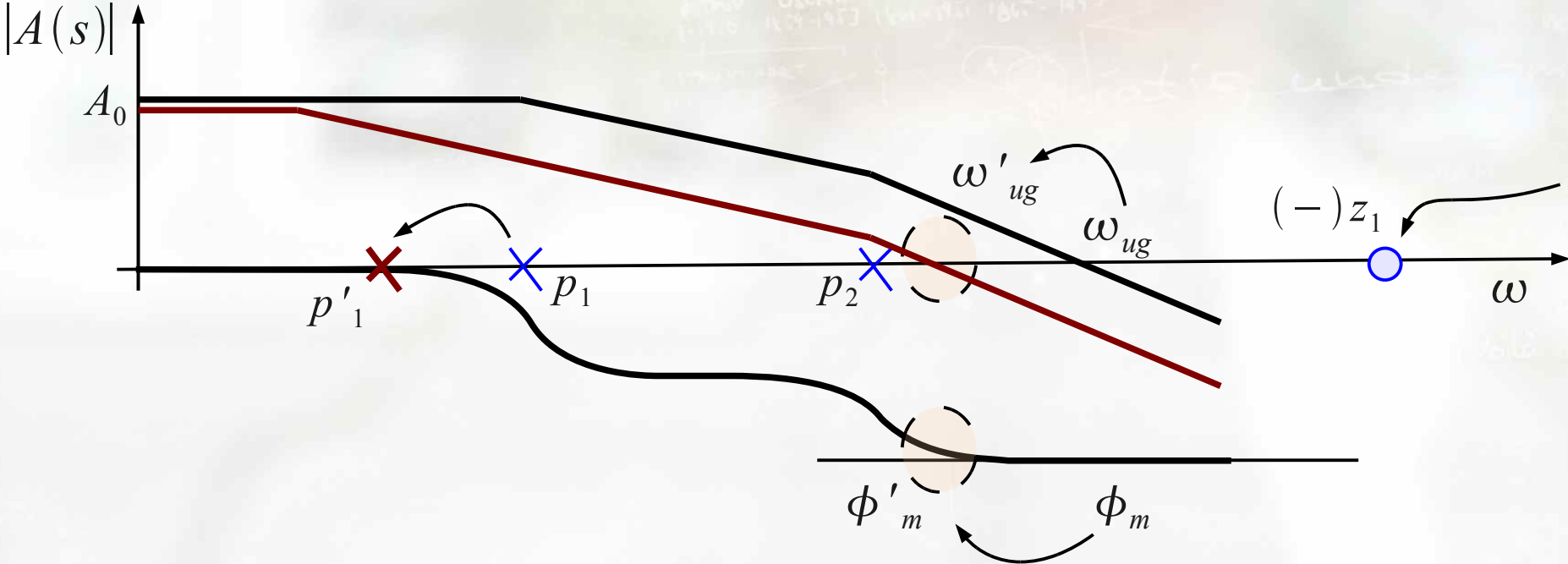




# Compensation



What is the cost associated with compensation?



# Compensation, two cases:



## 1) "Internal" node sees a low-impedance node

Typically: output load dominates, and we should drive a capacitive load  
Load-compensation, i.e., increase cap externally

## 2) "Internal" node sees a high-impedance node

Typically: internal load dominates, and we should drive a resistive load  
Miller-compensation, i.e., utilize the second-stage gain to multiply  $C_C$

As always, some exceptions to the rule:

We could add common-drain at output

Nested compensation, active compensation, ... and more ...

# Compensation compiled:



	Miller	Load compensation
Cap	<p>A circuit diagram showing two inverters in series. A capacitor is connected between the output of the first inverter and the input of the second inverter. This capacitor is highlighted with a dashed orange box. A load capacitor is connected to the output of the second inverter to ground.</p>	<p>A circuit diagram showing two inverters in series. A load capacitor is connected to the input of the second inverter to ground. A compensation capacitor is connected between the output of the first inverter and the input of the second inverter. This compensation capacitor is highlighted with a dashed orange box.</p>
Cap + Res	<p>A circuit diagram showing two inverters in series. A resistor and a capacitor are connected in parallel between the output of the first inverter and the input of the second inverter. This parallel combination is highlighted with a dashed orange box. A load capacitor is connected to the output of the second inverter to ground.</p>	<p>A circuit diagram showing two inverters in series. A load capacitor is connected to the input of the second inverter to ground. A parallel combination of a resistor and a capacitor is connected between the output of the first inverter and the input of the second inverter. This parallel combination is highlighted with a dashed orange box.</p>

# Rule-of-thumbs for hand-calculation



Use MATLAB or similar to support your calculations for better understanding

See for example

[/site/edu/es/ANTIK/antikPoleZero.m](#)

[/site/edu/es/ANTIK/antikSettling.m](#)

In the end, use the simulator.

It has to be robust over several corners, temperatures, and other variations.

Hand calculations are incorrect per definition

Model corresponds quite well with circuit once you have identified the different stages

See for example exercises



# What did we do today?



Operational amplifiers

Top-level aspects

Compensation

Stability

# What will we do next time?

Operational amplifiers

Circuit-level aspects

