Lecture 5, ANIK

Differential signals and circuits
Mismatch

LiU EXPANDING REALITY

What did we do last time?

Current mirrors

- Simple, Cascoded, and Wide-Swing
- Decoupling design parameters using current mirrors

Improved amplifier stages

- Folded-cascoded gain stage
- Gain-boosting

The switch

The frequency domain

- Dominant-pole, DC gain, unity-gain frequency

Revisit frequency domain

Bode plot

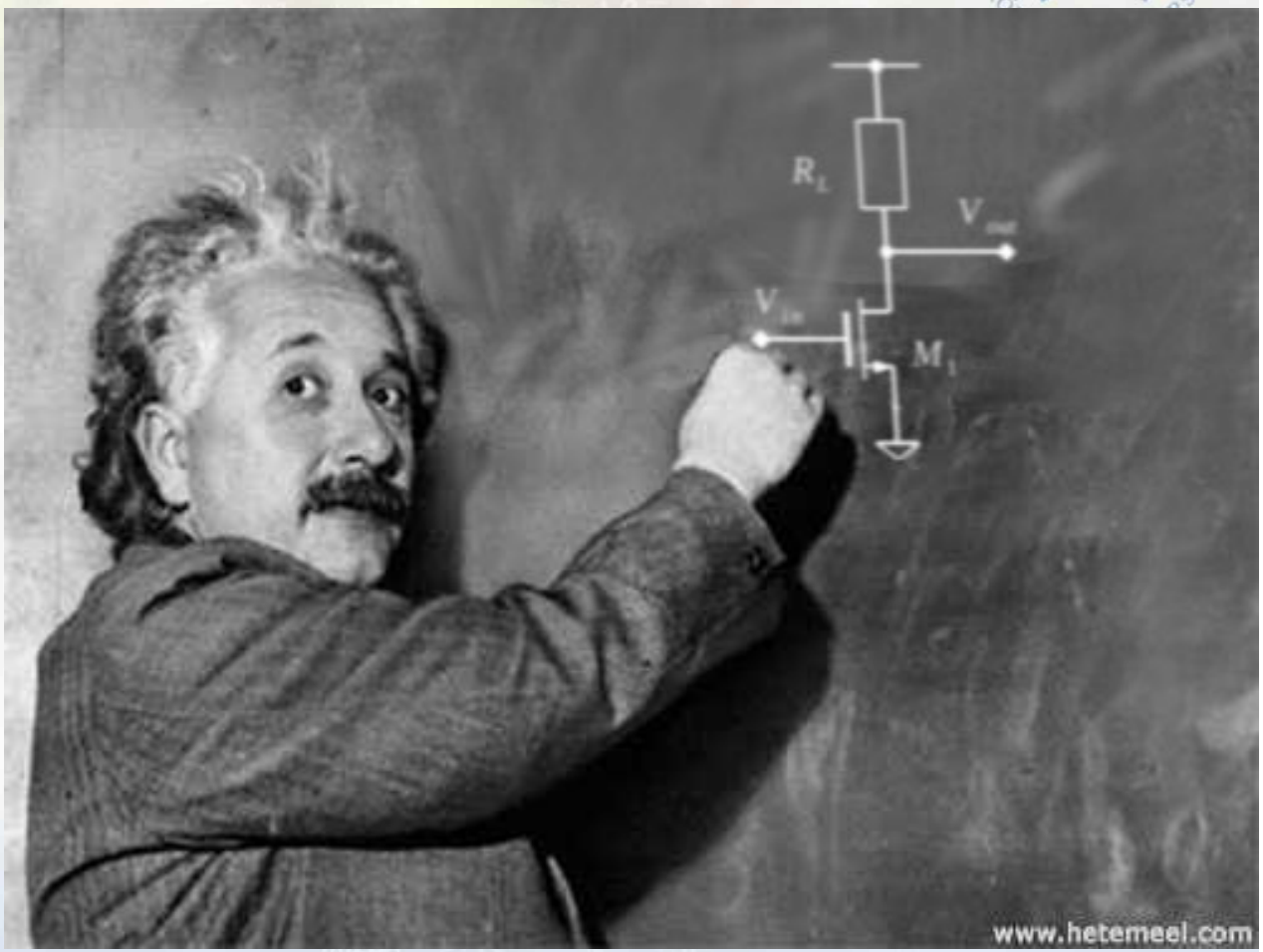
Pole

Zero

Phase margin

Gain vs frequency trade-off

$$A_0 \cdot p_1 \approx \omega_{ug}$$



What will we do today?

Differential signals

- Why differential?
- Common-mode definitions

Differential pair

- Analysis
- Operation

Mismatch

- Impact of mismatch on design/performance/behavior

Differential signals

Differential signals

$$\Delta V = V_p - V_n$$

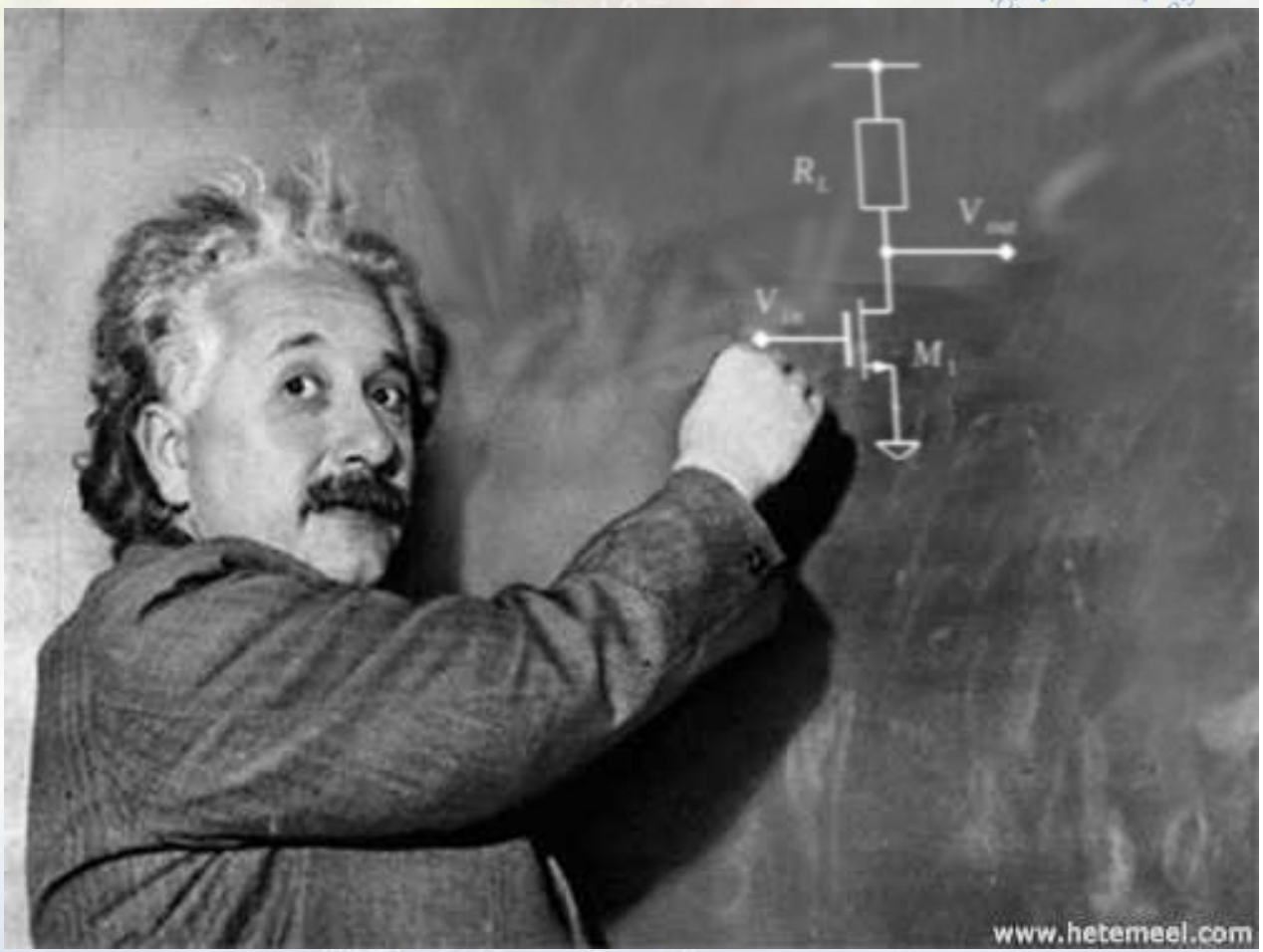
Common-mode signal

$$\nabla V = \frac{V_p + V_n}{2}$$

Common-mode supression

Should cancel common-mode (why?)

The matrix



Differential signals, the matrix compiled

Compile the transfer functions into a handy matrix

$$\begin{bmatrix} \Delta V_{out} \\ \nabla V_{out} \end{bmatrix} = \begin{bmatrix} A_{df} & A_{df,cm} \\ A_{cm,df} & A_{cm} \end{bmatrix} \begin{bmatrix} \Delta V_{in} \\ \nabla V_{in} \end{bmatrix}$$

Which terms should be 0?

Differential signals, metrics

Common-mode rejection ratio

$$\mathrm{CMRR} = \frac{A_{df}}{A_{cm}}$$

Design targets

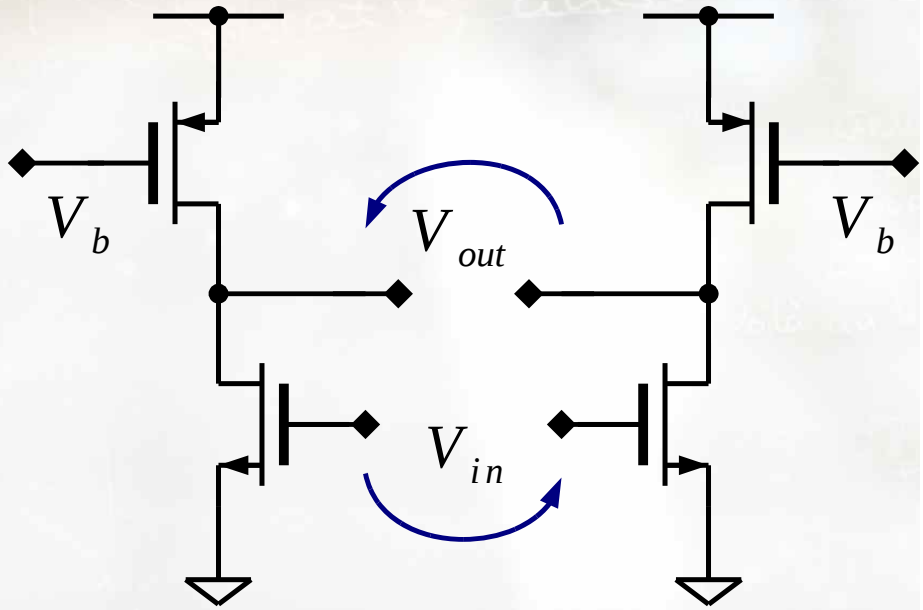
- Maximize the differential gain
- Minimize the common-mode gain

Differential signals, two CS stages

Common-mode range (CMR)

Common-mode levels for which the transistors operate in saturation

The common-mode rejection is 0 dB - effectively there is no rejection!



Differential signals

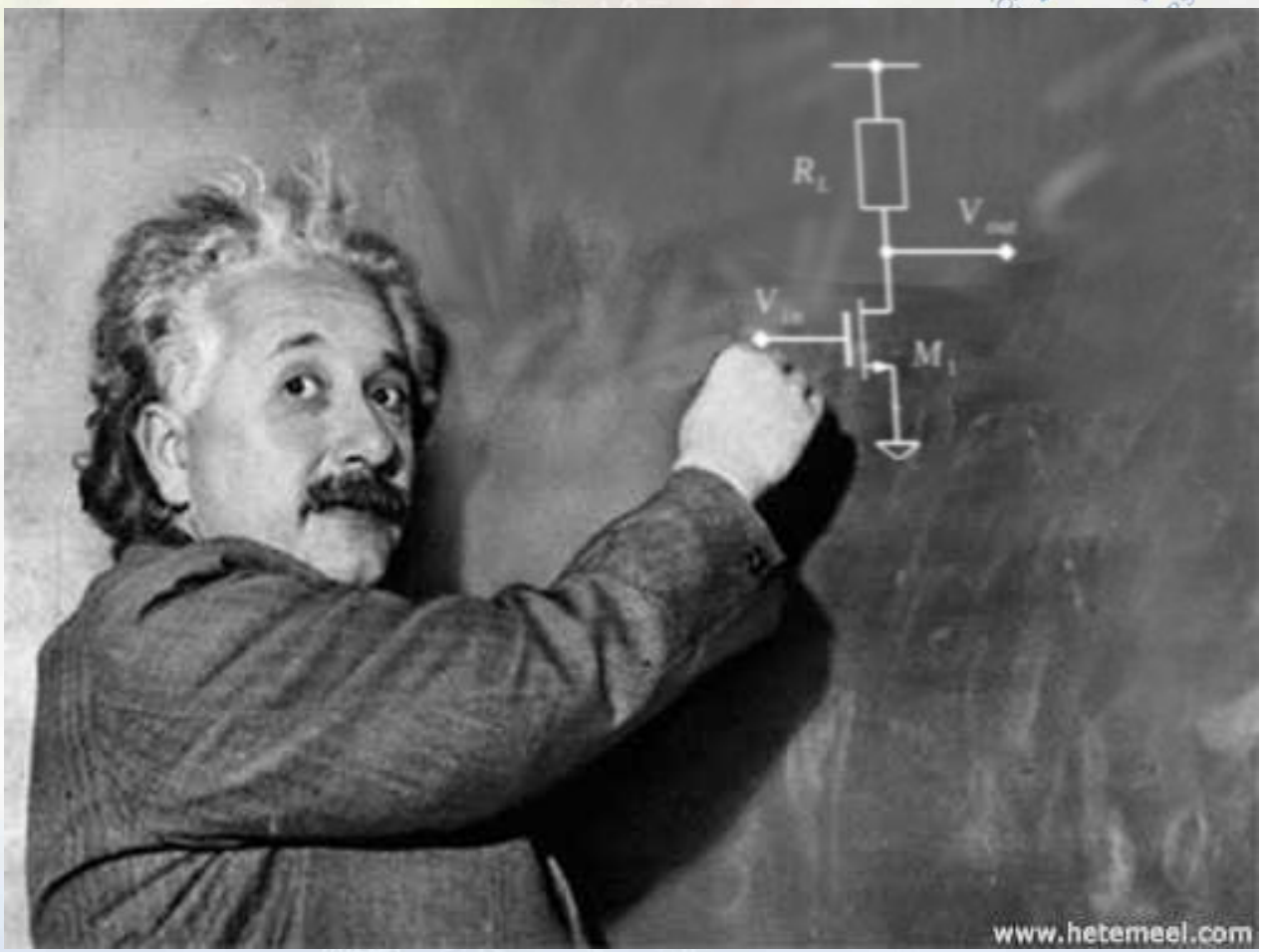
Two common-source stages in parallel

$$\mathrm{CMRR} = \frac{A_{df}}{A_{cm}}$$

The differential pair

Tail source

$$\mathrm{CMRR} = \infty$$



Differential signals, differential pair

Improved (infinite) CMRR to the cost of CMR

$\Delta I = 4\alpha \cdot V_{eff} \cdot \Delta V$ and $\nabla I = I_0/2$ (!)

Further on

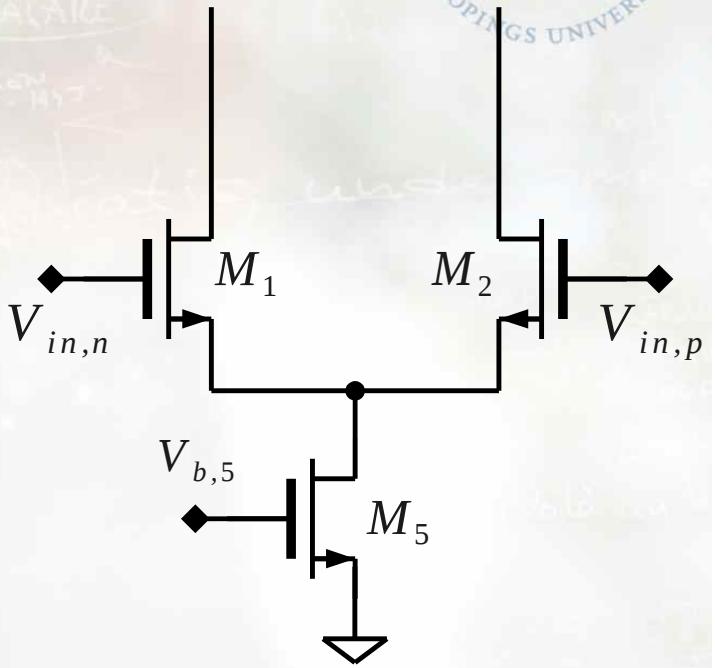
$$I_0 = 2\alpha \cdot \left(V_{eff}^2 + \Delta V^2 \right)$$

combines into

$$\Delta I = 4\alpha \cdot \Delta V \cdot \sqrt{\frac{I_0}{2\alpha} - \Delta V^2} \quad (!)$$

such that

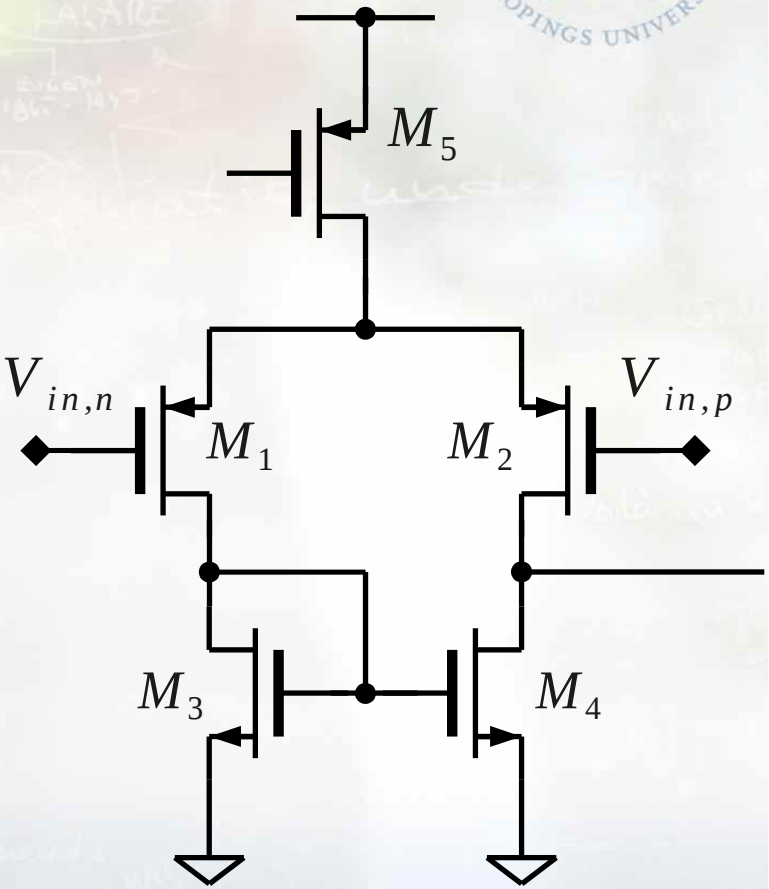
$$\frac{d\Delta I}{d\Delta V} = 4\alpha \cdot \sqrt{\frac{I_0}{2\alpha}} = 4\alpha V_{eff} = \frac{2I_0}{V_{eff}} \text{ and } \frac{d\nabla I}{d\nabla V} = 0$$



Differential pair with active load

Current-to-voltage conversion

- Resistors
- Current mirror active load
- Current-source active load



Common-mode can be further supressed using a common-mode feedback circuit (CMFB)

- Additional feedback amplifier sensing the common-mode level at the output

And that were all basic building blocks!

The basic stages

- Common-source, Common-gate, Common-drain
- Current-mirror

Enhanced gain

- Gain boosting, (Telescopic) cascodes, folded cascode
- Multiple-stages

The differential pair

Mismatch, or

"In reality, nothing is perfect ..."

Differences in

- Fabs (wafer-to-wafer, fabrication, date)
- Wafer locations (chip-to-chip, doping)
- Transistor (block-by-block, orientation and side effects, doping)
- Temperatures, Voltages, Currents

You cannot assume that one transistor is identical to another

- Especially not for high-speed, high-accuracy applications

Mismatch, cont'd

The drain current in the saturation region:

$$\Delta I_D = \underbrace{\frac{dI_D}{d\beta}\cdot\Delta\beta + \frac{dI_D}{dS}\cdot\Delta S}_{\Delta\alpha} + \frac{dI_D}{dV_{eff}}\cdot\Delta V_{eff} + \frac{dI_D}{dV_{ds}}\cdot\Delta V_{ds} =$$

$$= \underbrace{\frac{I_D}{\beta}\cdot\Delta\beta + \frac{I_D}{S}\cdot\Delta S}_{\Delta\alpha} + \frac{2I_d}{V_{eff}}\cdot\Delta V_{eff} + \frac{\lambda I_d}{1+\lambda(V_{ds}-V_{eff})}\cdot\Delta V_{ds} \Rightarrow$$

$$\frac{\Delta I_D}{I_D} = \underbrace{\frac{\Delta\beta}{\beta} + \frac{\Delta S}{S}}_{\Delta\alpha} + \frac{2\Delta V_{eff}}{V_{eff}} + \frac{\lambda\Delta V_{ds}}{1+\lambda(V_{ds}-V_{eff})} \Rightarrow$$

$$\frac{\Delta I_D}{I_D} \approx \frac{\Delta\alpha}{\alpha} + \frac{2\Delta V_{eff}}{V_{eff}}$$

Mismatch, cont'd

Ignoring the low-impact ones, and assuming that they are decoupled, gives us, with the help of stochastic variables:

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right)=\sigma^2\left(\frac{\Delta \alpha}{\alpha}\right)+\frac{\sigma^2\left(\Delta V_{eff}\right)}{V_{eff}^2}$$

First-order assumptions

$$\sigma^2\left(\frac{\Delta \alpha}{\alpha}\right)\approx\frac{A_S^2}{W\cdot L}$$ and $$\sigma^2\left(\Delta V_{eff}\right)\approx\frac{A_{VT}^2}{W\cdot L}$$

Second-order assumptions

Distance-related, correlations, etc.

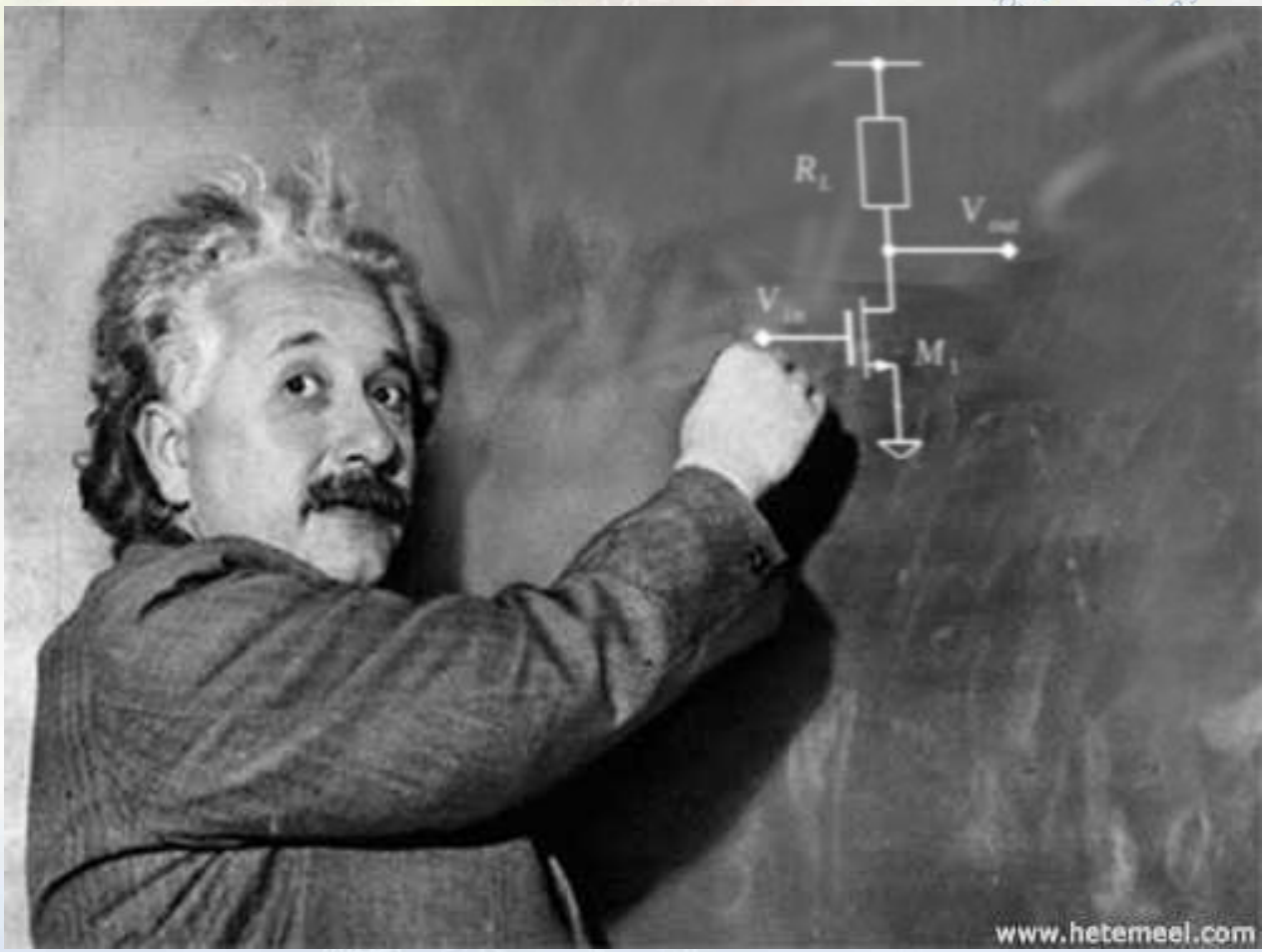
Mismatch, what does this mean?

Unmatched references

- Current mirrors will have different output currents

Offset

- A skewed differential pair can be modeled as an input offset



Mismatch, conclusions

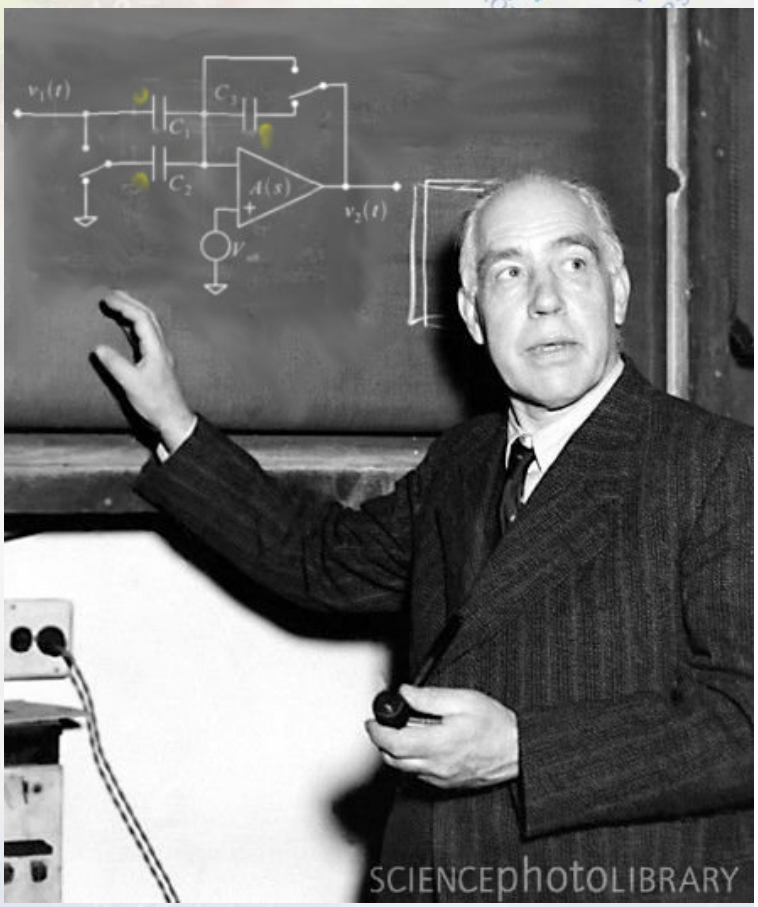
Effective voltage cannot be too low

$$V_{eff} > 100\,mV$$

Transistors need to be very large for high accuracy

Large transistors mean larger capacitors mean slower systems

Mismatch errors will give an offset at input, unbalanced branches and thus poor CMRR and PSRR (power supply rejection).



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What will we do next time?

Operational amplifiers

- Stability
- Frequency analysis
- Compensation